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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4-an

6. AVR CPU

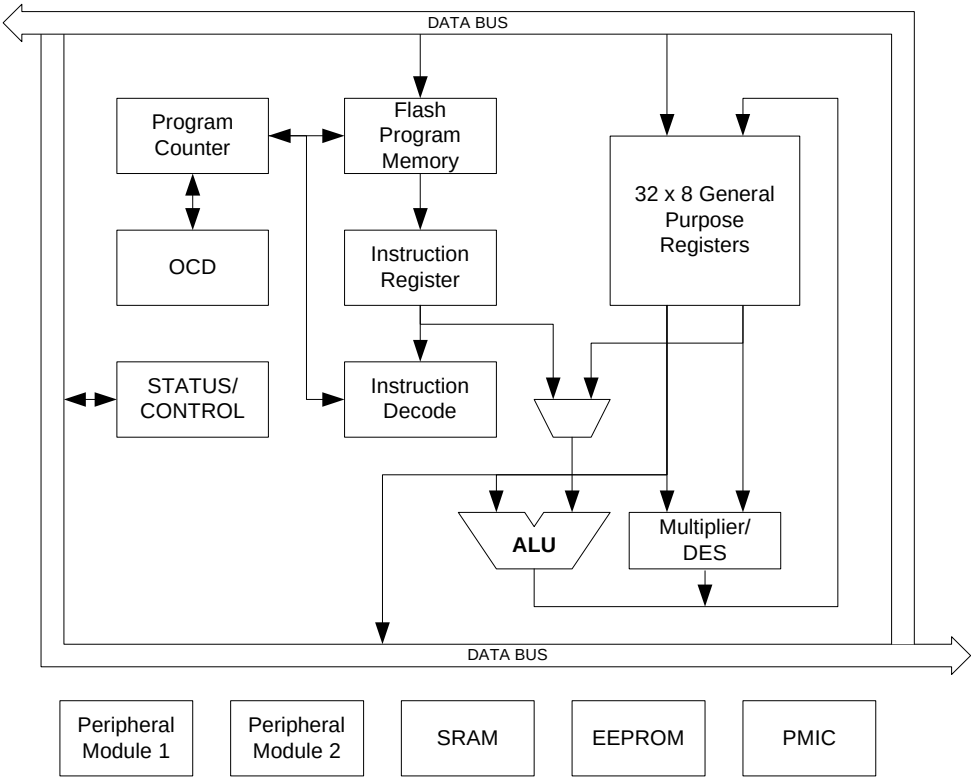
6.1 Features

- **8/16-bit high performance AVR RISC Architecture**
  - **138 instructions**
  - **Hardware multiplier**
- **32x8-bit registers directly connected to the ALU**
- **Stack in RAM**
- **Stack Pointer accessible in I/O memory space**
- **Direct addressing of up to 16M Bytes of program and data memory**
- **True 16/24-bit access to 16/24-bit I/O registers**
- **Support for 8-, 16- and 32-bit Arithmetic**
- **Configuration Change Protection of system critical features**

6.2 Overview

The XMEGA A4 uses the 8/16-bit AVR CPU. The main function of the CPU is program execution. The CPU must therefore be able to access memories, perform calculations and control peripherals. Interrupt handling is described in a separate section. Figure 6-1 on page 8 shows the CPU block diagram.

Figure 6-1. CPU block diagram



The AVR uses a Harvard architecture - with separate memories and buses for program and data. Instructions in the program memory are executed with a single level pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This

10. System Clock and Clock options

10.1 Features

- **Fast start-up time**
- **Safe run-time clock switching**
- **Internal Oscillators:**
  - **32 MHz run-time calibrated RC oscillator**
  - **2 MHz run-time calibrated RC oscillator**
  - **32.768 kHz calibrated RC oscillator**
  - **32 kHz Ultra Low Power (ULP) oscillator with 1 kHz ouput**
- **External clock options**
  - **0.4 - 16 MHz Crystal Oscillator**
  - **32 kHz Crystal Oscillator**
  - **External clock**
- **PLL with internal and external clock options with 1 to 31x multiplication**
- **Clock Prescalers with 1 to 2048x division**
- **Fast peripheral clock running at 2 and 4 times the CPU clock speed**
- **Automatic Run-Time Calibration of internal oscillators**
- **Crystal Oscillator failure detection**

10.2 Overview

XMEGA A4 has an advanced clock system, supporting a large number of clock sources. It incorporates both integrated oscillators, external crystal oscillators and resonators. A high frequency Phase Locked Loop (PLL) and clock prescalers can be controlled from software to generate a wide range of clock frequencies from the clock source input.

It is possible to switch between clock sources from software during run-time. After reset the device will always start up running from the 2 Mhz internal oscillator.

A calibration feature is available, and can be used for automatic run-time calibration of the internal 2 MHz and 32 MHz oscillators. This reduce frequency drift over voltage and temperature.

A Crystal Oscillator Failure Monitor can be enabled to issue a Non-Maskable Interrupt and switch to internal oscillator if the external oscillator fails. Figure 10-1 on page 19 shows the principal clock system in XMEGA A4.

12. System Control and Reset

12.1 Features

- **Multiple reset sources for safe operation and device reset**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
    - **The Watchdog Timer runs from separate, dedicated oscillator**
  - **Brown-Out Reset**
    - **Accurate, programmable Brown-Out levels**
  - **PDI reset**
  - **Software reset**
- **Asynchronous reset**
  - **No running clock in the device is required for reset**
- **Reset status register**

12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, ‘0’, but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, so no running clock is required to reset the device.

After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

12.3 Reset Sources

12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 24.

12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

14. PMIC - Programmable Multi-level Interrupt Controller

14.1 Features

- **Separate interrupt vector for each interrupt**
- **Short, predictable interrupt response time**
- **Programmable Multi-level Interrupt Controller**
  - **3 programmable interrupt levels**
  - **Selectable priority scheme within low level interrupts (round-robin or fixed)**
  - **Non-Maskable Interrupts (NMI)**
- **Interrupt vectors can be moved to the start of the Boot Section**

14.2 Overview

XMEGA A4 has a Programmable Multi-level Interrupt Controller (PMIC). All peripherals can define three different priority levels for interrupts; high, medium or low. Medium level interrupts may interrupt low level interrupt service routines. High level interrupts may interrupt both low- and medium level interrupt service routines. Low level interrupts have an optional round robin scheme to make sure all interrupts are serviced within a certain amount of time.

The built in oscillator failure detection mechanism can issue a Non-Maskable Interrupt (NMI).

14.3 Interrupt vectors

When an interrupt is serviced, the program counter will jump to the interrupt vector address. The interrupt vector is the sum of the peripheral's base interrupt address and the offset address for specific interrupts in each peripheral. The base addresses for the XMEGA A4 devices are shown in Table 14-1. Offset addresses for each interrupt available in the peripheral are described for each peripheral in the XMEGA A manual. For peripherals or modules that have only one interrupt, the interrupt vector is shown in Table 14-1. The program address is the word address.

Table 14-1. Reset and Interrupt Vectors

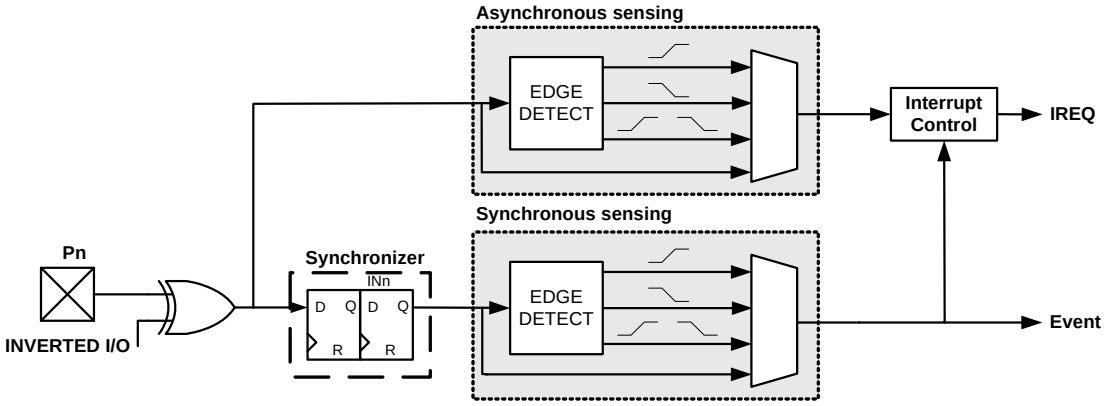
Program Address (Base Address)	Source	Interrupt Description
0x000	RESET	
0x002	OSCF_INT_vect	Crystal Oscillator Failure Interrupt vector (NMI)
0x004	PORTC_INT_base	Port C Interrupt base
0x008	PORTR_INT_base	Port R Interrupt base
0x00C	DMA_INT_base	DMA Controller Interrupt base
0x014	RTC_INT_base	Real Time Counter Interrupt base
0x018	TWIC_INT_base	Two-Wire Interface on Port C Interrupt base
0x01C	TCC0_INT_base	Timer/Counter 0 on port C Interrupt base
0x028	TCC1_INT_base	Timer/Counter 1 on port C Interrupt base
0x030	SPIC_INT_vect	SPI on port C Interrupt vector
0x032	USARTC0_INT_base	USART 0 on port C Interrupt base
0x038	USARTC1_INT_base	USART 1 on port C Interrupt base
0x03E	AES_INT_vect	AES Interrupt vector

15.4 Input sensing

- **Sense both edges**
- **Sense rising edges**
- **Sense falling edges**
- **Sense low level**

Input sensing is synchronous or asynchronous depending on the enabled clock for the ports, and the configuration is shown in Figure 15-7 on page 30.

Figure 15-7. Input sensing system overview



When a pin is configured with inverted I/O, the pin value is inverted before the input sensing.

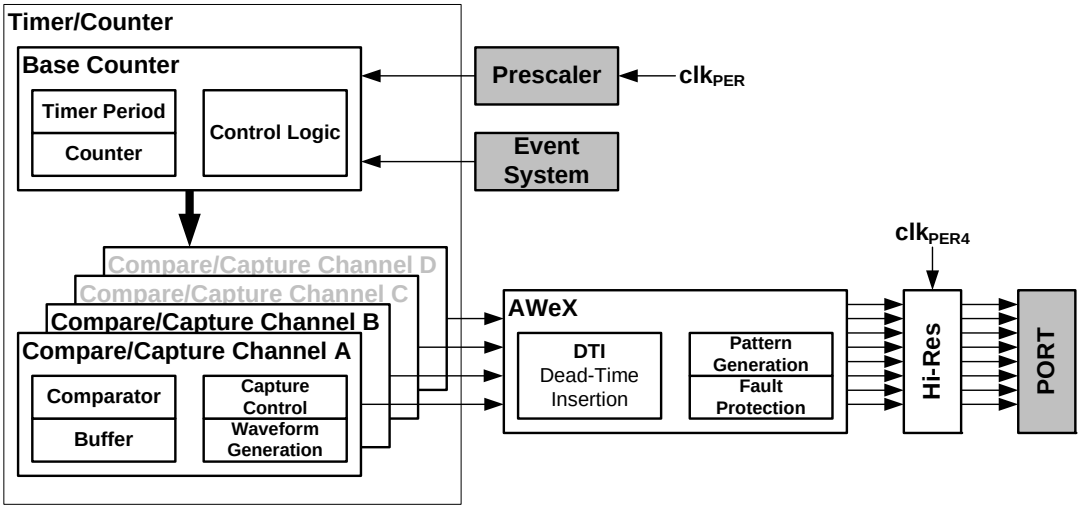
15.5 Port Interrupt

Each port has two interrupts with separate priority and interrupt vector. All pins on the port can be individually selected as source for each of the interrupts. The interrupts are then triggered according to the input sense configuration for each pin configured as source for the interrupt.

15.6 Alternate Port Functions

In addition to the input/output functions on all port pins, most pins have alternate functions. This means that other modules or peripherals connected to the port can use the port pins for their functions, such as communication or pulse-width modulation. ”Pinout and Pin Functions” on page 49 shows which modules on peripherals that enable alternate functions on a pin, and which alternate function is available on a pin.

Figure 16-1. Overview of a Timer/Counter and closely related peripherals



The Hi-Resolution Extension can be enabled to increase the waveform generation resolution by 2 bits (4x). This is available for all Timer/Counters. See ”Hi-Res - High Resolution Extension” on page 34 for more details.

The Advanced Waveform Extension can be enabled to provide extra and more advanced feature for the Timer/Counter. This is only available for Timer/Counter 0. See ”AWEX - Advanced Waveform Extension” on page 33 for more details.

18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by 2-bits (4x)**
- **Supports Frequency, single- and dual-slope PWM operation**
- **Supports the AWEX when this is enabled and used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of 4. When enabled for a Timer/Counter, the Fast Peripheral clock running at four times the CPU clock speed will be as input to the Timer/Counter.

The High Resolution Extension can also be used when an AWEX is enabled and used with a Timer/Counter.

XMEGA A4 devices have three Hi-Res Extensions that each can be enabled for each Timer/Counters pair on PORTC, PORTD and PORTE. The notation of these are HIRESC, HIRESD and HIRESE, respectively.

21. SPI - Serial Peripheral Interface

21.1 Features

- **Two Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

21.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed full-duplex, synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data is transferred both to and from the devices simultaneously.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

25. ADC - 12-bit Analog to Digital Converter

25.1 Features

- **One ADC with 12-bit resolution**
- **2 Msps sample rate**
- **Signed and Unsigned conversions**
- **4 result registers with individual input channel control**
- **12 single ended inputs**
- **8x4 differential inputs**
- **4 internal inputs:**
  - **Integrated Temperature Sensor**
  - **DAC Output**
  - **VCC voltage divided by 10**
  - **Bandgap voltage**
- **Software selectable gain of 2, 4, 8, 16, 32 or 64**
- **Selectable accuracy of 8- or 12-bit.**
- **Internal or External Reference selection**
- **Event triggered conversion for accurate timing**
- **DMA transfer of conversion results**
- **Interrupt/Event on compare result**

25.2 Overview

XMEGA A4 devices have one Analog to Digital Converter (ADC), see Figure 25-1 on page 42.

The ADC converts analog voltages to digital values. The ADC has 12-bit resolution and is capable of converting up to 2 million samples per second. The input selection is flexible, and both single-ended and differential measurements can be done. For differential measurements an optional gain stage is available to increase the dynamic range. In addition several internal signal inputs are available. The ADC can provide both signed and unsigned results.

This is a pipeline ADC. A pipeline ADC consists of several consecutive stages, where each stage convert one part of the result. The pipeline design enables high sample rate at low clock speeds, and remove limitations on samples speed versus propagation delay. This also means that a new analog voltage can be sampled and a new ADC measurement started while other ADC measurements are ongoing.

ADC measurements can either be started by application software or an incoming event from another peripheral in the device. Four different result registers with individual input selection (MUX selection) are provided to make it easier for the application to keep track of the data. Each result register and MUX selection pair is referred to as an ADC Channel. It is possible to use DMA to move ADC results directly to memory or peripherals when conversions are done.

Both internal and external analog reference voltages can be used. An accurate internal 1.0V reference is available.

An integrated temperature sensor is available and the output from this can be measured with the ADC. The output from the DAC, VCC/10 and the Bandgap voltage can also be measured by the ADC.

27. AC - Analog Comparator

27.1 Features

- **Two Analog Comparators**
- **Selectable Power vs. Speed**
- **Selectable hysteresis**
  - **0, 20 mV, 50 mV**
- **Analog Comparator output available on pin**
- **Flexible Input Selection**
  - **All pins on the port**
  - **Output from the DAC**
  - **Bandgap reference voltage.**
  - **Voltage scaler that can perform a 64-level scaling of the internal VCC voltage.**
- **Interrupt and event generation on**
  - **Rising edge**
  - **Falling edge**
  - **Toggle**
- **Window function interrupt and event generation on**
  - **Signal above window**
  - **Signal inside window**
  - **Signal below window**

27.2 Overview

XMEGA A4 features two Analog Comparators (AC). An Analog Comparator compares two voltages, and the output indicates which input is largest. The Analog Comparator may be configured to give interrupt requests and/or events upon several different combinations of input change.

Both hysteresis and propagation delays may be adjusted in order to find the optimal operation for each application.

A wide range of input selection is available, both external pins and several internal signals can be used.

The Analog Comparators are always grouped in pairs (AC0 and AC1) on each analog port. They have identical behavior but separate control registers.

Optionally, the state of the comparator is directly available on a pin.

PORTA has one AC pair. Notation of this peripheral is ACA.

29. Program and Debug Interfaces

29.1 Features

- **PDI - Program and Debug Interface (Atmel proprietary 2-pin interface)**
- **Access to the OCD system**
- **Programming of Flash, EEPROM, Fuses and Lock Bits**

29.2 Overview

The programming and debug facilities are accessed through PDI physical interface. The PDI physical interface uses one dedicated pin together with the Reset pin, and no general purpose pins are used.

29.3 PDI - Program and Debug Interface

The PDI is an Atmel proprietary protocol for communication between the microcontroller and Atmel's development tools.

Figure 35-5. Active Supply Current vs. Vcc

f_{SYS} = 2.0 MHz internal RC.

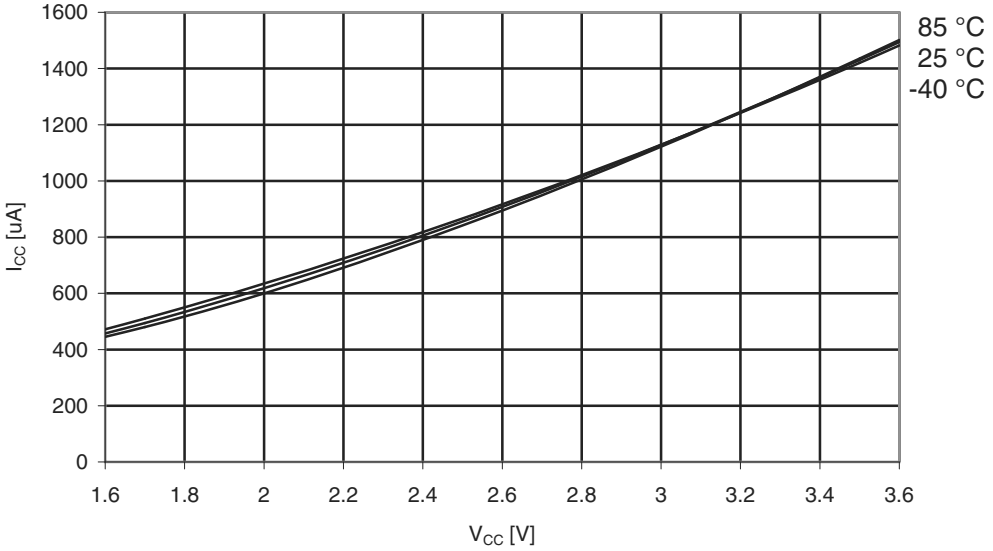
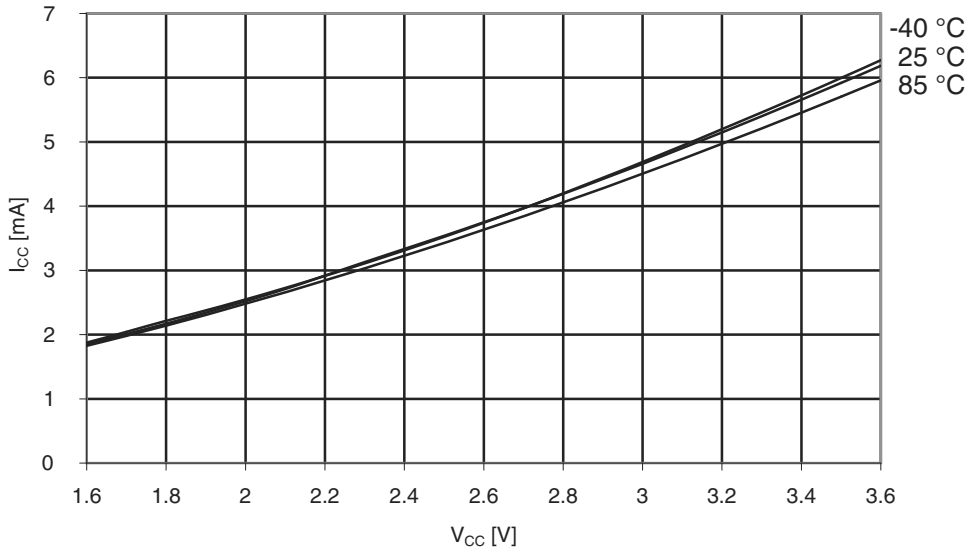


Figure 35-6. Active Supply Current vs. Vcc

f_{SYS} = 32 MHz internal RC prescaled to 8 MHz.



35.3 Power-down Supply Current

Figure 35-15. Power-down Supply Current vs. Temperature

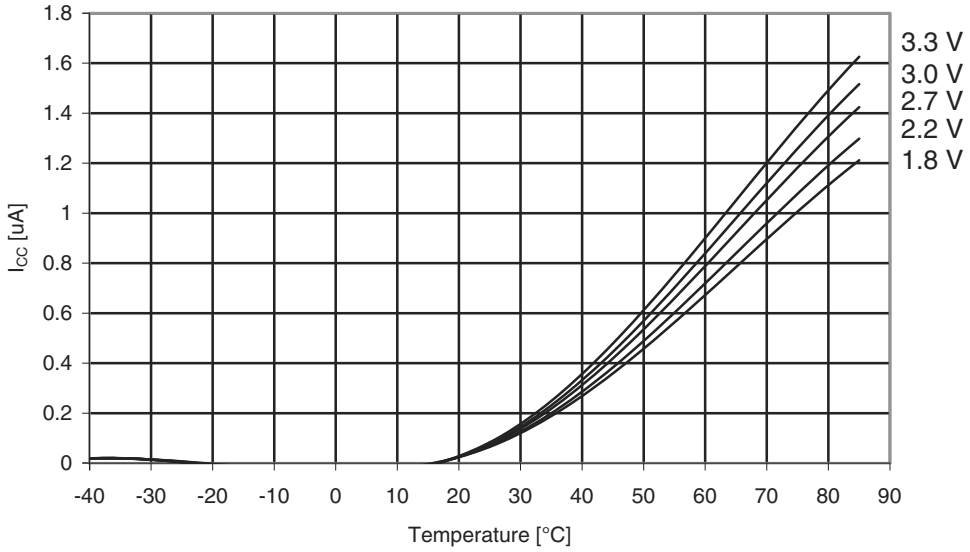
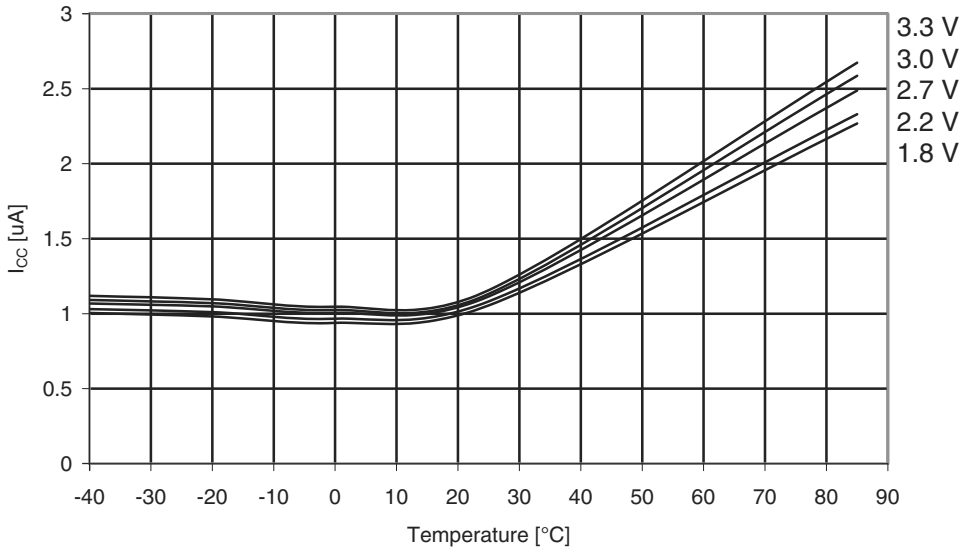


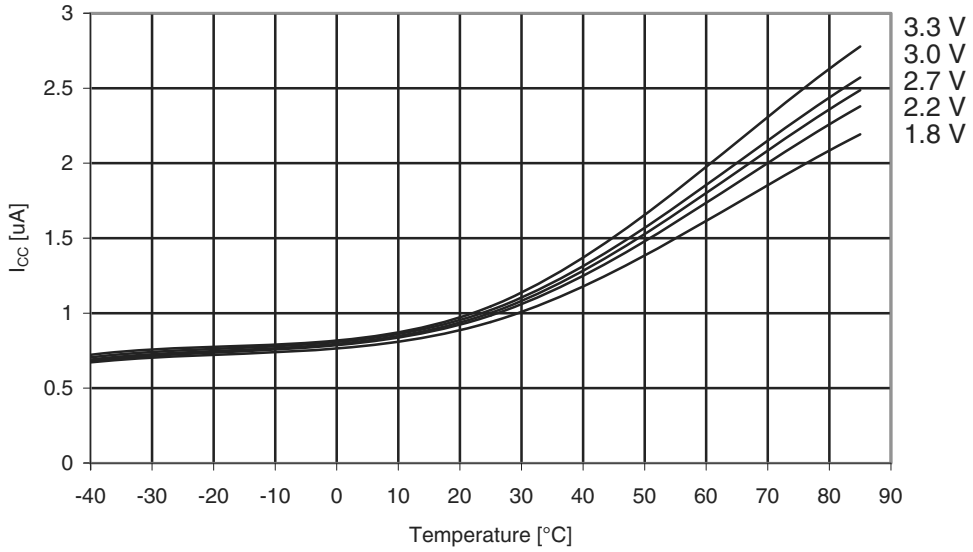
Figure 35-16. Power-down Supply Current vs. Temperature

With WDT and sampled BOD enabled.



35.4 Power-save Supply Current

Figure 35-17. Power-save Supply Current vs. Temperature
With WDT, sampled BOD and RTC from ULP enabled.



35.5 Pin Pull-up

Figure 35-18. Reset Pull-up Resistor Current vs. Reset Pin Voltage
V_{CC} = 1.8V.

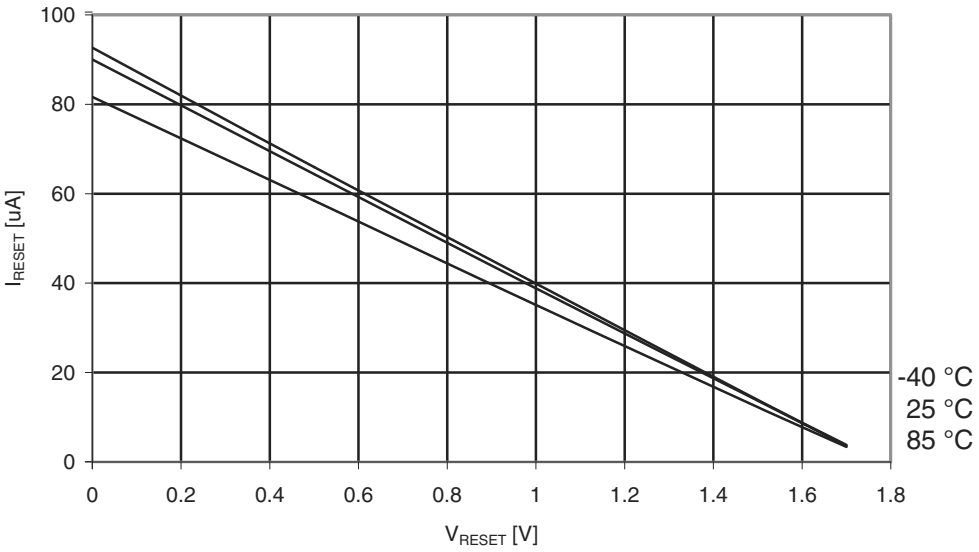


Figure 35-25. I/O Pin Output Voltage vs. Sink Current

Vcc = 3.0V.

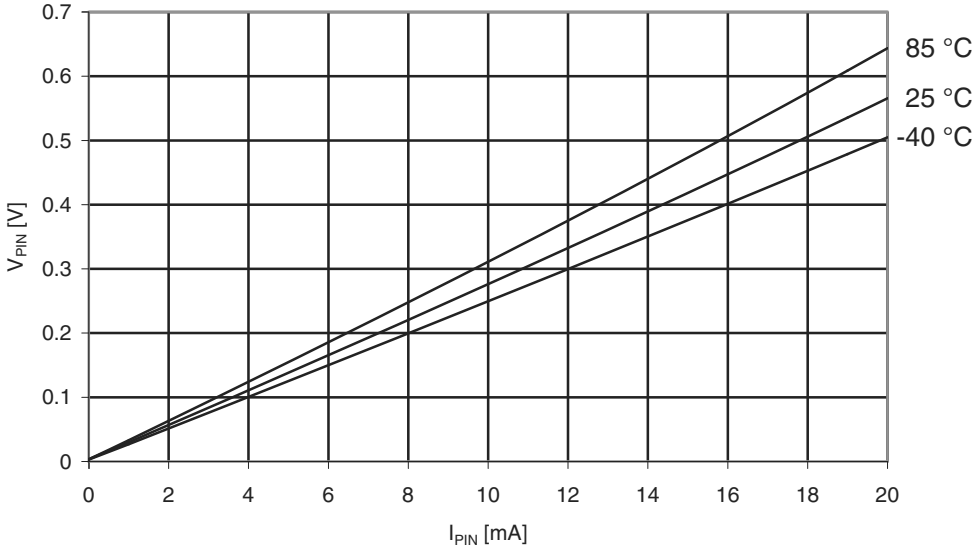


Figure 35-26. I/O Pin Output Voltage vs. Sink Current

Vcc = 3.3V.

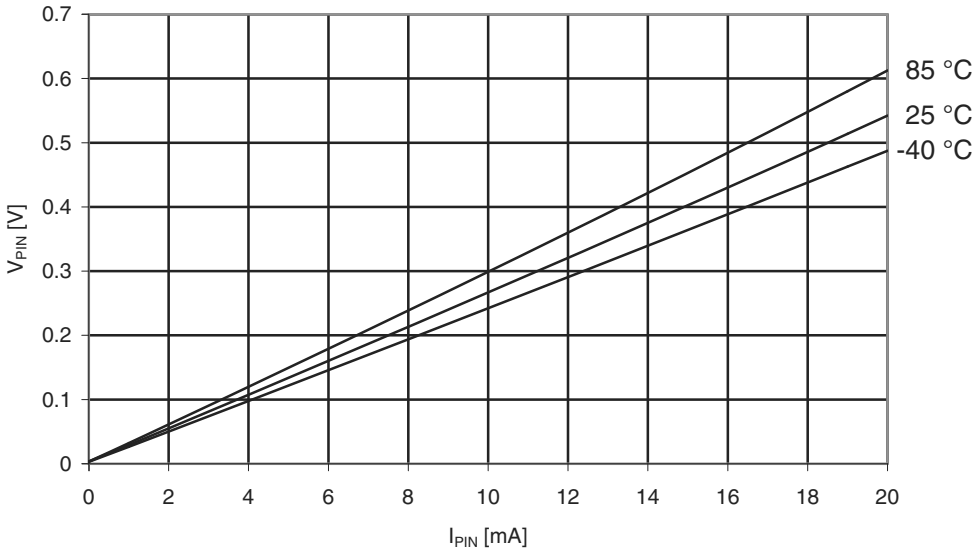
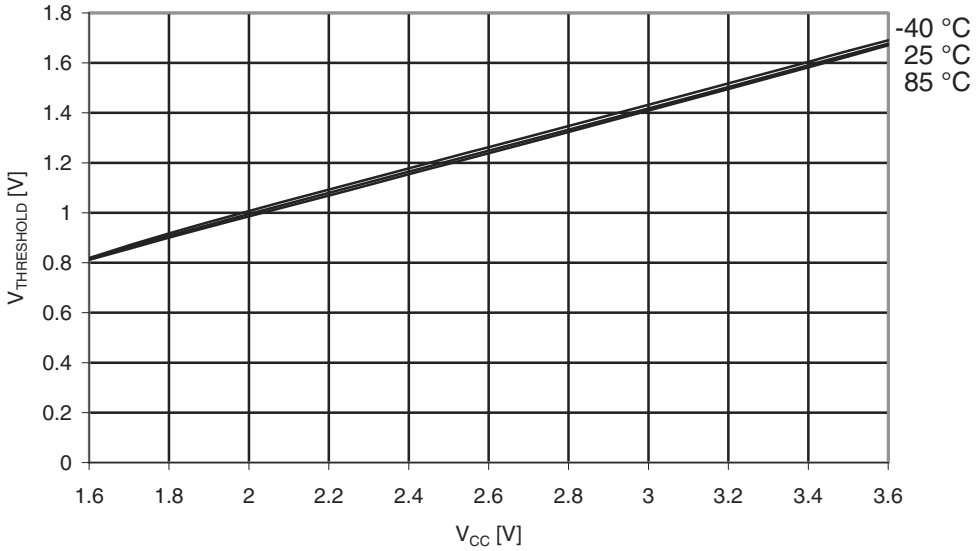


Figure 35-31. Reset Input Threshold Voltage vs. V_{CC}

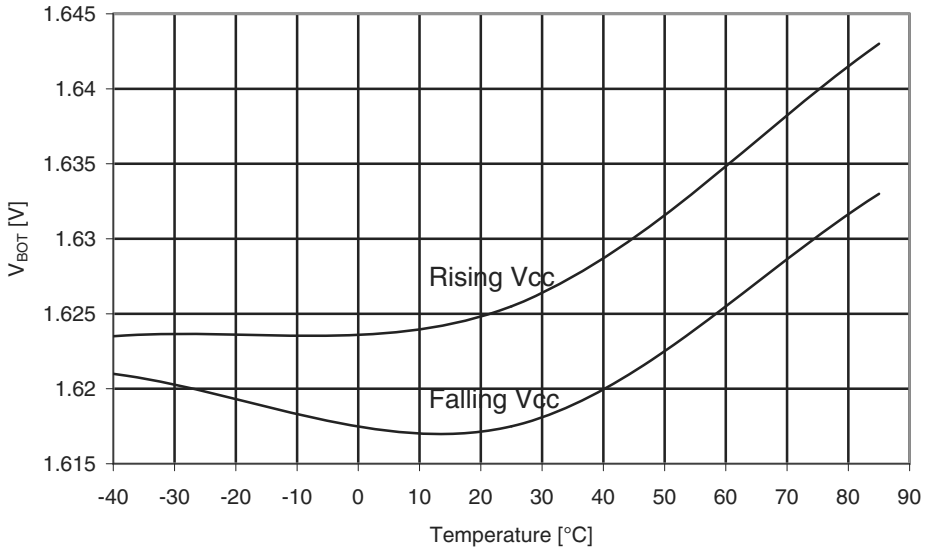
V_{IL} - I/O Pin Read as "0".



35.8 Bod Thresholds

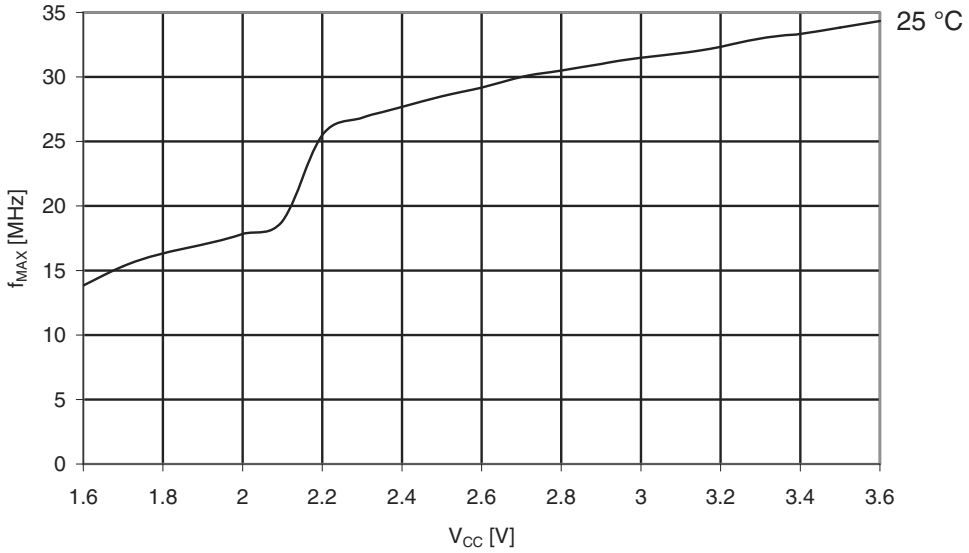
Figure 35-32. BOD Thresholds vs. Temperature

BOD Level = 1.6V.



35.13 PDI Speed

Figure 35-45. PDI Speed vs. Vcc



36. Errata

36.1 ATxmega16A4, ATxmega32A4

36.1.1 rev. A/B

- **Bandgap voltage input for the ACs can not be changed when used for both ACs simultaneously**
- **VCC voltage scaler for AC is non-linear**
- **ADC has increased INL error for some operating conditions**
- **ADC gain stage output range is limited to 2.4 V**
- **ADC Event on compare match non-functional**
- **Bandgap measurement with the ADC is non-functional when VCC is below 2.7V**
- **Accuracy lost on first three samples after switching input to ADC gain stage**
- **Configuration of PGM and CWCM not as described in XMEGA A Manual**
- **PWM is not restarted properly after a fault in cycle-by-cycle mode**
- **BOD: BOD will be enabled at any reset**
- **Sampled BOD in Active mode will cause noise when bandgap is used as reference**
- **DAC is nonlinear and inaccurate when reference is above 2.4V or VCC - 0.6V**
- **DAC has increased INL or noise for some operating conditions**
- **EEPROM page buffer always written when NVM DATA0 is written**
- **Pending full asynchronous pin change interrupts will not wake the device**
- **Pin configuration does not affect Analog Comparator Output**
- **NMI Flag for Crystal Oscillator Failure automatically cleared**
- **Flash Power Reduction Mode can not be enabled when entering sleep**
- **Crystal start-up time required after power-save even if crystal is source for RTC**
- **RTC Counter value not correctly read after sleep**
- **Pending asynchronous RTC-interrupts will not wake up device**
- **TWI Transmit collision flag not cleared on repeated start**
- **Clearing TWI Stop Interrupt Flag may lock the bus**
- **TWI START condition at bus timeout will cause transaction to be dropped**
- **TWI Data Interrupt Flag (DIF) erroneously read as set**
- **WDR instruction inside closed window will not issue reset**

1. **Bandgap voltage input for the ACs cannot be changed when used for both ACs simultaneously**

   If the Bandgap voltage is selected as input for one Analog Comparator (AC) and then selected/deselected as input for another AC, the first comparator will be affected for up to 1 µs and could potentially give a wrong comparison result.

   Problem fix/Workaround

   If the Bandgap is required for both ACs simultaneously, configure the input selection for both ACs before enabling any of them.

2. **VCC voltage scaler for AC is non-linear**

   The 6-bit VCC voltage scaler in the Analog Comparators is non-linear.

37.15 8069D – 08/08

1. Updated ”Features” on page 1 and ”Overview” on page 5.
2. Inserted ”Interrupt Vector Summary.” on page 52.

37.16 8069C – 06/08

1. Updated Figure 2-1 on page 3 and ”Pinout and Pin Functions” on page 49.
2. Updated ”Overview” on page 5.
3. Updated XMEGA A4 Block Diagram, Figure 3-1 on page 6 by removing JTAG from the block diagram.
4. Removed the sections related to JTAG: JTAG Reset and JTAG Interface.
5. Updated Table 14-1 on page 25.
6. Updated all tables in section ”Alternate Pin Functions” on page 51.

37.17 8069B – 06/08

1. Updated ”Features” on page 1.
2. Updated ”Pinout/Block Diagram” on page 3 and ”Pinout and Pin Functions” on page 49.
3. Updated ”Ordering Information” on page 2.
4. Updated ”Overview” on page 5, included the XMEGA A4 explanation text on page 6.
5. Added XMEGA A4 Block Diagram, Figure 3-1 on page 6.
6. Updated AVR CPU ”Features” on page 8 and Updated Figure 6-1 on page 8.
7. Updated Event System block diagram, Figure 9-1 on page 17.
8. Updated ”PMIC - Programmable Multi-level Interrupt Controller” on page 25.
9. Updated ”AC - Analog Comparator” on page 44.
10. Updated ”I/O configuration” on page 27.
11. Inserted a new Figure 16-1 on page 32.
12. Updated ”Peripheral Module Address Map” on page 53.
13. Inserted ”Instruction Set Summary” on page 54.
14. Added Speed grades in ”Speed” on page 63.

37.18 8069A – 02/08

1. Initial revision.