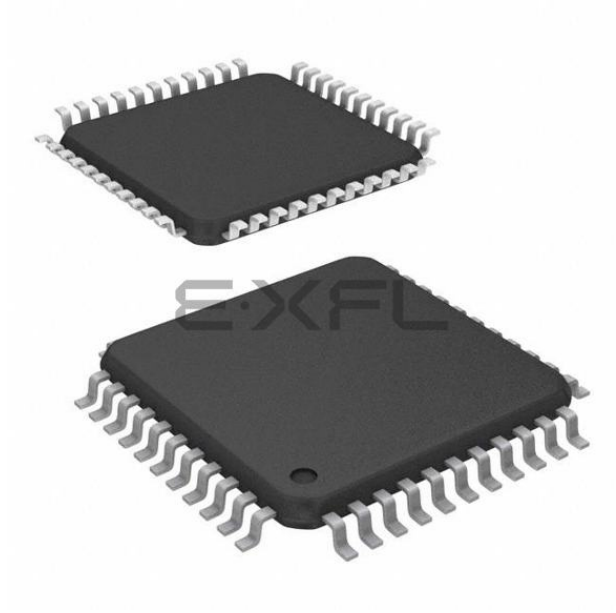

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What is "Embedded - Microcontrollers"?

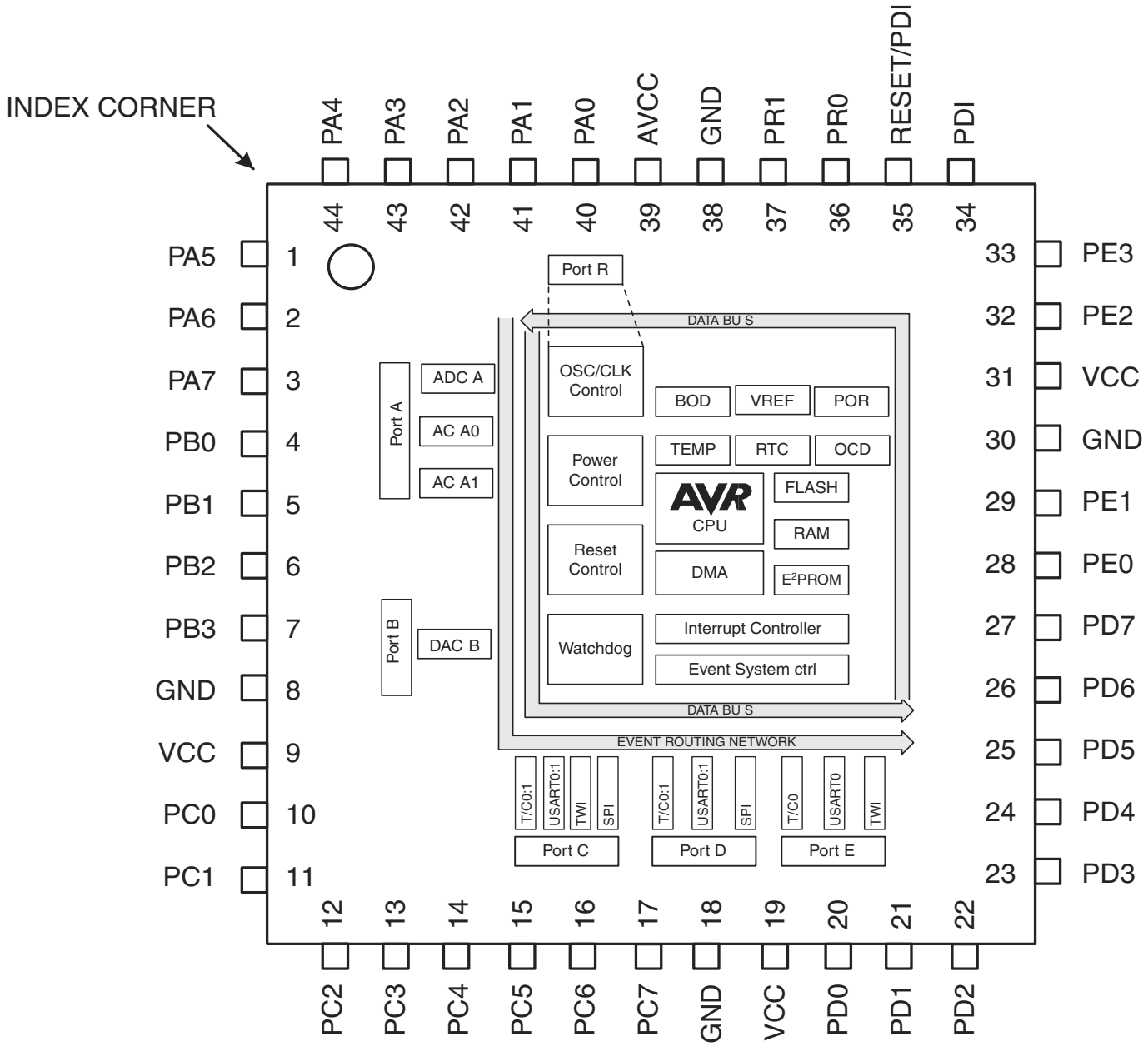
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8/16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 3.6V
Data Converters	A/D 12x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atxmega32a4-au

2. Pinout/Block Diagram

Figure 2-1. Bock Diagram and TQFP/QFN pinout



Notes: 1. For full details on pinout and pin functions refer to ”Pinout and Pin Functions” on page 49.
2. The large center pad underneath the QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

7. Memories

7.1 Features

- **Flash Program Memory**
  - **One linear address space**
  - **In-System Programmable**
  - **Self-Programming and Bootloader support**
  - **Application Section for application code**
  - **Application Table Section for application code or data storage**
  - **Boot Section for application code or bootloader code**
  - **Separate lock bits and protection for all sections**
  - **Built in fast CRC check of a selectable flash program memory section**
- **Data Memory**
  - **One linear address space**
  - **Single cycle access from CPU**
  - **SRAM**
  - **EEPROM**
    - **Byte and page accessible**
    - **Optional memory mapping for direct load and store**
  - **I/O Memory**
    - **Configuration and Status registers for all peripherals and modules**
    - **16 bit-accessible General Purpose Register for global variables or flags**
  - **Bus arbitration**
    - **Safe and deterministic handling of CPU and DMA Controller priority**
  - **Separate buses for SRAM, EEPROM, I/O Memory and External Memory access**
    - **Simultaneous bus access for CPU and DMA Controller**
- **Production Signature Row Memory for factory programmed data**
  - **Device ID for each microcontroller device type**
  - **Serial number for each device**
  - **Oscillator calibration bytes**
  - **ADC, DAC and temperature sensor calibration data**
- **User Signature Row**
  - **One flash page in size**
  - **Can be read and written from software**
  - **Content is kept after chip erase**

7.2 Overview

The AVR architecture has two main memory spaces, the Program Memory and the Data Memory. In addition, the XMEGA A4 features an EEPROM Memory for non-volatile data storage. All three memory spaces are linear and require no paging. The available memory size configurations are shown in ”Ordering Information” on page 2. In addition each device has a Flash memory signature row for calibration data, device identification, serial number etc.

Non-volatile memory spaces can be locked for further write or read/write operations. This prevents unrestricted access to the application software.

7.7 Flash and EEPROM Page Size

The Flash Program Memory and EEPROM data memory are organized in pages. The pages are word accessible for the Flash and byte accessible for the EEPROM.

Table 7-2 on page 14 shows the Flash Program Memory organization. Flash write and erase operations are performed on one page at a time, while reading the Flash is done one byte at a time. For Flash access the Z-pointer (Z[m:n]) is used for addressing. The most significant bits in the address (FPAGE) give the page number and the least significant address bits (FWORD) give the word in the page.

Table 7-2. Number of words and Pages in the Flash.

Devices	Flash Size	Page Size (words)	FWORD	FPAGE	Application		Boot	
					Size	No of Pages	Size	No of Pages
ATxmega16A4	16 KB + 4 KB	128	Z[6:0]	Z[13:7]	16 KB	64	4 KB	16
ATxmega32A4	32 KB + 4 KB	128	Z[6:0]	Z[14:7]	32 KB	128	4 KB	16
ATxmega64A4	64 KB + 4 KB	128	Z[6:0]	Z[15:7]	64 KB	128	4 KB	16
ATxmega128A4	128 KB + 8 KB	256	Z[7:0]	Z[16:8]	128 KB	256	8 KB	16

Table 7-3 on page 14 shows EEPROM memory organization for the XMEGA A4 devices. EEPROM write and erase operations can be performed one page or one byte at a time, while reading the EEPROM is done one byte at a time. For EEPROM access the NVM Address Register (ADDR[m:n]) is used for addressing. The most significant bits in the address (E2PAGE) give the page number and the least significant address bits (E2BYTE) give the byte in the page.

Table 7-3. Number of Bytes and Pages in the EEPROM.

Devices	EEPROM Size	Page Size (Bytes)	E2BYTE	E2PAGE	No of Pages
ATxmega16A4	1 KB	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega32A4	1 KB	32	ADDR[4:0]	ADDR[10:5]	32
ATxmega64A4	2 KB	32	ADDR[4:0]	ADDR[10:5]	64
ATxmega128A4	2 KB	32	ADDR[4:0]	ADDR[10:5]	64

11. Power Management and Sleep Modes

11.1 Features

- **5 sleep modes**
  - **Idle**
  - **Power-down**
  - **Power-save**
  - **Standby**
  - **Extended standby**
- **Power Reduction registers to disable clocks to unused peripherals**

11.2 Overview

The XMEGA A4 provides various sleep modes tailored to reduce power consumption to a minimum. All sleep modes are available and can be entered from Active mode. In Active mode the CPU is executing application code. The application code decides when and what sleep mode to enter. Interrupts from enabled peripherals and all enabled reset sources can restore the microcontroller from sleep to Active mode.

In addition, Power Reduction registers provide a method to stop the clock to individual peripherals from software. When this is done, the current state of the peripheral is frozen and there is no power consumption from that peripheral. This reduces the power consumption in Active mode and Idle sleep mode.

11.3 Sleep Modes

11.3.1 Idle Mode

In Idle mode the CPU and Non-Volatile Memory are stopped, but all peripherals including the Interrupt Controller, Event System and DMA Controller are kept running. Interrupt requests from all enabled interrupts will wake the device.

11.3.2 Power-down Mode

In Power-down mode all system clock sources, and the asynchronous Real Time Counter (RTC) clock source, are stopped. This allows operation of asynchronous modules only. The only interrupts that can wake up the MCU are the Two Wire Interface address match interrupts, and asynchronous port interrupts, e.g pin change.

11.3.3 Power-save Mode

Power-save mode is identical to Power-down, with one exception: If the RTC is enabled, it will keep running during sleep and the device can also wake up from RTC interrupts.

11.3.4 Standby Mode

Standby mode is identical to Power-down with the exception that all enabled system clock sources are kept running, while the CPU, Peripheral and RTC clocks are stopped. This reduces the wake-up time when external crystals or resonators are used.

12. System Control and Reset

12.1 Features

- **Multiple reset sources for safe operation and device reset**
  - **Power-On Reset**
  - **External Reset**
  - **Watchdog Reset**
    - **The Watchdog Timer runs from separate, dedicated oscillator**
  - **Brown-Out Reset**
    - **Accurate, programmable Brown-Out levels**
  - **PDI reset**
  - **Software reset**
- **Asynchronous reset**
  - **No running clock in the device is required for reset**
- **Reset status register**

12.2 Resetting the AVR

During reset, all I/O registers are set to their initial values. The SRAM content is not reset. Application execution starts from the Reset Vector. The instruction placed at the Reset Vector should be an Absolute Jump (JMP) instruction to the reset handling routine. By default the Reset Vector address is the lowest Flash program memory address, ‘0’, but it is possible to move the Reset Vector to the first address in the Boot Section.

The I/O ports of the AVR are immediately tri-stated when a reset source goes active.

The reset functionality is asynchronous, so no running clock is required to reset the device.

After the device is reset, the reset source can be determined by the application by reading the Reset Status Register.

12.3 Reset Sources

12.3.1 Power-On Reset

The MCU is reset when the supply voltage VCC is below the Power-on Reset threshold voltage.

12.3.2 External Reset

The MCU is reset when a low level is present on the RESET pin.

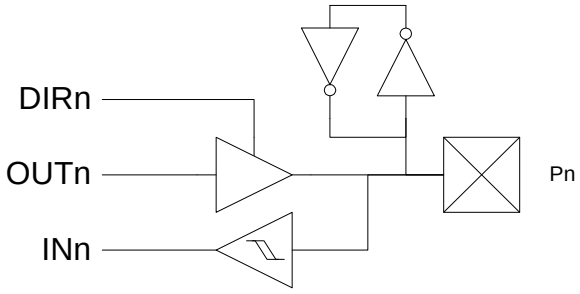
12.3.3 Watchdog Reset

The MCU is reset when the Watchdog Timer period expires and the Watchdog Reset is enabled. The Watchdog Timer runs from a dedicated oscillator independent of the System Clock. For more details see ”WDT - Watchdog Timer” on page 24.

12.3.4 Brown-Out Reset

The MCU is reset when the supply voltage VCC is below the Brown-Out Reset threshold voltage and the Brown-out Detector is enabled. The Brown-out threshold voltage is programmable.

Figure 15-4. I/O configuration - Totem-pole with bus-keeper



15.3.5 Others

Figure 15-5. Output configuration - Wired-OR with optional pull-down

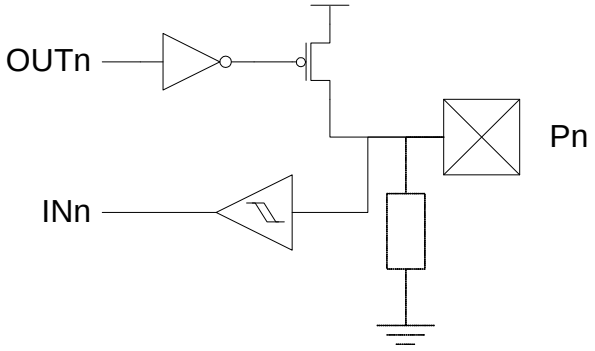
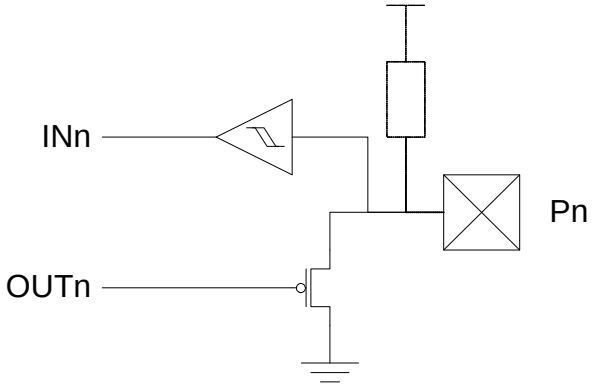


Figure 15-6. I/O configuration - Wired-AND with optional pull-up



18. Hi-Res - High Resolution Extension

18.1 Features

- **Increases Waveform Generator resolution by 2-bits (4x)**
- **Supports Frequency, single- and dual-slope PWM operation**
- **Supports the AWEX when this is enabled and used for the same Timer/Counter**

18.2 Overview

The Hi-Resolution (Hi-Res) Extension is able to increase the resolution of the waveform generation output by a factor of 4. When enabled for a Timer/Counter, the Fast Peripheral clock running at four times the CPU clock speed will be as input to the Timer/Counter.

The High Resolution Extension can also be used when an AWEX is enabled and used with a Timer/Counter.

XMEGA A4 devices have three Hi-Res Extensions that each can be enabled for each Timer/Counters pair on PORTC, PORTD and PORTE. The notation of these are HIRESC, HIRESD and HIRESE, respectively.

21. SPI - Serial Peripheral Interface

21.1 Features

- **Two Identical SPI peripherals**
- **Full-duplex, Three-wire Synchronous Data Transfer**
- **Master or Slave Operation**
- **LSB First or MSB First Data Transfer**
- **Seven Programmable Bit Rates**
- **End of Transmission Interrupt Flag**
- **Write Collision Flag Protection**
- **Wake-up from Idle Mode**
- **Double Speed (CK/2) Master SPI Mode**

21.2 Overview

The Serial Peripheral Interface (SPI) allows high-speed full-duplex, synchronous data transfer between different devices. Devices can communicate using a master-slave scheme, and data is transferred both to and from the devices simultaneously.

PORTC and PORTD each has one SPI. Notation of these peripherals are SPIC and SPID, respectively.

28. OCD - On-chip Debug

28.1 Features

- **Complete Program Flow Control**
  - **Go, Stop, Reset, Step into, Step over, Step out, Run-to-Cursor**
- **Debugging on C and high-level language source code level**
- **Debugging on Assembler and disassembler level**
- **1 dedicated program address or source level breakpoint for AVR Studio / debugger**
- **4 Hardware Breakpoints**
- **Unlimited Number of User Program Breakpoints**
- **Unlimited Number of User Data Breakpoints, with break on:**
  - **Data location read, write or both read and write**
  - **Data location content equal or not equal to a value**
  - **Data location content is greater or less than a value**
  - **Data location content is within or outside a range**
  - **Bits of a data location are equal or not equal to a value**
- **Non-Intrusive Operation**
  - **No hardware or software resources in the device are used**
- **High Speed Operation**
  - **No limitation on debug/programming clock frequency versus system clock frequency**

28.2 Overview

The XMEGA A4 has a powerful On-Chip Debug (OCD) system that - in combination with Atmel's development tools - provides all the necessary functions to debug an application. It has support for program and data breakpoints, and can debug an application from C and high level language source code level, as well as assembler and disassembler level. It has full Non-Intrusive Operation and no hardware or software resources in the device are used. The ODC system is accessed through an external debugging tool which connects to the PDI physical interface. Refer to "Program and Debug Interfaces" on page 48.

30.2 Alternate Pin Functions

The tables below shows the main and alternate pin functions for all pins on each port. It also shows which peripheral which make use of or enable the alternate pin function.

Table 30-1. Port A - Alternate functions

PORTA	PIN #	INTERRUPT	ADCA POS	ADCA NEG	ADCA GAINPOS	ADCA GAINNEG	ACA POS	ACA NEG	ACA OUT	REF
GND	38									
AVCC	39									
PA0	40	SYNC	ADC0	ADC0	ADC0		AC0	AC0		AREF
PA1	41	SYNC	ADC1	ADC1	ADC1		AC1	AC1		
PA2	42	SYNC/ASYNC	ADC2	ADC2	ADC2		AC2			
PA3	43	SYNC	ADC3	ADC3	ADC3		AC3	AC3		
PA4	44	SYNC	ADC4		ADC4	ADC4	AC4			
PA5	1	SYNC	ADC5		ADC5	ADC5	AC5	AC5		
PA6	2	SYNC	ADC6		ADC6	ADC6	AC6			
PA7	3	SYNC	ADC7		ADC7	ADC7		AC7	AC0 OUT	

Table 30-2. Port B - Alternate functions

PORTB	PIN #	INTERRUPT	ADCA POS	DACB	REF
PB0	4	SYNC	ADC8		AREF
PB1	5	SYNC	ADC9		
PB2	6	SYNC/ASYNC	ADC10	DAC0	
PB3	7	SYNC	ADC11	DAC1	

Table 30-3. Port C - Alternate functions

PORTC	PIN #	INTERRUPT	TCC0	AWEXC	TCC1	USARTC0	USARTC1	SPI	TWIC	CLOCKOUT	EVENTOUT
GND	8										
VCC	9										
PC0	10	SYNC	OC0A	OC0ALS					SDA		
PC1	11	SYNC	OC0B	OC0AHS		XCK0			SCL		
PC2	12	SYNC/ASYNC	OC0C	OC0BLS		RXD0					
PC3	13	SYNC	OC0D	OC0BHS		TXD0					
PC4	14	SYNC		OC0CLS	OC1A			$\overline{SS}$			
PC5	15	SYNC		OC0CHS	OC1B		XCK1	MOSI			
PC6	16	SYNC		OC0DLS			RXD1	MISO			
PC7	17	SYNC		OC0DHS			TXD1	SCK		CLKOUT	EVOUT

Mnemonics	Operands	Description	Operation	Flags	#Clocks
CALL	k	call Subroutine	PC ← k	None	3 / 4[1]
RET		Subroutine Return	PC ← STACK	None	4 / 5[1]
RETI		Interrupt Return	PC ← STACK	I	4 / 5[1]
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2 / 3
CP	Rd,Rr	Compare	Rd - Rr	Z,C,N,V,S,H	1
CPC	Rd,Rr	Compare with Carry	Rd - Rr - C	Z,C,N,V,S,H	1
CPI	Rd,K	Compare with Immediate	Rd - K	Z,C,N,V,S,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) PC ← PC + 2 or 3	None	1 / 2 / 3
SBRS	Rr, b	Skip if Bit in Register Set	if (Rr(b) = 1) PC ← PC + 2 or 3	None	1 / 2 / 3
SBIC	A, b	Skip if Bit in I/O Register Cleared	if (I/O(A,b) = 0) PC ← PC + 2 or 3	None	2 / 3 / 4
SBIS	A, b	Skip if Bit in I/O Register Set	If (I/O(A,b) =1) PC ← PC + 2 or 3	None	2 / 3 / 4
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC ← PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC ← PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2
Data Transfer Instructions					
MOV	Rd, Rr	Copy Register	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Pair	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LDS	Rd, k	Load Direct from data space	Rd ← (k)	None	2[1][2]
LD	Rd, X	Load Indirect	Rd ← (X)	None	1[1][2]
LD	Rd, X+	Load Indirect and Post-Increment	Rd ← (X) X ← X + 1	None	1[1][2]
LD	Rd, -X	Load Indirect and Pre-Decrement	X ← X - 1, ← X - 1 Rd ← (X) ← (X)	None	2[1][2]
LD	Rd, Y	Load Indirect	Rd ← (Y) ← (Y)	None	1[1][2]
LD	Rd, Y+	Load Indirect and Post-Increment	Rd ← (Y) Y ← Y + 1	None	1[1][2]

Table 34-1. Current Consumption (Continued)

Symbol	Parameter	Condition		Min.	Typ.	Max.	Units
I_{CC}	Power-save mode	RTC 1 kHz from Low Power 32 kHz TOSC, T = 25°C	V_{CC} = 1.8V		0.5	4	µA
			V_{CC} = 3.0V		0.7	4	
		RTC from Low Power 32 kHz TOSC	V_{CC} = 3.0V		1.16		
	Reset Current Consumption	without Reset pull-up resistor current	V_{CC} = 3.0V		505		
Module current consumption(2)							
I_{CC}	RC32M				470		µA
	RC32M w/DFLL	Internal 32.768 kHz oscillator as DFLL source			600		
	RC2M				112		
	RC2M w/DFLL	Internal 32.768 kHz oscillator as DFLL source			145		
	RC32K				30		
	PLL	Multiplication factor = 10x			225		
	Watchdog normal mode				0.9		
	BOD Continuous mode				120		
	BOD Sampled mode				1		
	Internal 1.00 V ref				80		
	Temperature reference				80		
	RTC with int. 32 kHz RC as source	No prescaling			30		
	RTC with ULP as source	No prescaling			0.9		
	ADC	250 kS/s - Int. 1V Ref			2.9		mA
	DAC Normal Mode	Single channel, Int. 1V Ref			2.4		
	DAC Low-Power Mode	Single channel, Int. 1V Ref			1.1		
	AC High-speed				280		µA
	AC Low-power				110		
	USART	Rx and Tx enabled, 9600 BAUD			5.3		
	DMA				95		
	Timer/Counter	Prescaler DIV1			19		
	AES				140		
	Flash/EEPROM Programming	Vcc = 2V			13		mA
		Vcc = 3V			18		

Note: 1. All Power Reduction Registers set.

2. All parameters measured as the difference in current consumption between module enabled and disabled. All data at V_{CC} = 3.0V, Clk_{SYS} = 1 MHz External clock with no prescaling.

34.5 ADC Characteristics

Table 34-5. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
RES	Resolution	Programmable: 8/12	8	12	12	Bits
INL	Integral Non-Linearity	500 ksps	-5	±2	5	LSB
DNL	Differential Non-Linearity	500 ksps		< ±1		
	Gain Error			< ±10		mV
	Offset Error			< ±2		
ADC_{clk}	ADC Clock frequency	Max is 1/4 of Peripheral Clock			2000	kHz
	Conversion rate				2000	ksps
	Conversion time (propagation delay)	(RES+2)/2+GAIN RES = 8 or 12, GAIN = 0 or 1	5	7	8	ADC_{clk} cycles
	Sampling Time	1/2 ADC_{clk} cycle	0.25			uS
	Conversion range		0		VREF	V
AVCC	Analog Supply Voltage		V_{cc}-0.3		V_{cc}+0.3	
VREF	Reference voltage		1.0		V_{cc}-0.6V	
	Input bandwidth					kHz
INT1V	Internal 1.00V reference(1)			1.00		V
INTVCC	Internal V_{CC}/1.6			V_{CC}/1.6		
SCALEDVCC	Scaled internal V_{CC}/10 input			V_{CC}/10		
R_{AREF}	Reference input resistance			> 10		MΩ
	Start-up time			12	24	ADC_{clk} cycles
	Internal input sampling speed	Temp. sensor, V_{CC}/10, Bandgap			100	ksps

Note: 1. Refer to ”Bandgap Characteristics” on page 66 for more parameter details.

Table 34-6. ADC Gain Stage Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
	Gain error	1 to 64 gain			< ±1		%
	Offset error				< ±1		mV
Vrms	Noise level at input	64x gain	VREF = Int. 1V		0.12		
			VREF = Ext. 2V		0.06		
	Clock rate	Same as ADC				1000	kHz

Figure 35-3. Active Supply Current vs. Vcc

f_{SYS} = 1.0 MHz External Clock.

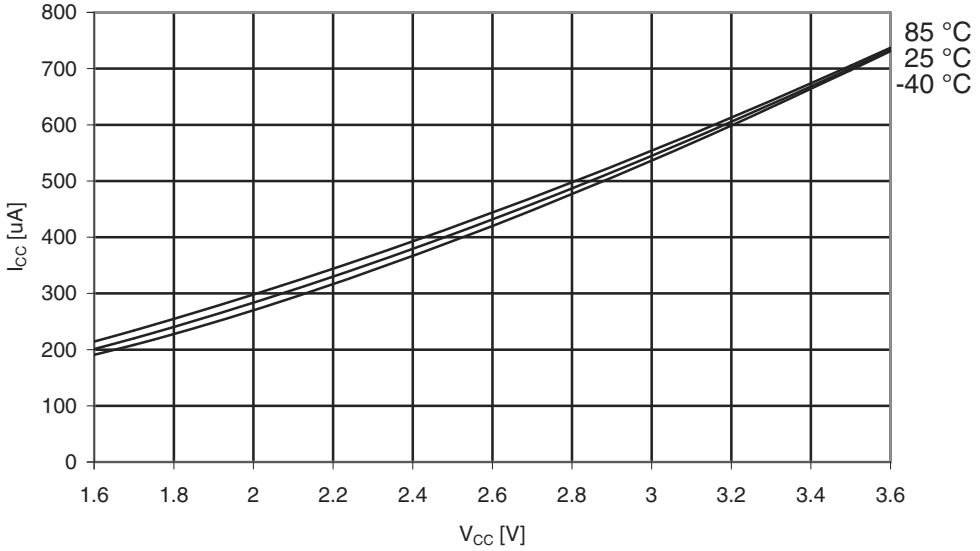


Figure 35-4. Active Supply Current vs. VCC

f_{SYS} = 32.768 kHz internal RC.

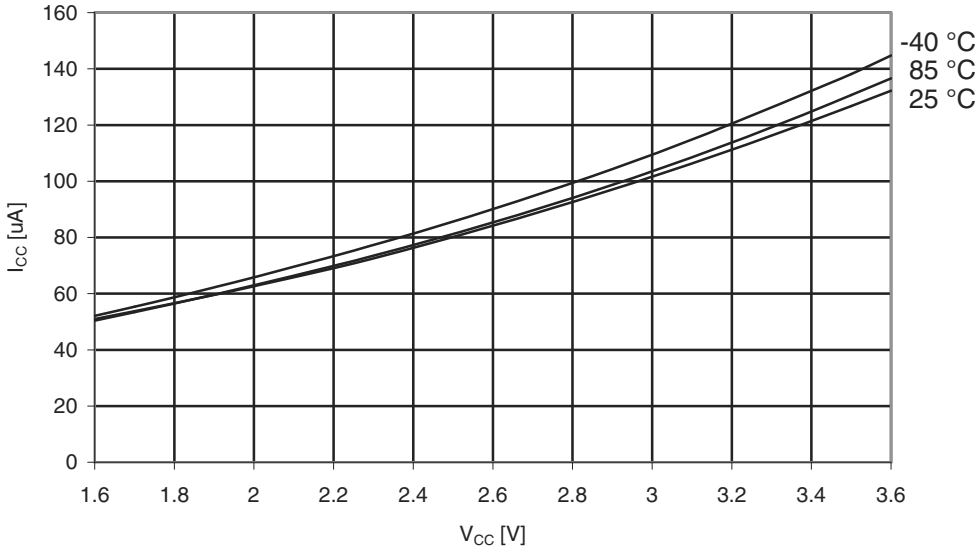


Figure 35-23. I/O Pin Output Voltage vs. Source Current

Vcc = 3.3V.

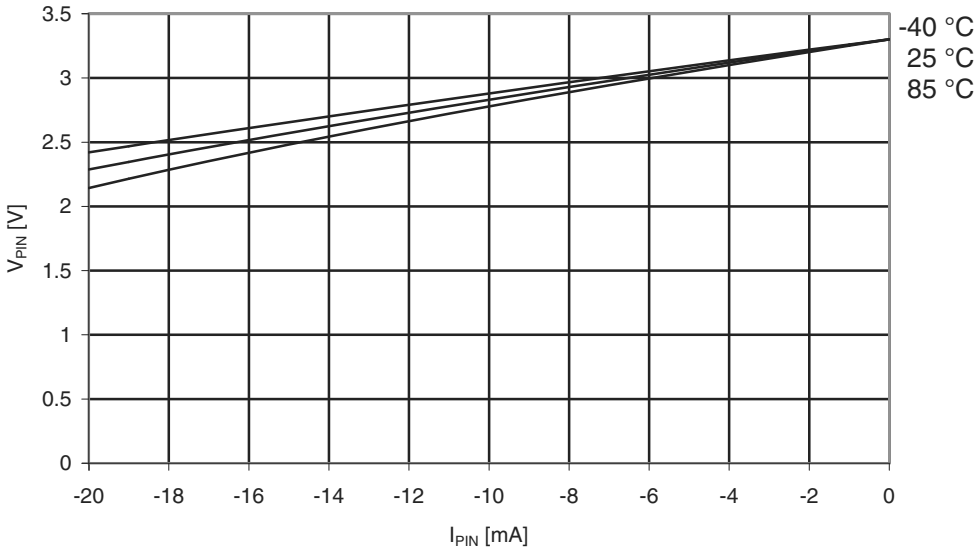
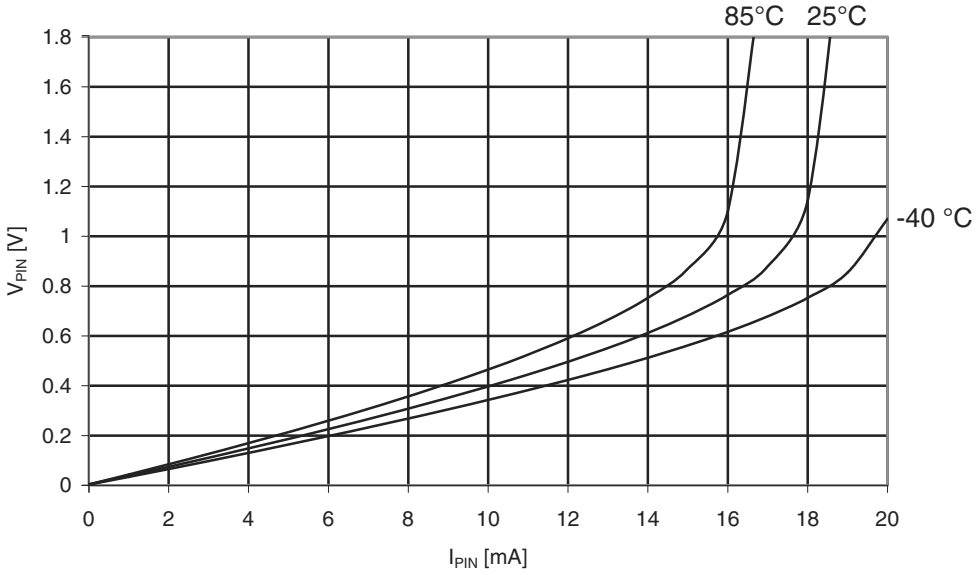


Figure 35-24. I/O Pin Output Voltage vs. Sink Current

Vcc = 1.8V.



35.7 Pin Thresholds and Hysteresis

Figure 35-27. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IH} - I/O Pin Read as "1".

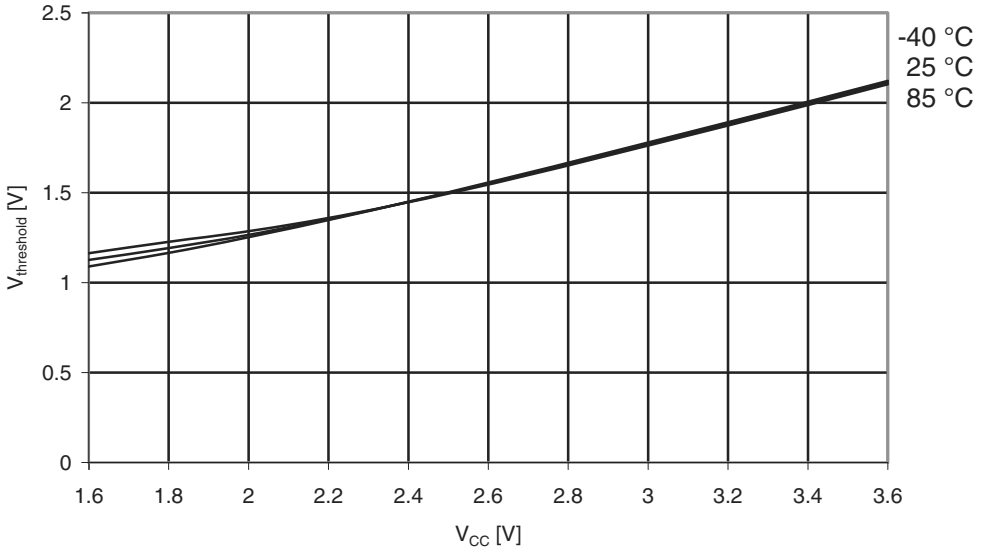


Figure 35-28. I/O Pin Input Threshold Voltage vs. V_{CC}

V_{IL} - I/O Pin Read as "0".

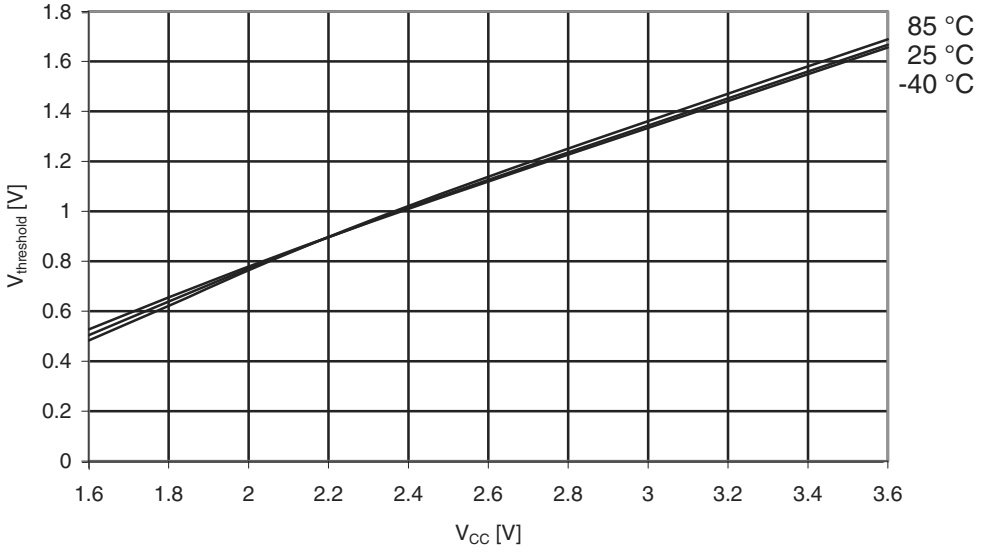
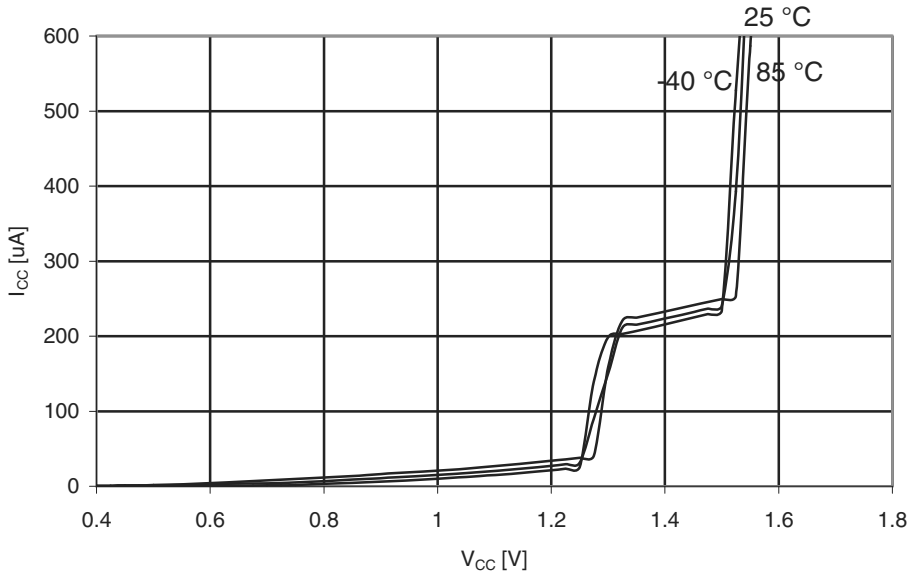


Figure 35-43. Power-up current consumption vs. Vcc



35.12 Reset Pulsewidth

Figure 35-44. Minimum Reset Pulse Width vs. Vcc

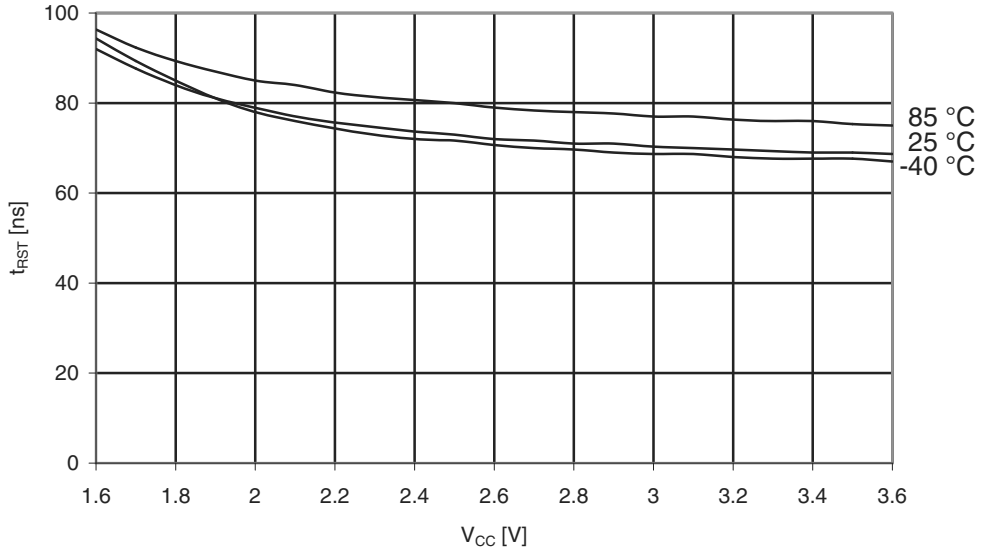
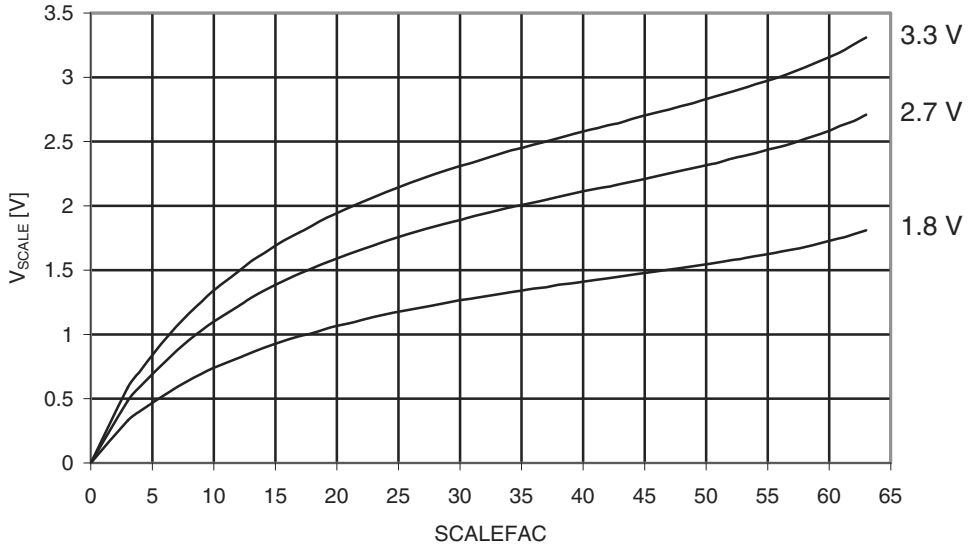


Figure 36-1. Analog Comparator Voltage Scaler vs. Scalefac
T = 25°C



Problem fix/Workaround

Use external voltage input for the analog comparator if accurate voltage levels are needed

3. ADC has increased INL error for some operating conditions

Some ADC configurations or operating condition will result in increased INL error.

In signed mode INL is increased to:

– 6LSB for sample rates above 1Msps, and up to 8 LSB for 2Msps sample rate.

– 6LSB for reference voltage below 1.1V when VCC is above 3.0V.

– 20LSB for ambient temperature below 0 degree C and reference voltage below 1.3V.

In unsigned mode, the INL error cannot be guaranteed, and this mode should not be used.

Problem fix/Workaround

None, avoid using the ADC in the above configurations in order to prevent increased INL error. Use the ADC in signed mode also for single ended measurements.

4. ADC gain stage output range is limited to 2.4 V

The amplified output of the ADC gain stage will never go above 2.4 V, hence the differential input will only give correct output when below 2.4 V/gain. For the available gain settings, this gives a differential input range of:

– 1x gain: 2.4 V

– 2x gain: 1.2 V

– 4x gain: 0.6 V

– 8x gain: 300 mV

– 16x gain: 150 mV

– 32x gain: 75 mV

– 64x gain: 38 mV

For inverted I/O, configure the Analog Comparator to give an inverted result (i.e. connect positive input to the negative AC input and vice versa), or use and external inverter to change polarity of Analog Comparator output.

17. NMI Flag for Crystal Oscillator Failure automatically cleared

NMI flag for Crystal Oscillator Failure (XOSCFDIF) will be automatically cleared when executing the NMI interrupt handler.

Problem fix/Workaround

This device revision has only one NMI interrupt source, so checking the interrupt source in software is not required.

18. Flash Power Reduction Mode can not be enabled when entering sleep

If Flash Power Reduction Mode is enabled when entering Power-save or Extended Standby sleep mode, the device will only wake up on every fourth wake-up request. If Flash Power Reduction Mode is enabled when entering Idle sleep mode, the wake-up time will vary with up to 16 CPU clock cycles.

Problem fix/Workaround

Disable Flash Power Reduction mode before entering sleep mode.

19. Crystal start-up time required after power-save even if crystal is source for RTC

Even if 32.768 kHz crystal is used for RTC during sleep, the clock from the crystal will not be ready for the system before the specified start-up time. See "XOSCSEL[3:0]: Crystal Oscillator Selection" in XMEGA A Manual. If BOD is used in active mode, the BOD will be on during this period (0.5s).

Problem fix/Workaround

If faster start-up is required, go to sleep with internal oscillator as system clock.

20. RTC Counter value not correctly read after sleep

If the RTC is set to wake up the device on RTC Overflow and bit 0 of RTC CNT is identical to bit 0 of RTC PER as the device is entering sleep, the value in the RTC count register can not be read correctly within the first prescaled RTC clock cycle after wakeup. The value read will be the same as the value in the register when entering sleep.

The same applies if RTC Compare Match is used as wake-up source.

Problem fix/Workaround

Wait at least one prescaled RTC clock cycle before reading the RTC CNT value.

21. Pending asynchronous RTC-interrupts will not wake up device

Asynchronous Interrupts from the Real-Time-Counter that is pending when the sleep instruction is executed, will be ignored until the device is woken from another source or the source triggers again.

Problem fix/Workaround

None.

22. TWI Transmit collision flag not cleared on repeated start

The TWI transmit collision flag should be automatically cleared on start and repeated start, but is only cleared on start.

Problem fix/Workaround

Clear the flag in software after address interrupt.

23. Clearing TWI Stop Interrupt Flag may lock the bus

If software clears the STOP Interrupt Flag (APIF) on the same Peripheral Clock cycle as the hardware sets this flag due to a new address received, CLKHOLD is not cleared and the SCL line is not released. This will lock the bus.

Problem fix/Workaround

Check if the bus state is IDLE. If this is the case, it is safe to clear APIF. If the bus state is not IDLE, wait for the SCL pin to be low before clearing APIF.

Code:

```
/* Only clear the interrupt flag if within a "safe zone". */
while ( /* Bus not IDLE: */
       ((COMMS_TWI.MASTER.STATUS & TWI_MASTER_BUSSTATE_gm) !=
         TWI_MASTER_BUSSTATE_IDLE_gc)) &&
         /* SCL not held by slave: */
         !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm)
      )
{
    /* Ensure that the SCL line is low */
    if ( !(COMMS_PORT.IN & PIN1_bm) )
        if ( !(COMMS_PORT.IN & PIN1_bm) )
            break;
}
/* Check for an pending address match interrupt */
if ( !(COMMS_TWI.SLAVE.STATUS & TWI_SLAVE_CLKHOLD_bm) )
{
    /* Safely clear interrupt flag */
    COMMS_TWI.SLAVE.STATUS |= (uint8_t)TWI_SLAVE_APIF_bm;
}
```

24. TWI START condition at bus timeout will cause transaction to be dropped

If Bus Timeout is enabled and a timeout occurs on the same Peripheral Clock cycle as a START is detected, the transaction will be dropped.

Problem fix/Workaround

None.

25. TWI Data Interrupt Flag erroneously read as set

When issuing the TWI slave response command CMD=0b11, it takes 1 Peripheral Clock cycle to clear the data interrupt flag (DIF). A read of DIF directly after issuing the command will show the DIF still set.

Problem fix/Workaround

Add one NOP instruction before checking DIF.

26. WDR instruction inside closed window will not issue reset

When a WDR instruction is execute within one ULP clock cycle after updating the window control register, the counter can be cleared without giving a system reset.

Problem fix/Workaround

Wait at least one ULP clock cycle before executing a WDR instruction.