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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

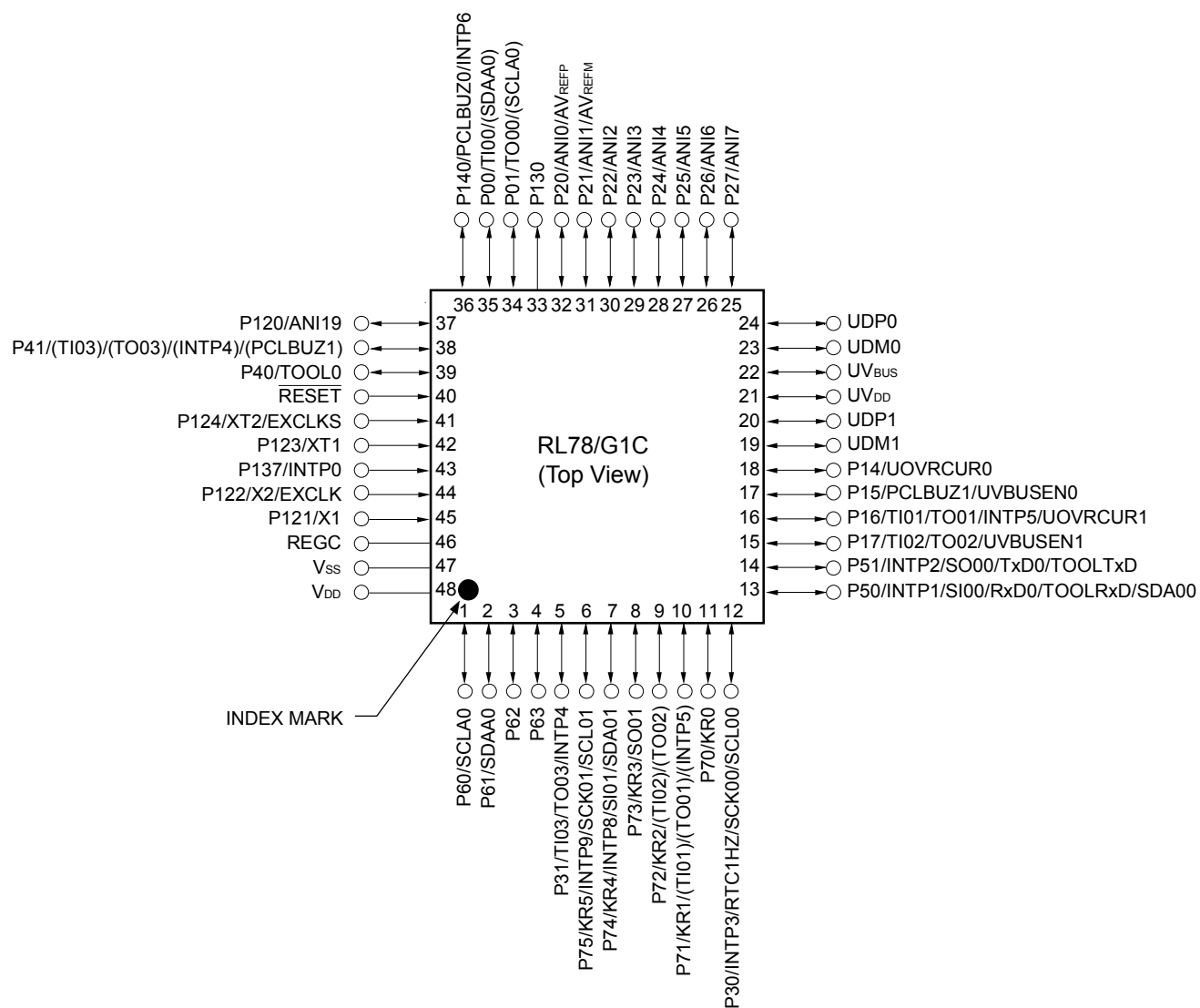
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10jbcafp-v0

1.3.2 48-pin products

- 48-pin plastic LFQFP (fine pitch) (7 × 7, 0.5 mm pitch)

(1) USB function: Host/Function controller (R5F10JGC)

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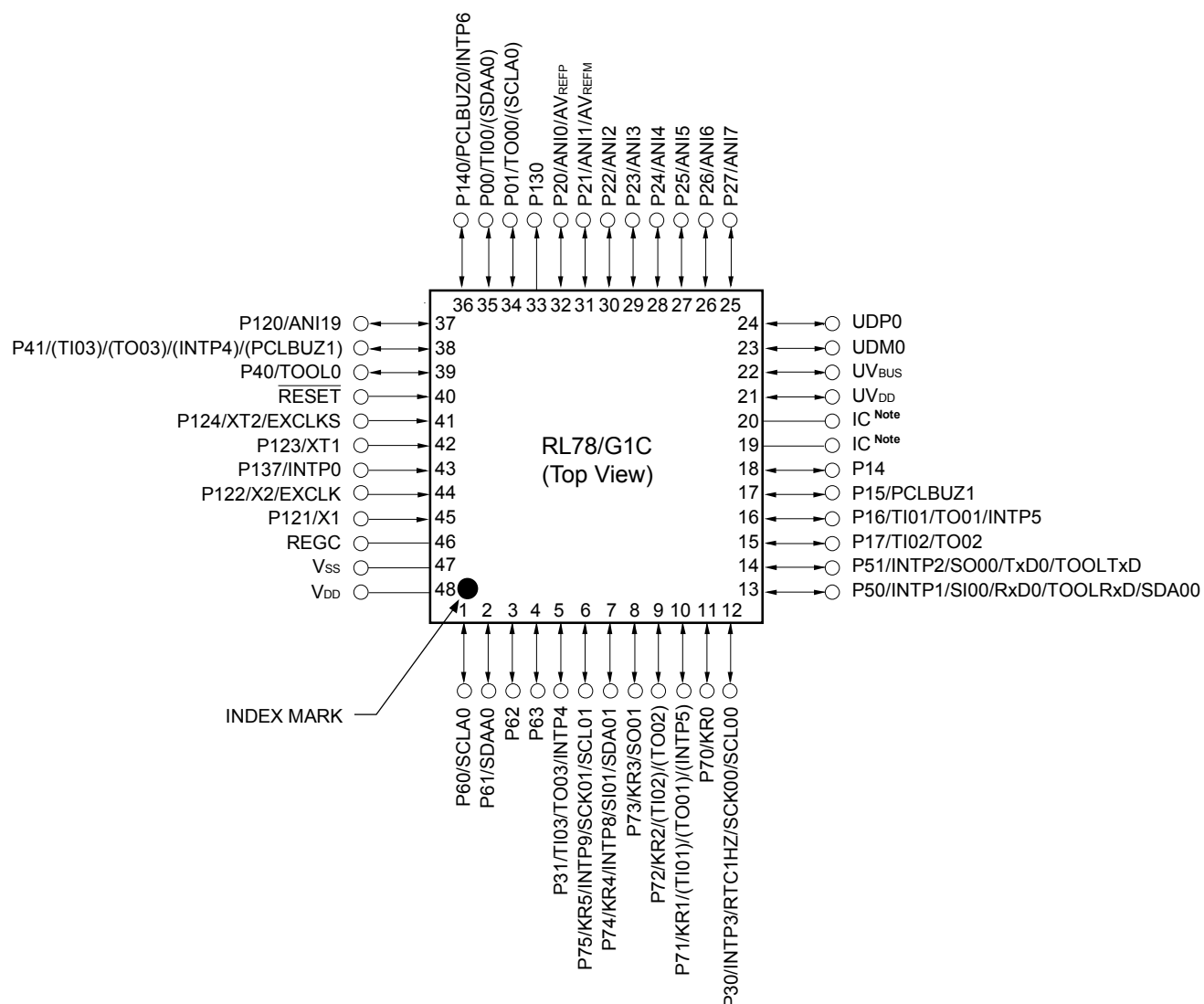
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2) USB function: Function controller only (R5F10KGC)

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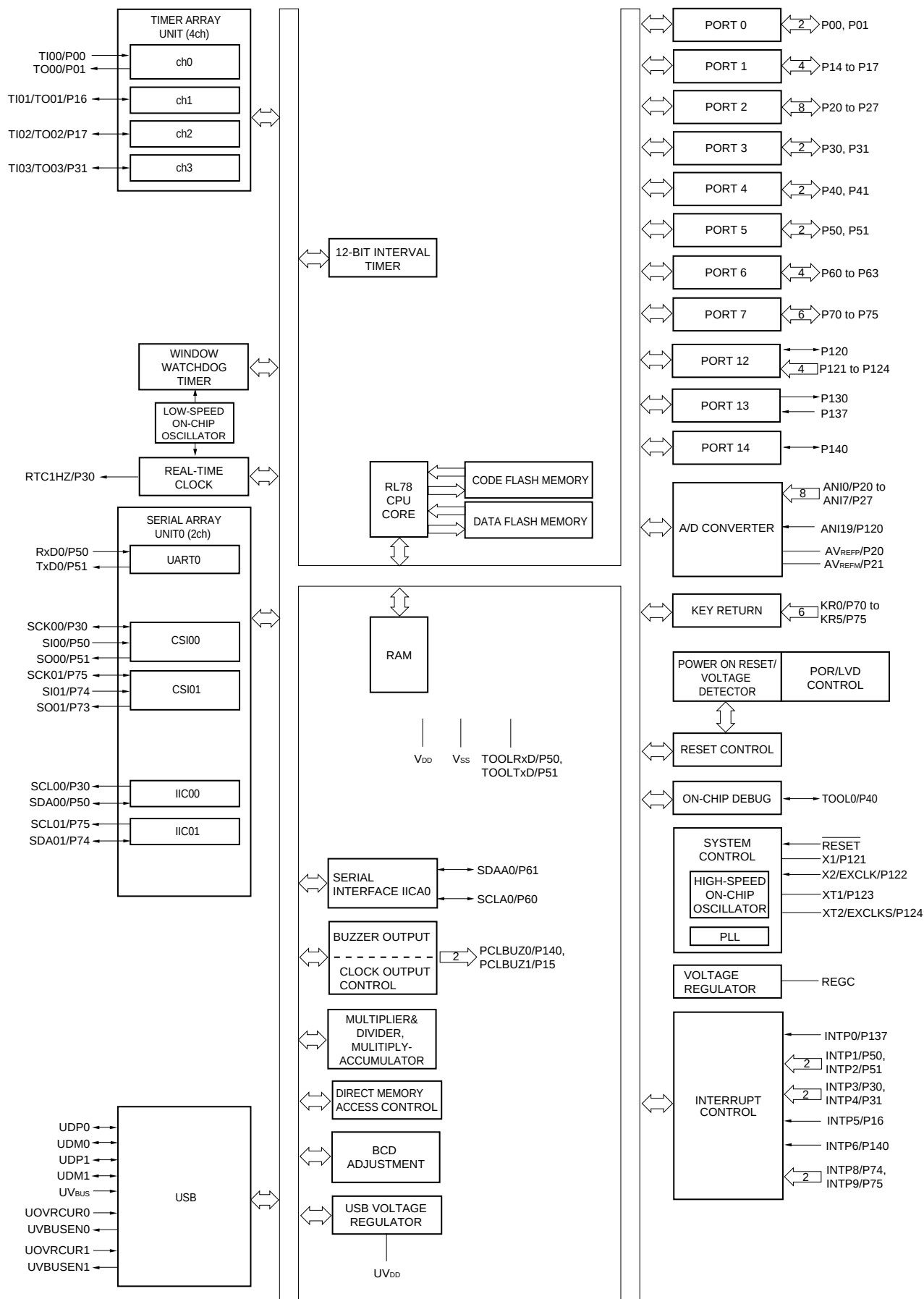
Note IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.2 48-pin products



2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 ^{Note 1}	V
UV _{DD} pin input voltage	V _{IUVDD}	UV _{DD}	-0.3 to V _{DD} +0.3	V
Input voltage	V _{I1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P70 to P75, P120 to P124, P137, P140, EXCLK, EXCLKS, RESET	-0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	UDP0, UDM0, UDP1, UDM1	-0.3 to +6.5	V
	V _{I4}	UV _{BUS}	-0.3 to +6.5	V
Output voltage	V _{O1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	-0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{O2}	UDP0, UDM0, UDP1, UDM1	-0.3 to +6.5	V
Analog input voltage	V _{AI1}	ANI16, ANI17, ANI19	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI7	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V

- Notes 1.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Must be 6.5 V or lower.
- 3.** Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.** AV_{REF} (+) : The + side reference voltage of the A/D converter. This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and V_{DD}.
- 3.** V_{SS} : Reference voltage

(TA = -40 to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	$0.8V_{DD}$	V_{DD}	V
	V_{IH2}	P00, P01, P30, P50	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.2	V_{DD}	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	2.0	V_{DD}	V
			TTL input buffer $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	1.5	V_{DD}	V
	V_{IH3}	P20 to P27	$0.7V_{DD}$		V_{DD}	V
	V_{IH4}	P60 to P63	$0.7V_{DD}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	$0.8V_{DD}$		V_{DD}	V
Input voltage, low	V_{IL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0	$0.2V_{DD}$	V
	V_{IL2}	P00, P01, P30, P50	TTL input buffer $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq V_{DD} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $2.4\text{ V} \leq V_{DD} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20 to P27	0		$0.3V_{DD}$	V
	V_{IL4}	P60 to P63	0		$0.3V_{DD}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		$0.2V_{DD}$	V

Caution The maximum value of V_{IH} of pins P00, P01, P30, and P74 is V_{DD} , even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(6) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}			4.0	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}			4.0	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /6 ^{Note 1}	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 2}			4.0	Mbps

Notes 1. Use it with V_{DD} ≥ V_b.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 5)**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00))

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

 $(T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$ $4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	200			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	300			ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 50$			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 120$			ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 7$			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 10$			ns
Slp setup time (to SCKp $\uparrow$) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	58			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	121			ns
Slp hold time (from SCKp $\uparrow$) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	10			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	10			ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			60	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			130	ns
Slp setup time (to SCKp $\downarrow$) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	23			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	33			ns
Slp hold time (from SCKp $\downarrow$) ^{Note 2}	t_{KSI1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	10			ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	10			ns
Delay time from SCKp $\uparrow$ to SOp output ^{Note 2}	t_{KSO1}	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			10	ns
		$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 20\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(Caution and Remark are listed on the next page.)

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ V _{DD} ≤ 5.5 V	0	100	kHz
			2.4 V ≤ V _{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		250		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		250		μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ V _{DD} ≤ 5.5 V		0	3.45	μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		0	3.45	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.0		μs
Bus-free time	t _{BUF}	2.7 V ≤ V _{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V _{DD} ≤ 5.5 V		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the $\overline{\text{ACK}}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

2.5.3 USB

(1) Electrical specifications

(T_A = -40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

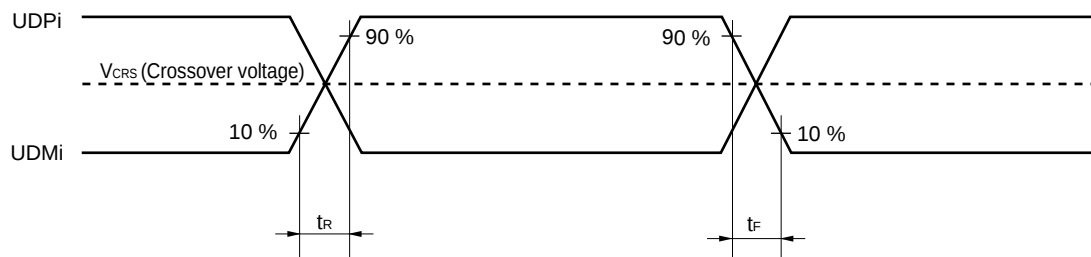
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UV _{DD}	UV _{DD} input voltage characteristic	UV _{DD}	V _{DD} = 3.0 to 5.5 V, PXXCON = 1, VDDUSEB = 0 (UV _{DD} ≤ V _{DD})	3.0	3.3	3.6	V
	UV _{DD} output voltage characteristic	UV _{DD}	V _{DD} = 4.0 to 5.5 V, PXXCON = VDDUSEB = 1	3.0	3.3	3.6	V
UV _{BUS}	UV _{BUS} input voltage characteristic	UV _{BUS}	Function	4.35 (4.02 ^{Note})	5.00	5.25	V
			Host	4.75	5.00	5.25	V

Note Value of instantaneous voltage(T_A = -40 to +85°C, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 3.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi pins input characteristic (FS/LS receiver)	Input voltage	V _{IH}		2.0			V
		V _{IL}				0.8	V
	Difference input sensitivity	V _{DI}	UDP voltage – UDM voltage	0.2			V
	Difference common mode range	V _{CM}		0.8		2.5	V
UDPi/UDMi pins output characteristic (FS driver)	Output voltage	V _{OH}	I _{OH} = -200 μA	2.8		3.6	V
		V _{OL}	I _{OL} = 2.4 mA	0		0.3	V
	Transi-ti on time	t _{FR}	Rising: From 10% to 90 % of amplitude,	4		20	ns
		t _{FF}	Falling: From 90% to 10 % of amplitude,	4		20	ns
	Matching (TFR/TFF)	V _{FRFM}	CL = 50 pF	90		111.1	%
	Crossover voltage	V _{FCRS}		1.3		2.0	V
	Output Impedance	Z _{DRV}	UV _{DD} voltage = 3.3 V, Pin voltage = 1.65 V	28		44	Ω
UDPi/UDMi pins output characteristic (LS driver)	Output voltage	V _{OH}		2.8		3.6	V
		V _{OL}		0		0.3	V
	Transi-ti on time	t _{LR}	Rising: From 10% to 90 % of amplitude,	75		300	ns
		t _{LF}	Falling: From 90% to 10 % of amplitude,	75		300	ns
	Matching (TFR/TFF) Note	V _{LTFM}	CL = 200 to 600 pF	80		125	%
	Crossover voltage Note	V _{LCRS}	When the host controller function is selected: The UDMi pin (i = 0, 1) is pulled up via 1.5 kΩ. When the function controller function is selected: The UDP0 and UDM0 pins are individually pulled down via 15 kΩ	1.3		2.0	V
UDPi/UDMi pins pull-up, pull-down	Pull-down resistor	R _{PD}		14.25		24.80	kΩ
	Pull-up resistor (i = 0 only)	R _{PUI}	Idle	0.9		1.575	kΩ
		R _{PUA}	Recep-t ion	1.425		3.09	kΩ
UV _{BUS}	UV _{BUS} pull-down resistor	R _{VBUS}	UV _{BUS} voltage = 5.5 V		1000		kΩ
	UV _{BUS} input voltage	V _{IH}		3.20			V
		V _{IL}				0.8	V

Note Excludes the first signal transition from the idle state.**Remark** i = 0, 1

Timing of UDPI and UDMI



(2) BC standard

(
 $T_A = -40$ to $+85^{\circ}\text{C}$, $3.0\text{ V} \leq UV_{DD} \leq 3.6\text{ V}$, $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB standard BC1.2	UDPi sink current	I_{DP_SINK}		25		175	μA
	UDMi sink current	I_{DM_SINK}		25		175	μA
	DCD source current	I_{DP_SRC}		7		13	μA
	Dedicated charging port resistor	R_{DCP_DAT}	$0\text{ V} < \text{UDP/UDM voltage} < 1.0\text{ V}$			200	Ω
	Data detection voltage	V_{DAT_REF}		0.25		0.4	V
	UDPi source voltage	V_{DP_SRC}	Output current $250\text{ }\mu\text{A}$	0.5		0.7	V
	UDMi source voltage	V_{DM_SRC}	Output current $250\text{ }\mu\text{A}$	0.5		0.7	V

Remark i = 0, 1

(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (–) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0 to ANI7, ANI16, ANI17, ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = AV_{REFM} ^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			Bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	EZS	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = -40 to $+85^{\circ}\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

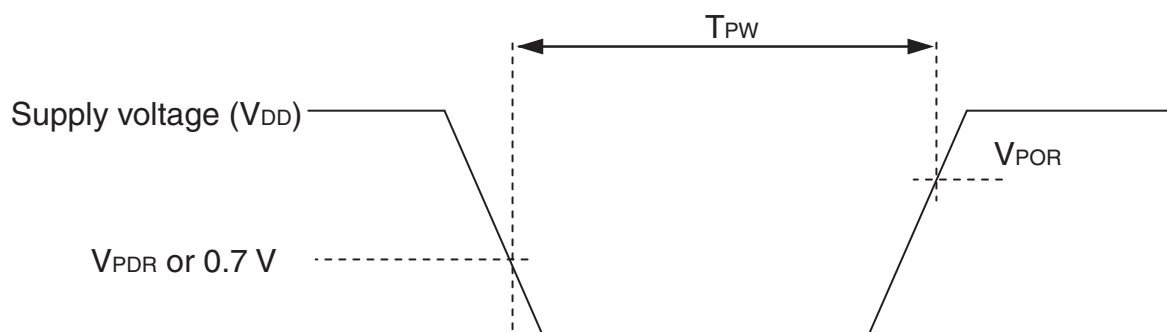
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMP25}	Setting ADS register = 80H, T _A = $+25^{\circ}\text{C}$		1.05		V
Internal reference voltage	V _{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMP25}	Temperature sensor that depends on the temperature		-3.6		mV/ $^{\circ}\text{C}$
Operation stabilization wait time	t _{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = -40 to $+85^{\circ}\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	Power supply rise time	1.47	1.51	1.55	V
	V _{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock (f_{MAIN}) is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	−40	mA
		Total of all pins −170 mA	P00, P01, P40, P41, P120, P130, P140	−70	mA
			P14 to P17, P30, P31, P50, P51, P70 to P75	−100	mA
	I _{OH2}	Per pin	P20 to P27	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I _{OL1}	Per pin	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	40	mA
		Total of all pins 170 mA	P00, P01, P40, P41, P120, P130, P140	70	mA
			P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75	100	mA
	I _{OL2}	Per pin	P20 to P27	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T _A	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2.3 PLL oscillator characteristics

(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency ^{Note}	f _{PLLIN}	High-speed system clock	6.00		16.00	MHz
PLL output frequency ^{Note}	f _{PLL}			48.00		MHz
Lock up time		From PLL output enable to stabilization of the output frequency	40.00			μs
Interval time		From PLL stop to PLL re-operation setting Wait time	4.00			μs
Setting wait time		From after PLL input clock stabilization and PLL setting is fixed to start setting Wait time required	1.00			μs

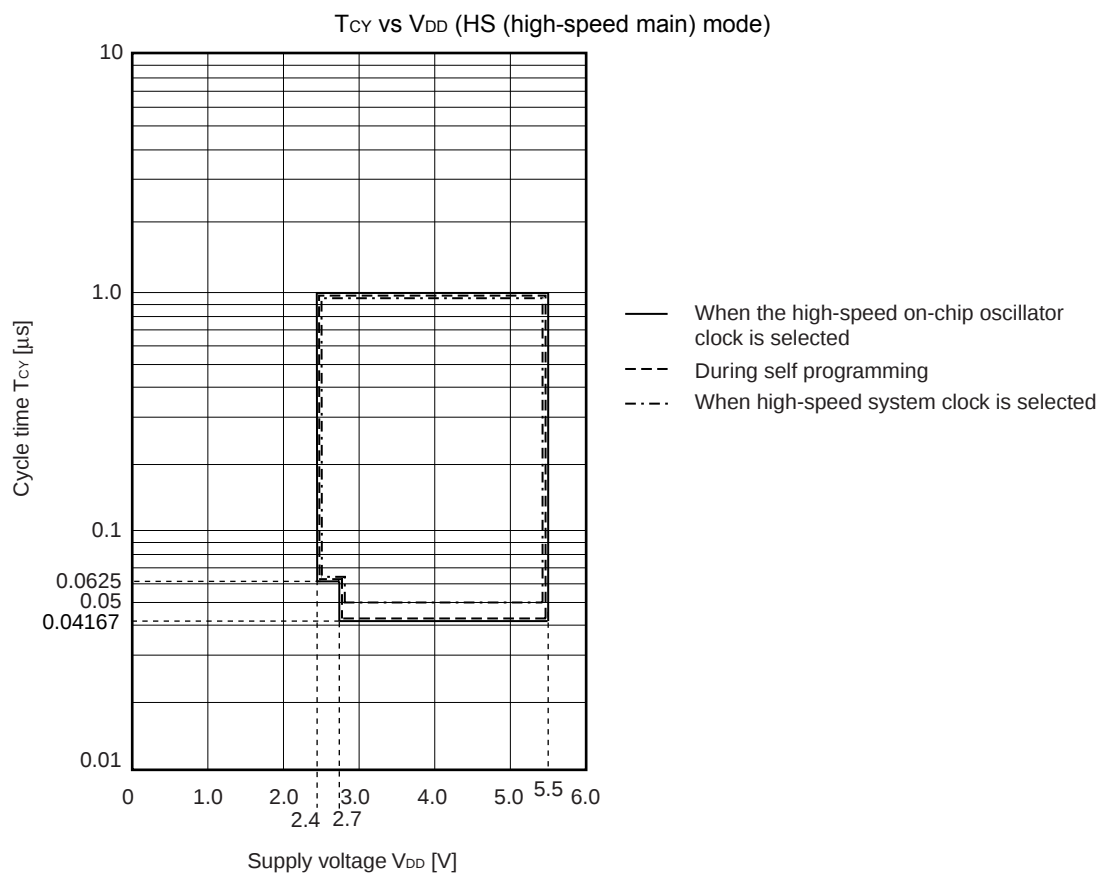
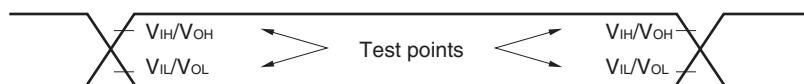
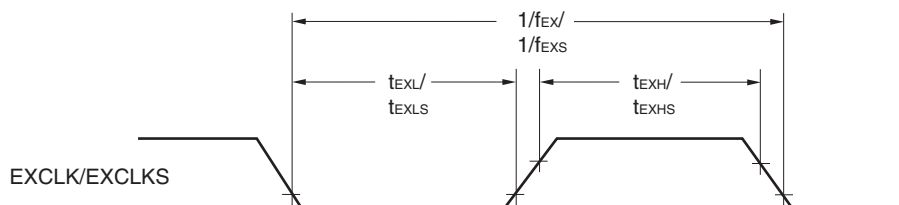
Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

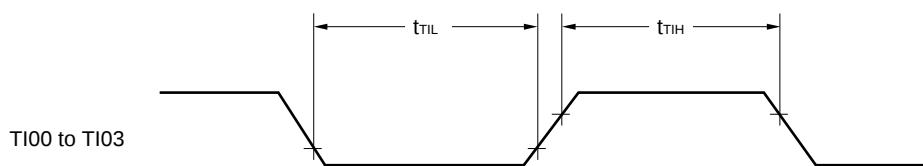
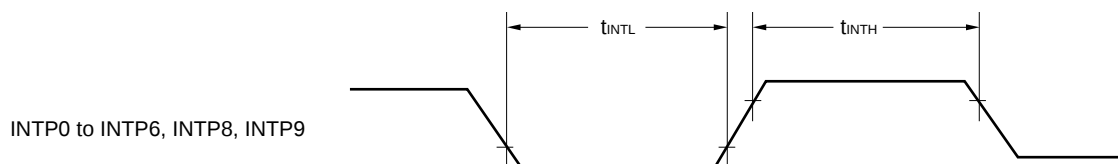
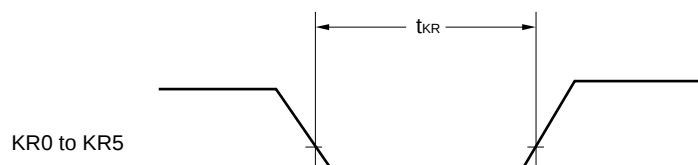
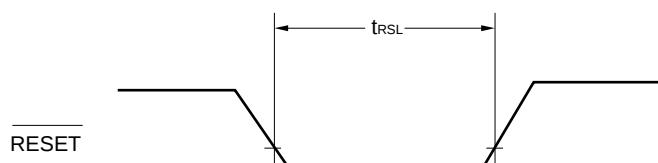
(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0.8V _{DD}	V _{DD}	V
	V _{IH2}	P00, P01, P30, P50	TTL input buffer 4.0 V ≤ V _{DD} ≤ 5.5 V	2.2	V _{DD}	V
			TTL input buffer 3.3 V ≤ V _{DD} < 4.0 V	2.0	V _{DD}	V
			TTL input buffer 2.4 V ≤ V _{DD} < 3.3 V	1.5	V _{DD}	V
	V _{IH3}	P20 to P27	0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60 to P63	0.7V _{DD}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	Normal input buffer	0	0.2V _{DD}	V
	V _{IL2}	P00, P01, P30, P50	TTL input buffer 4.0 V ≤ V _{DD} ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ V _{DD} < 4.0 V	0	0.5	V
			TTL input buffer 2.4 V ≤ V _{DD} < 3.3 V	0	0.32	V
	V _{IL3}	P20 to P27	0		0.3V _{DD}	V
	V _{IL4}	P60 to P63	0		0.3V _{DD}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P00, P01, P30, and P74 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Points****External System Clock Timing**

TI/TO Timing**Interrupt Request Input Timing****Key Interrupt Input Timing** **$\overline{\text{RESET}}$ Input Timing**

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (1/2)**(T_A = -40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V _{DD} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			f _{MCK} /12 Note 1	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 24 MHz, f _{MCK} = f _{CLK} Note 2			2.0	Mbps
			2.7 V ≤ V _{DD} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			f _{MCK} /12 Note 1	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 24 MHz, f _{MCK} = f _{CLK} Note 2			2.0	Mbps
			2.4 V ≤ V _{DD} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			f _{MCK} /12 Note 1	bps
			Theoretical value of the maximum transfer rate f _{CLK} = 24 MHz, f _{MCK} = f _{CLK} Note 2			2.0	Mbps

Notes 1. Use it with V_{DD} ≥ V_b.**2.** The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected

Remarks 1. V_b[V]: Communication line voltage**2.** q: UART number (q = 0), g: PIM and POM number (g = 5)**3.** f_{MCK}: Serial array unit operation clock frequency

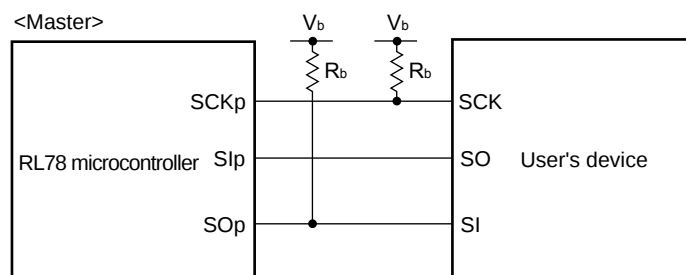
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00)

- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. Use it with $V_{DD} \geq V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number, n: Channel number ($mn = 00$), g: PIM and POM number ($g = 0, 3, 5, 7$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number ($mn = 00$))
 4. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

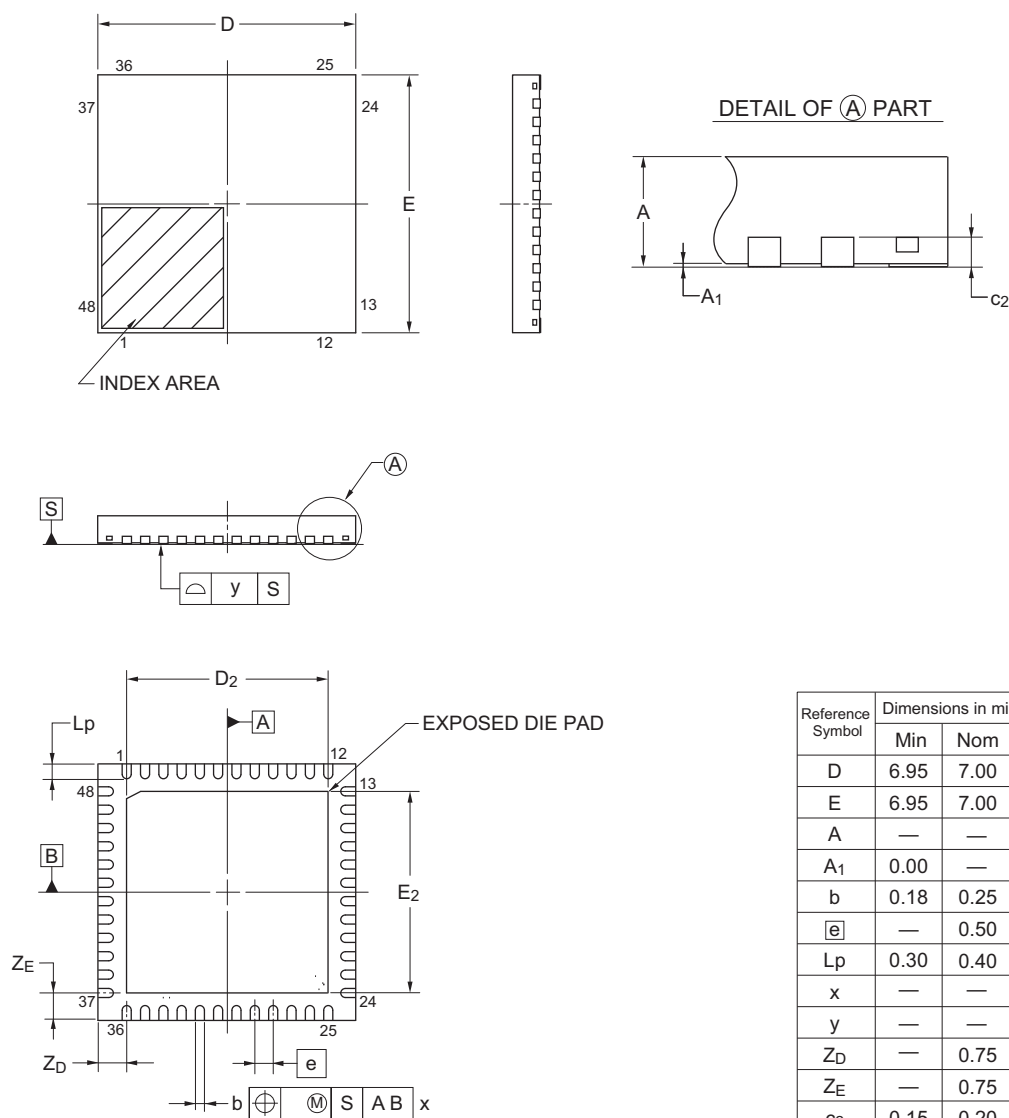
R5F10JGCANA, R5F10KGCANA

R5F10JGCGNA, R5F10KGCNA

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13

Unit: mm



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