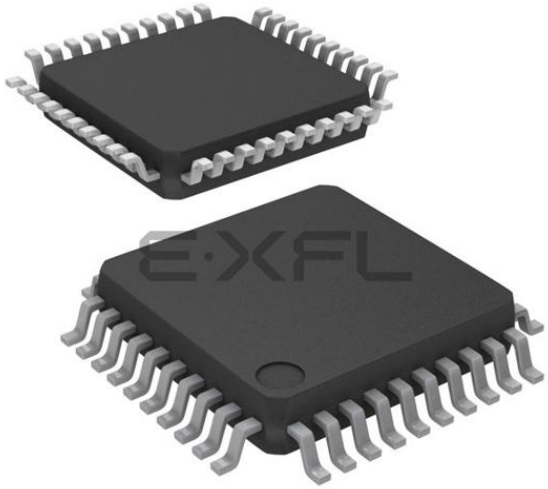
Renesas Electronics America Inc - R5F10JBCGFP#V0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10jbcgfp-v0

(2) USB function: Function controller only (R5F10KBC)

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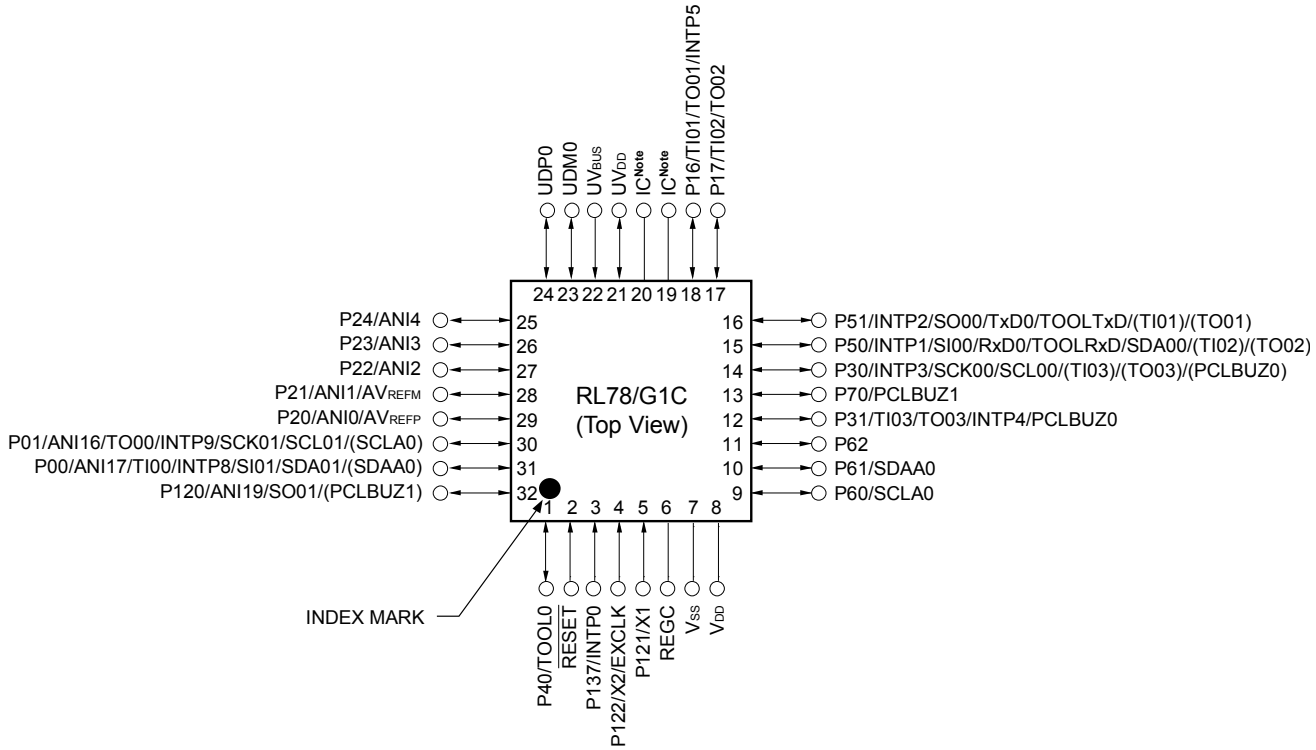


Note IC: Internal Connection Pin Leave open.

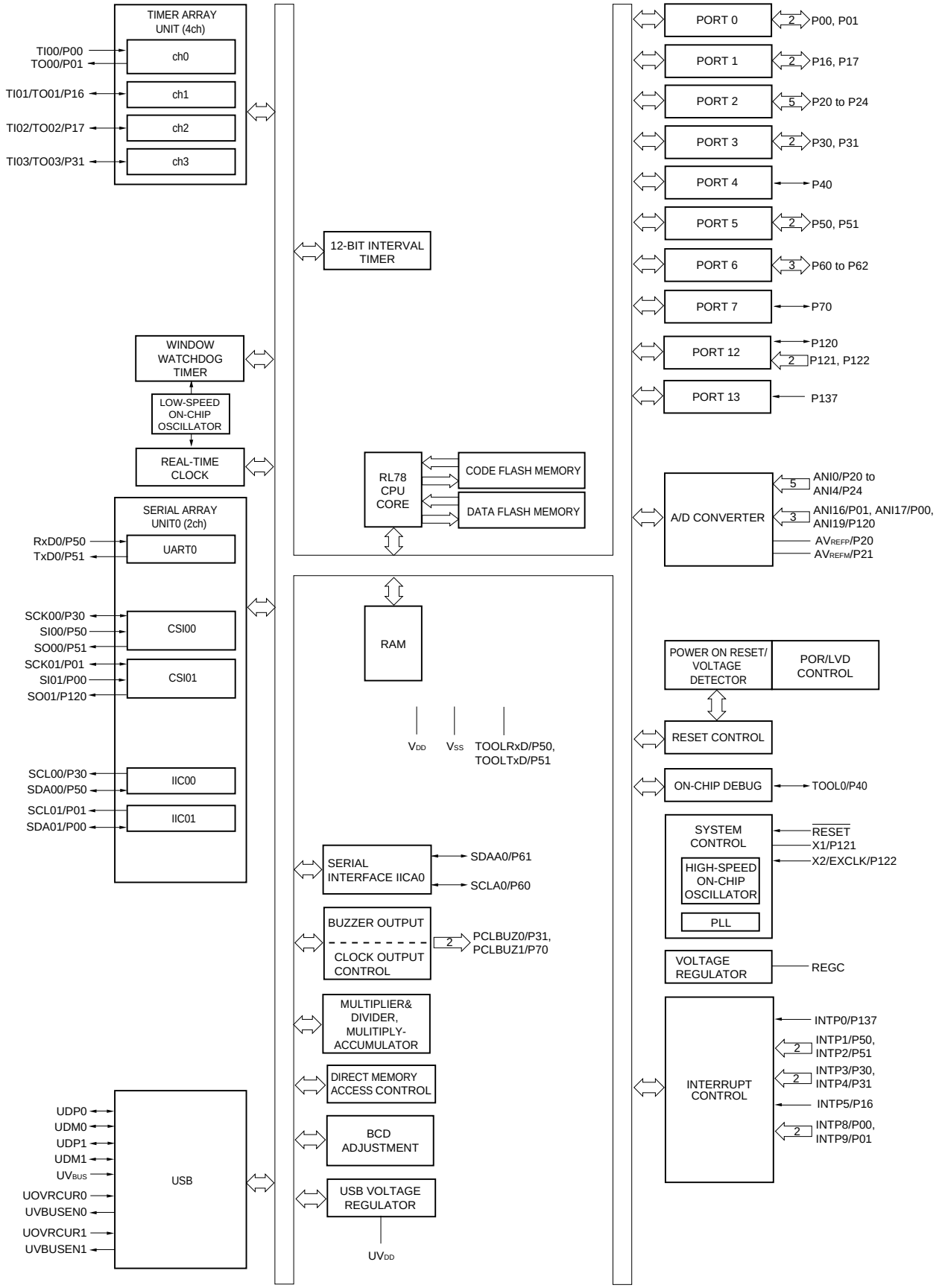
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5 Block Diagram

1.5.1 32-pin products



1.6 Outline of Functions

[32-pin, 48-pin products]

(1/2)

Item		32-pin		48-pin	
		R5F10JBC	R5F10KBC	R5F10JGC	R5F10KGC
Code flash memory (KB)		32 KB		32 KB	
Data flash memory (KB)		2 KB		2 KB	
RAM (KB)		5.5 KB Note 1		5.5 KB Note 1	
Memory space		1 MB			
<R> Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)			
	High-speed on-chip oscillator	1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)			
	PLL clock	6, 12, 24 MHz Note 2 : V_{DD} = 2.4 to 5.5 V			
Subsystem clock		–		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 2.4 to 5.5 V	
Low-speed on-chip oscillator		On-chip oscillation (Watchdog timer/Real-time clock/12-bit interval timer clock) 15 kHz (TYP.): V_{DD} = 2.4 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator: f_{HOCO} = 48 MHz /f_{IH} = 24 MHz operation)			
		0.04167 μs (PLL clock: f_{PLL} = 48 MHz /f_{IH} = 24 MHz Note 2 operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	22		38	
	CMOS I/O	16 (N-ch O.D. I/O [V_{DD} withstand voltage]: 5)		28 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)	
	CMOS input	3		5	
	CMOS output	–		1	
	N-ch open-drain I/O (6 V tolerance)	3		4	
Timer	16-bit timer	4 channel			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel Note 3			
	12-bit Interval timer (IT)	1 channel			
	Timer output	4 channels (PWM output: 3) Note 4			
	RTC output	–		1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

Notes 1. In the case of the 5.5 KB, this is about 4.5 KB when the self-programming function is used.

2. In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.

3. In 32-pin products, this channel can only be used for the constant-period interrupt function based on the low-speed on-chip oscillator clock (f_{IL}).

4. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4 V ≤ V_{DD} ≤ 5.5 V			–10.0 [Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–55.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P70 to P75 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–19.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])	2.4 V ≤ V_{DD} ≤ 5.5 V			–135.0	mA
	I_{OH2}	Per pin for P20 to P27	2.4 V ≤ V_{DD} ≤ 5.5 V			–0.1 [Note 2]	mA
		Total of all pins (When duty ≤ 70% [Note 3])	2.4 V ≤ V_{DD} ≤ 5.5 V			–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Per pin for P60 to P63	2.4V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4V ≤ V_{DD} ≤ 5.5 V			150.0	mA
	I_{OL2}	Per pin for P20 to P27	2.4V ≤ V_{DD} ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

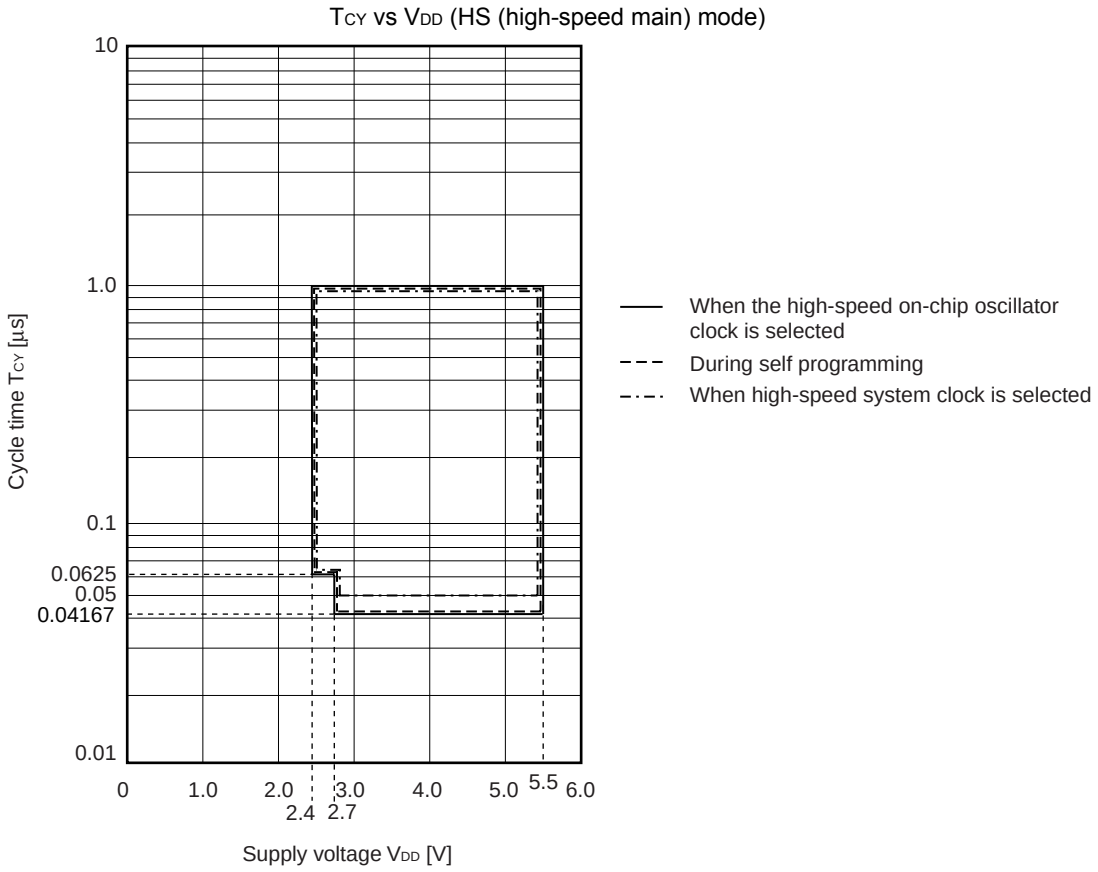
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

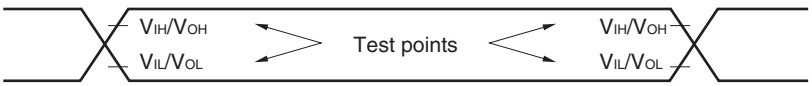
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 9	f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.67	1.25	mA
					V_{DD} = 3.0 V		0.67	1.25	mA
				f_{HOCO} = 24 MHz Note 7, f_{IH} = 12 MHz Note 4	V_{DD} = 5.0 V		0.50	0.86	mA
					V_{DD} = 3.0 V		0.50	0.86	mA
				f_{HOCO} = 12 MHz Note 7, f_{IH} = 6 MHz Note 4	V_{DD} = 5.0 V		0.41	0.67	mA
					V_{DD} = 3.0 V		0.41	0.67	mA
				f_{HOCO} = 6 MHz Note 7, f_{IH} = 3 MHz Note 4	V_{DD} = 5.0 V		0.37	0.58	mA
					V_{DD} = 3.0 V		0.37	0.58	mA
			HS (High-speed main) mode Note 9	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			HS (High-speed main) mode (PLL operation) Note 9	f_{PLL} = 48 MHz, f_{CLK} = 24 MHz Note 3	V_{DD} = 5.0 V		0.91	1.52	mA
					V_{DD} = 3.0 V		0.91	1.52	mA
				f_{PLL} = 48 MHz, f_{CLK} = 12 MHz Note 3	V_{DD} = 5.0 V		0.85	1.28	mA
					V_{DD} = 3.0 V		0.85	1.28	mA
				f_{PLL} = 48 MHz, f_{CLK} = 6 MHz Note 3	V_{DD} = 5.0 V		0.82	1.15	mA
					V_{DD} = 3.0 V		0.82	1.15	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = –40°C	Square wave input		0.25	0.57	µA
					Resonator connection		0.44	0.76	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.30	0.57	µA
					Resonator connection		0.49	0.76	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.33	1.17	µA
					Resonator connection		0.63	1.36	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.46	1.97	µA
					Resonator connection		0.76	2.16	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		0.97	3.37	µA
					Resonator connection		1.16	3.56	µA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.18	0.50	µA
			T_A = +25°C				0.23	0.50	µA
			T_A = +50°C				0.26	1.10	µA
			T_A = +70°C				0.29	1.90	µA
			T_A = +85°C				0.90	3.30	µA

(**Notes** and **Remarks** are listed on the next page.)

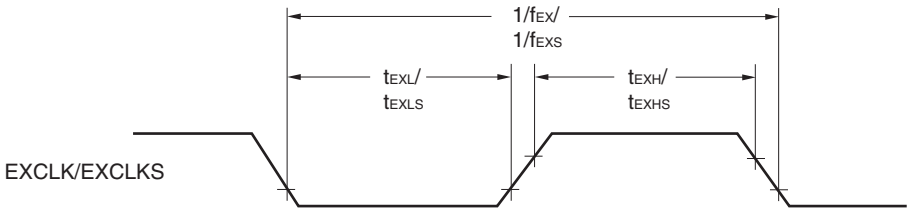
Minimum Instruction Execution Time during Main System Clock Operation



AC Timing Test Points



External System Clock Timing



2.5 Peripheral Functions Characteristics

2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note			4.0	Mbps

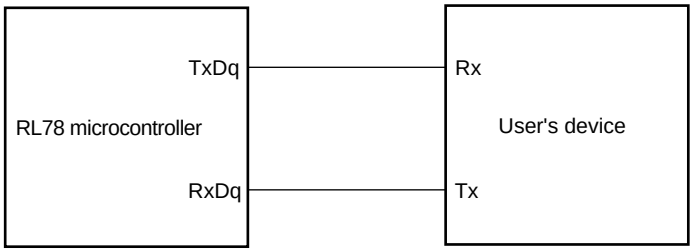
Note The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

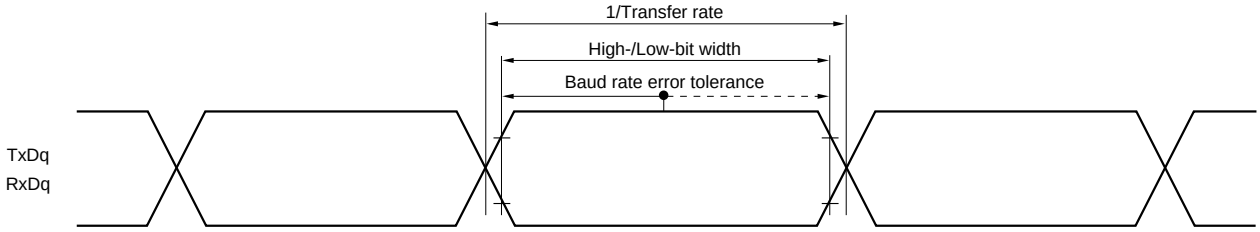
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 5)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200			ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300			ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2 - 50$			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2 - 120$			ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2 - 7$			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2 - 10$			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121			ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10			ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ				60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ				130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		23			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33			ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10			ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ				10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ				10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Caution** and **Remark** are listed on the next page.)

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00)

4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300			ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500			ns
			2.4 V ≤ V_{DD} < 3.3 V, 2.4 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150			ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458			ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50			ns

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. Use it with $V_{DD} \geq V_b$.

(**Remarks** are listed two pages after the next page.)

(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0 to ANI7, ANI16, ANI17, ANI19

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		Bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time		t_{LD}				300	μs

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V_{DD} ≤ 5.5 V			8.5 Note 2	mA
		Per pin for P60 to P63	2.4V ≤ V_{DD} ≤ 5.5 V			15.0 Note 2	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4V ≤ V_{DD} ≤ 5.5 V			80.0	mA
	I_{OL2}	Per pin for P20 to P27	2.4V ≤ V_{DD} ≤ 5.5 V			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P137, P140, $\overline{\text{RESET}}$	$V_I = V_{DD}$				1	μA
	I_{LIH2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P137, P140, $\overline{\text{RESET}}$	$V_I = V_{SS}$				–1	μA
	I_{LIL2}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_I = V_{SS}$	In input port or external clock input			–1	μA
				In resonator connection			–10	μA
On-chip pll-up resistance	R_U	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140	$V_I = V_{SS}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 9	f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.67	2.25	mA
					V_{DD} = 3.0 V		0.67	2.25	mA
				f_{HOCO} = 24 MHz Note 7, f_{IH} = 12 MHz Note 4	V_{DD} = 5.0 V		0.50	1.55	mA
					V_{DD} = 3.0 V		0.50	1.55	mA
				f_{HOCO} = 12 MHz Note 7, f_{IH} = 6 MHz Note 4	V_{DD} = 5.0 V		0.41	1.21	mA
					V_{DD} = 3.0 V		0.41	1.21	mA
				f_{HOCO} = 6 MHz Note 7, f_{IH} = 3 MHz Note 4	V_{DD} = 5.0 V		0.37	1.05	mA
					V_{DD} = 3.0 V		0.37	1.05	mA
			HS (High-speed main) mode Note 9	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
			HS (High-speed main) mode (PLL operation) Note 9	f_{PLL} = 48 MHz, f_{CLK} = 24 MHz Note 3	V_{DD} = 5.0 V		0.91	2.74	mA
					V_{DD} = 3.0 V		0.91	2.74	mA
				f_{PLL} = 48 MHz, f_{CLK} = 12 MHz Note 3	V_{DD} = 5.0 V		0.85	2.31	mA
					V_{DD} = 3.0 V		0.85	2.31	mA
				f_{PLL} = 48 MHz, f_{CLK} = 6 MHz Note 3	V_{DD} = 5.0 V		0.82	2.07	mA
					V_{DD} = 3.0 V		0.82	2.07	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = –40°C	Square wave input		0.25	0.57	µA
					Resonator connection		0.44	0.76	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.30	0.57	µA
					Resonator connection		0.49	0.76	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.33	1.17	µA
					Resonator connection		0.63	1.36	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.46	1.97	µA
					Resonator connection		0.76	2.16	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		0.97	3.37	µA
					Resonator connection		1.16	3.56	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +105°C	Square wave input		3.01	15.37	µA
					Resonator connection		3.20	15.56	µA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.18	0.50	µA
			T_A = +25°C				0.23	0.50	µA
			T_A = +50°C				0.26	1.10	µA
			T_A = +70°C				0.29	1.90	µA
			T_A = +85°C				0.90	3.30	µA
			T_A = +105°C				2.94	15.30	µA

(**Notes** and **Remarks** are listed on the next page.)

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
USB operating current	I_{USBH} **Note 11**	During USB communication operation under the following settings and conditions (V_{DD} = 5.0 V, T_A = +25°C): • The internal power supply for the USB is used. • X1 oscillation frequency (f_X) = 12 MHz, PLL oscillation frequency (f_{PLL}) = 48 MHz • The host controller (via two ports) is set to operate in full-speed mode with four pipes (end points) used simultaneously. (PIPE4: Bulk OUT transfer (64 bytes), PIPE5: Bulk IN transfer (64 bytes), PIPE6: Interrupt OUT transfer, PIPE7: Interrupt IN transfer). • The USB ports (two ports) are individually connected to a peripheral function via a 0.5 m USB cable.		9.0		mA
	I_{USBF} **Note 11**	During USB communication operation under the following settings and conditions (V_{DD} = 5.0 V, T_A = +25°C): • The internal power supply for the USB is used. • X1 oscillation frequency (f_X) = 12 MHz, PLL oscillation frequency (f_{PLL}) = 48 MHz • The function controller is set to operate in full-speed mode with four pipes (end points) used simultaneously. (PIPE4: Bulk OUT transfer (64 bytes), PIPE5: Bulk IN transfer (64 bytes), PIPE6: Interrupt OUT transfer, PIPE7: Interrupt IN transfer). • The USB port (one port) is connected to the host device via a 0.5 m USB cable.		2.5		mA
	I_{SUSP} **Note 12**	During suspended state under the following settings and conditions (V_{DD} = 5.0 V, T_A = +25°C): • The function controller is set to full-speed mode (the UDP0 pin is pulled up). • The internal power supply for the USB is used. • The system is set to STOP mode (When the high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When the watchdog timer is stopped.). • The USB port (one port) is connected to the host device via a 0.5 m USB cable.		240		μA

(**Notes** and **Remarks** are listed on the next page.)

(3) BC option standard (Host)

(T_A = –40 to +105°C, 4.75 V ≤ UV_{BUS} ≤ 5.25 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi output voltage (UV_{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{P20}		38	40	42	% UV_{BUS}
		1001	V_{P27}		51.6	53.6	55.6	% UV_{BUS}
		1010	V_{P20}		38	40	42	% UV_{BUS}
		1100	V_{P33}		60	66	72	% UV_{BUS}
UDMi output voltage (UV_{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{M20}		38	40	42	% UV_{BUS}
		1001	V_{M20}		38	40	42	% UV_{BUS}
		1010	V_{M27}		51.6	53.6	55.6	% UV_{BUS}
		1100	V_{M33}		60	66	72	% UV_{BUS}
UDPi comparing voltage Note 1 (UV_{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{HDETP_UP0}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETP_DWN0}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1001	V_{HDETP_UP1}	The rise of pin voltage detection voltage	60.5			% UV_{BUS}
			V_{HDETP_DWN1}	The fall of pin voltage detection voltage			45.0	% UV_{BUS}
		1010	V_{HDETP_UP2}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETP_DWN2}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
UDMi comparing voltage Note 1 (UV_{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{HDETM_UP0}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETM_DWN0}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1001	V_{HDETM_UP1}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETM_DWN1}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1010	V_{HDETM_UP2}	The rise of pin voltage detection voltage	60.5			% UV_{BUS}
			V_{HDETM_DWN2}	The fall of pin voltage detection voltage			45.0	% UV_{BUS}
UDPi pull-up detection Note 2 Connect detection with the full speed function (pull-up resistor)		1000 1001 1010	R_{HDET_PULL}	In full-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
UDMi pull-up detection Note 2 Connect detection with the low-speed (pull-up resistor)		1000 1001 1010	R_{HDET_PULL}	In low-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
UDMi sink current detection Note 2 Connect detection with the BC1.2 portable device (sink resistor)		1000 1001 1010	I_{HDET_SINK}		25			μA

Notes 1. If the voltage output from UDPi or UDMi (i = 0, 1) exceeds the range of the MAX and MIN values prescribed in this specification, DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

2. If the pull-up resistance or sink current prescribed in this specification is applied to UDPi or UDMi (i = 0, 1), DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

Remark i = 0, 1

(3) Reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), Reference voltage (–) = V_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI7, ANI16, ANI17, ANI19, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Notes 1, 2	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	tCONV	10-bit resolution Target ANI pin : ANI0 to ANI7, ANI16, ANI17, ANI19	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target ANI pin : Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI7, ANI16, ANI17, ANI19		0		V_{DD}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} Note 3			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} Note 3			V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0 to ANI7, ANI16, ANI17, ANI19

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		Bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

3.6.3 POR circuit characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock (f_{MAIN}) is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).