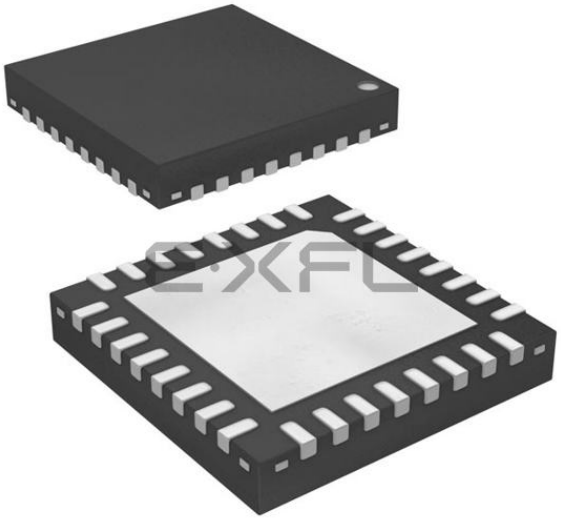
Renesas Electronics America Inc - R5F10KBCGNA#U0 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10kbcgna-u0

ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1C	
			32-pin	48-pin
32 KB	2 KB	5.5 KB Note	R5F10JBC, R5F10KBC	R5F10JGC, R5F10KGC

Note This is about 4.5 KB when the self-programming function is used.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Numbers

Pin count	Package	USB Function	Fields of Application Note	Part Number
32 pins	32-pin plastic HWQFN (5 × 5 , 0.5 mm pitch)	Host/Function controller	A	R5F10JBCANA#U0, R5F10JBCANA#W0
			G	R5F10JBCGNA#U0, R5F10JBCGNA#W0
		Function controller only	A	R5F10KBCANA#U0, R5F10KBCANA#W0
			G	R5F10KBCGNA#U0, R5F10KBCGNA#W0
	32-pin plastic LQFP (7 × 7 , 0.8 mm pitch)	Host/Function controller	A	R5F10JBCAFP#V0, R5F10JBCAFP#X0
			G	R5F10JBCGFP#V0, R5F10JBCGFP#X0
		Function controller only	A	R5F10KBCAFP#V0, R5F10KBCAFP#X0
			G	R5F10KBCGFP#V0, R5F10KBCGFP#X0
48 pins	48-pin plastic LFQFP (7 × 7 , 0.5 mm pitch)	Host/Function controller	A	R5F10JGCAFB#V0, R5F10JGCAFB#X0
			G	R5F10JGCGFB#V0, R5F10JGCGFB#X0
		Function controller only	A	R5F10KGCAFB#V0, R5F10KGCAFB#X0s
			G	R5F10JGCANA#U0, R5F10JGCANA#W0
	48-pin plastic HWQFN (7 × 7 , 0.5 mm pitch)	Host/Function controller	A	R5F10JGCANA#U0, R5F10JGCANA#W0
			G	R5F10JGCGNA#U0, R5F10JGCGNA#W0
		Function controller only	A	R5F10KGCANA#U0, R5F10KGCANA#W0
			G	R5F10KGCGNA#U0, R5F10KGCGNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G1C**.

Caution The part number above is valid as of when this manual was issued. For the latest part number, see the web page of the target product on the Renesas Electronics website.

1.6 Outline of Functions

[32-pin, 48-pin products]

(1/2)

Item		32-pin		48-pin	
		R5F10JBC	R5F10KBC	R5F10JGC	R5F10KGC
Code flash memory (KB)		32 KB		32 KB	
Data flash memory (KB)		2 KB		2 KB	
RAM (KB)		5.5 KB Note 1		5.5 KB Note 1	
Memory space		1 MB			
<R> Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)			
	High-speed on-chip oscillator	1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)			
	PLL clock	6, 12, 24 MHz Note 2 : V_{DD} = 2.4 to 5.5 V			
Subsystem clock		–		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 2.4 to 5.5 V	
Low-speed on-chip oscillator		On-chip oscillation (Watchdog timer/Real-time clock/12-bit interval timer clock) 15 kHz (TYP.): V_{DD} = 2.4 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator: f_{HOCO} = 48 MHz /f_{IH} = 24 MHz operation)			
		0.04167 μs (PLL clock: f_{PLL} = 48 MHz /f_{IH} = 24 MHz Note 2 operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	22		38	
	CMOS I/O	16 (N-ch O.D. I/O [V_{DD} withstand voltage]: 5)		28 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)	
	CMOS input	3		5	
	CMOS output	–		1	
	N-ch open-drain I/O (6 V tolerance)	3		4	
Timer	16-bit timer	4 channel			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel Note 3			
	12-bit Interval timer (IT)	1 channel			
	Timer output	4 channels (PWM output: 3) Note 4			
	RTC output	–		1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

Notes 1. In the case of the 5.5 KB, this is about 4.5 KB when the self-programming function is used.

2. In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.

3. In 32-pin products, this channel can only be used for the constant-period interrupt function based on the low-speed on-chip oscillator clock (f_{IL}).

4. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Per pin for P60 to P63	2.4V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4V ≤ V_{DD} ≤ 5.5 V			150.0	mA
	I_{OL2}	Per pin for P20 to P27	2.4V ≤ V_{DD} ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (High-speed main) mode Note 6	f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 3	Basic operation	V_{DD} = 5.0 V		1.7		mA
						V_{DD} = 3.0 V		1.7		mA
					Normal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	mA
				f_{HOCO} = 24 MHz Note 5, f_{IH} = 12 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.3	3.2	mA
						V_{DD} = 3.0 V		2.3	3.2	mA
				f_{HOCO} = 12 MHz Note 5, f_{IH} = 6 MHz Note 3	Normal operation	V_{DD} = 5.0 V		1.6	2.0	mA
						V_{DD} = 3.0 V		1.6	2.0	mA
				f_{HOCO} = 6 MHz Note 5, f_{IH} = 3 MHz Note 3	Normal operation	V_{DD} = 5.0 V		1.2	1.5	mA
						V_{DD} = 3.0 V		1.2	1.5	mA
			HS (High-speed main) mode Note 6	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			HS (High-speed main) mode (PLL operation) Note 6	f_{PLL} = 48 MHz, f_{CLK} = 24 MHz Note 2	Normal operation	V_{DD} = 5.0 V		4.0	5.9	mA
						V_{DD} = 3.0 V		4.0	5.9	mA
				f_{PLL} = 48 MHz, f_{CLK} = 12 MHz Note 2	Normal operation	V_{DD} = 5.0 V		2.6	3.6	mA
						V_{DD} = 3.0 V		2.6	3.6	mA
				f_{PLL} = 48 MHz, f_{CLK} = 6 MHz Note 2	Normal operation	V_{DD} = 5.0 V		1.9	2.4	mA
						V_{DD} = 3.0 V		1.9	2.4	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4, T_A = –40°C	Normal operation	Resonator connection		4.1	4.9	μA
						Square wave input		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +70°C	Normal operation	Square wave input		4.2	6.3	μA
						Resonator connection		4.3	6.4	μA
				f_{SUB} = 32.768 kHz Note 4, T_A = +85°C	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	μA

(**Notes** and **Remarks** are listed on the next page.)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.00	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.00	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.50	1.06	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	1.62	mA
		CSI operation			0.70	0.84	mA

(**Notes** and **Remarks** are listed on the next page.)

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	167			ns
			2.4 V ≤ V_{DD} ≤ 5.5 V	250			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 12			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 18			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2 – 38			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V		44			ns
		2.7 V ≤ V_{DD} ≤ 5.5 V		44			ns
		2.4 V ≤ V_{DD} ≤ 5.5 V		75			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4				25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01), m: Unit number (m = 0), n: Channel number (n = 0, 1), g: PIM and POM numbers (g = 0, 3, 5, 7)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01))

Notes 6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V ≤ V_{DD} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

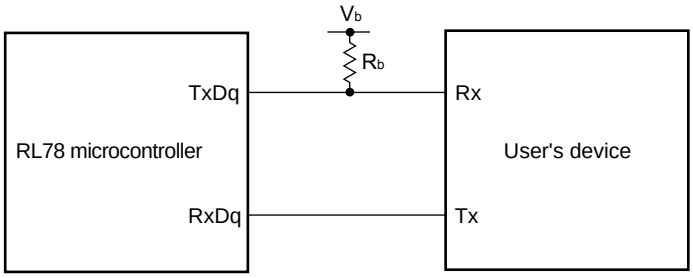
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

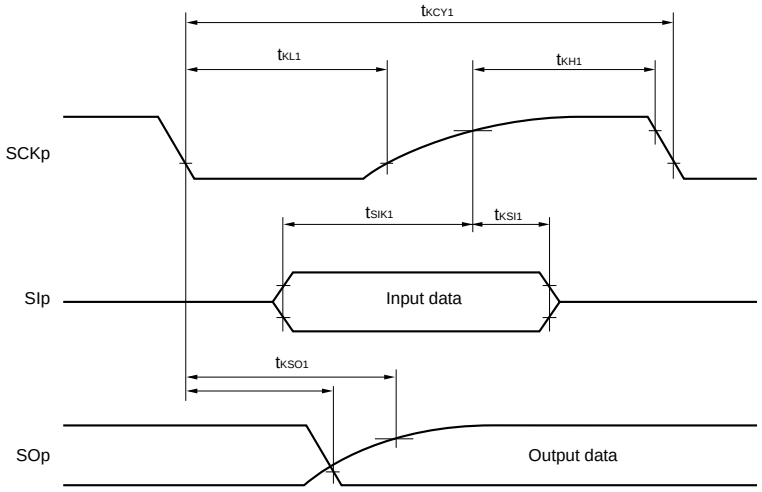
7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

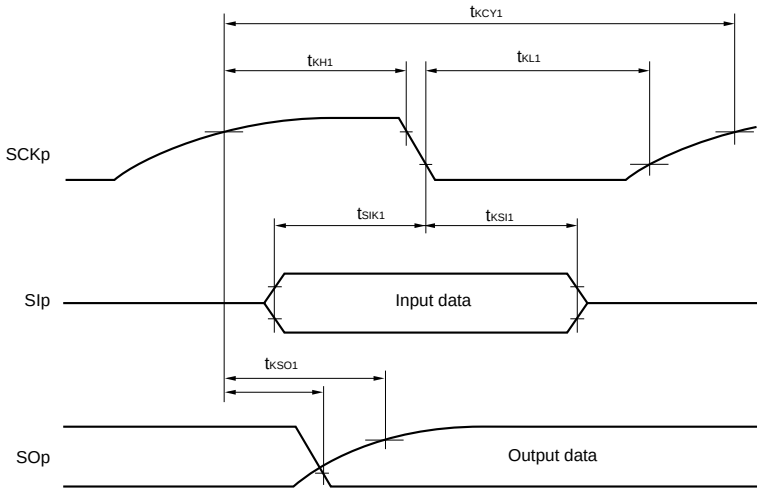
UART mode connection diagram (during communication at different potential)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00), m: Unit number, n: Channel number (mn = 00), g: PIM and POM number (g = 0, 3, 5, 7)

2. CSI01 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 – 50			ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		1/f_{MCK} + 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		1/f_{MCK} + 20			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 214	ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ				2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with V_{DD} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Caution** and **Remarks** are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (–) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (–) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (–) = AV_{REFM}
ANI0 to ANI7	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16, ANI17, ANI19	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		–

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI2 to ANI7, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI7	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	EZS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	EFS	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.25	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV_{REFP} = V_{DD} [Note 3]	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI7		0		AV_{REFP}	V
		Internal reference voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR} [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25} [Note 4]			V

(**Notes** are listed on the next page.)

3.2.3 PLL oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency Note	f_{PLLIN}	High-speed system clock	6.00		16.00	MHz
PLL output frequency Note	f_{PLL}			48.00		MHz
Lock up time		From PLL output enable to stabilization of the output frequency	40.00			μs
Interval time		From PLL stop to PLL re-operation setteing Wait time	4.00			μs
Setting wait time		From after PLL input clock stabilization and PLL setting is fixed to start setting Wait time required	1.00			μs

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4 V ≤ V_{DD} ≤ 5.5 V			–3.0 [Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P70 to P75 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–30.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–19.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])	2.4 V ≤ V_{DD} ≤ 5.5 V			-60.0	mA
	I_{OH2}	Per pin for P20 to P27	2.4 V ≤ V_{DD} ≤ 5.5 V			–0.1 [Note 2]	mA
		Total of all pins (When duty ≤ 70% [Note 3])	2.4 V ≤ V_{DD} ≤ 5.5 V			–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V_{DD} ≤ 5.5 V			8.5 Note 2	mA
		Per pin for P60 to P63	2.4V ≤ V_{DD} ≤ 5.5 V			15.0 Note 2	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			40.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4V ≤ V_{DD} ≤ 5.5 V			80.0	mA
	I_{OL2}	Per pin for P20 to P27	2.4V ≤ V_{DD} ≤ 5.5 V			0.4 Note 2	mA
		Total of all pins (When duty ≤ 70% Note 3)	2.4V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (1/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		1.3	1.8	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.8	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self-programming operating current	I_{FSP} Notes 1, 9				2.00	12.30	mA
BGO operating current	I_{BGO} Notes 1, 8				2.00	12.30	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed Note 10		0.80	1.97	mA
			The A/D conversion operations are performed, Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		1.20	3.00	mA
		CSI operation			0.70	1.56	mA

(**Notes** and **Remarks** are listed on the next page.)

3.5 Peripheral Functions Characteristics

3.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

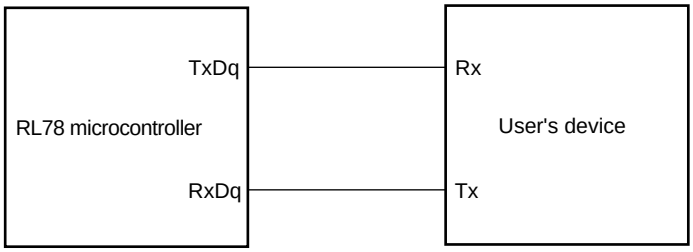
(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/12	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note			2.0	Mbps

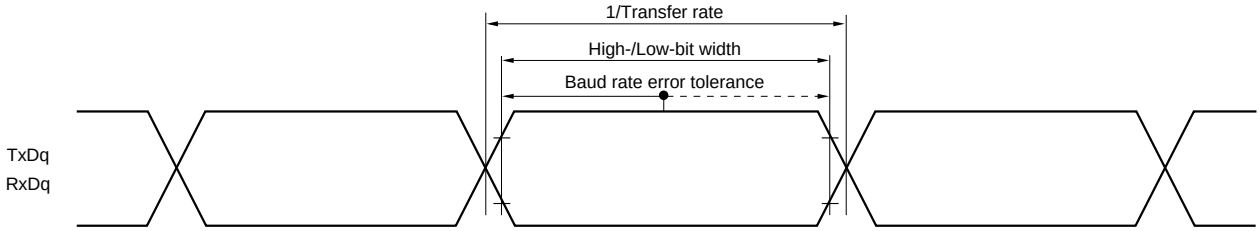
Note The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:
HS (high-speed main) mode: 24 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)
16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0), g: PIM and POM number (g = 5)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(4) BC option standard (Function)

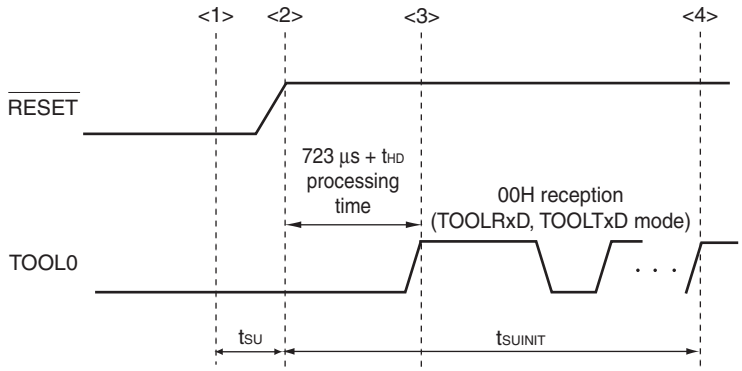
(T_A = –40 to +105°C, 4.35 V ≤ UV_{BUS} ≤ 5.25 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi input reference voltage (UV_{BUS} divider ratio) • VDOUEi = 0 (i = 0))	VDSELi [3:0] (i = 0)	0000	V_{DDET0}		27	32	37	% UV_{BUS}
		0001	V_{DDET1}		29	34	39	% UV_{BUS}
		0010	V_{DDET2}		32	37	42	% UV_{BUS}
		0011	V_{DDET3}		35	40	45	% UV_{BUS}
		0100	V_{DDET4}		38	43	48	% UV_{BUS}
		0101	V_{DDET5}		41	46	51	% UV_{BUS}
		0110	V_{DDET6}		44	49	54	% UV_{BUS}
		0111	V_{DDET7}		47	52	57	% UV_{BUS}
		1000	V_{DDET8}		51	56	61	% UV_{BUS}
		1001	V_{DDET9}		55	60	65	% UV_{BUS}
		1010	V_{DDET10}		59	64	69	% UV_{BUS}
		1011	V_{DDET11}		63	68	73	% UV_{BUS}
		1100	V_{DDET12}		67	72	77	% UV_{BUS}
		1101	V_{DDET13}		71	76	81	% UV_{BUS}
		1110	V_{DDET14}		75	80	85	% UV_{BUS}
		1111	V_{DDET15}		79	84	89	% UV_{BUS}

3.10 Timing Specs for Switching Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

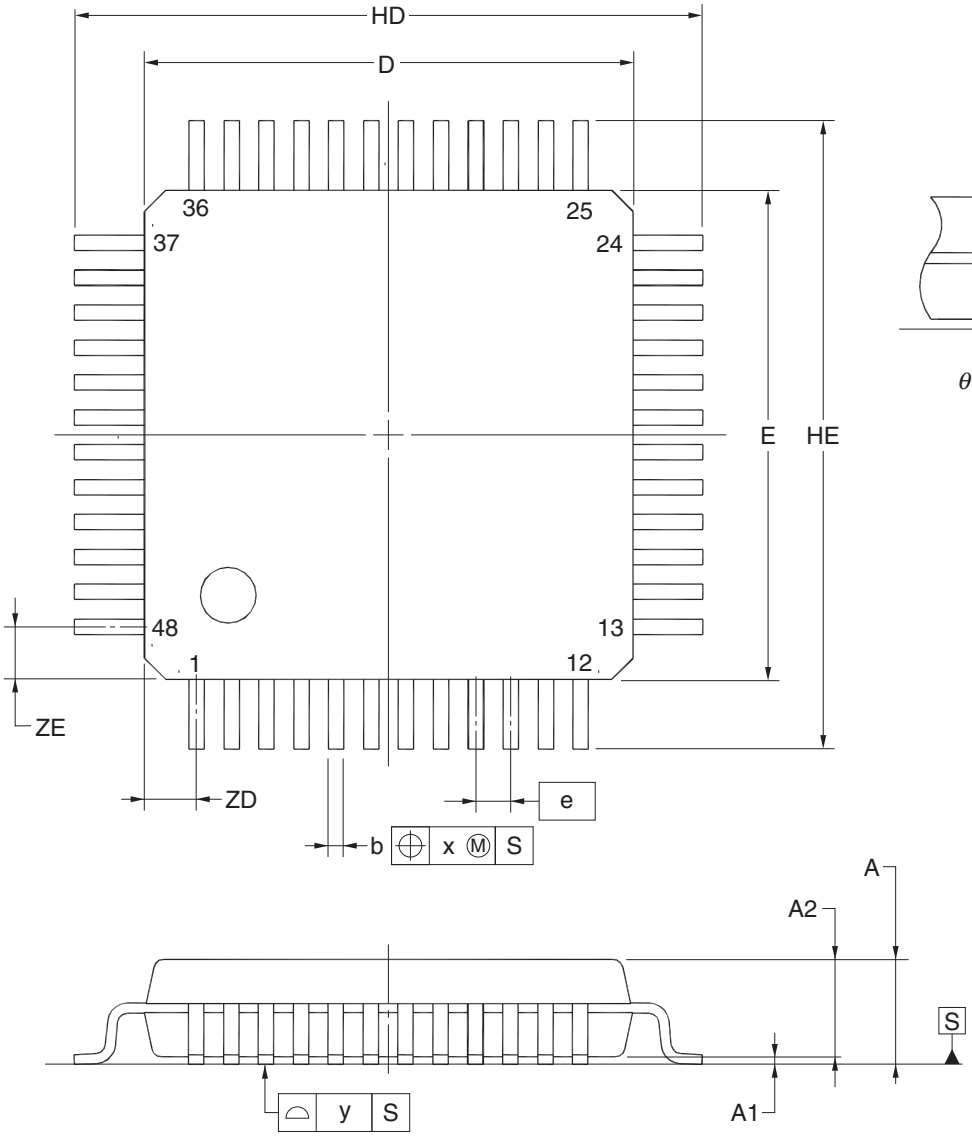
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends

t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end (excluding the processing time of the firmware to control the flash memory)

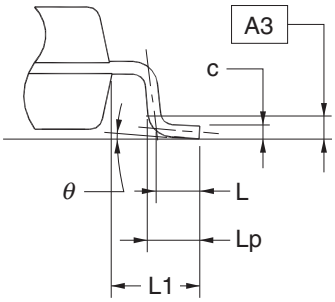
4.2 48-pin Products

R5F10JGCAFB, R5F10KGCAFB
R5F10JGCGFB, R5F10KGCGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

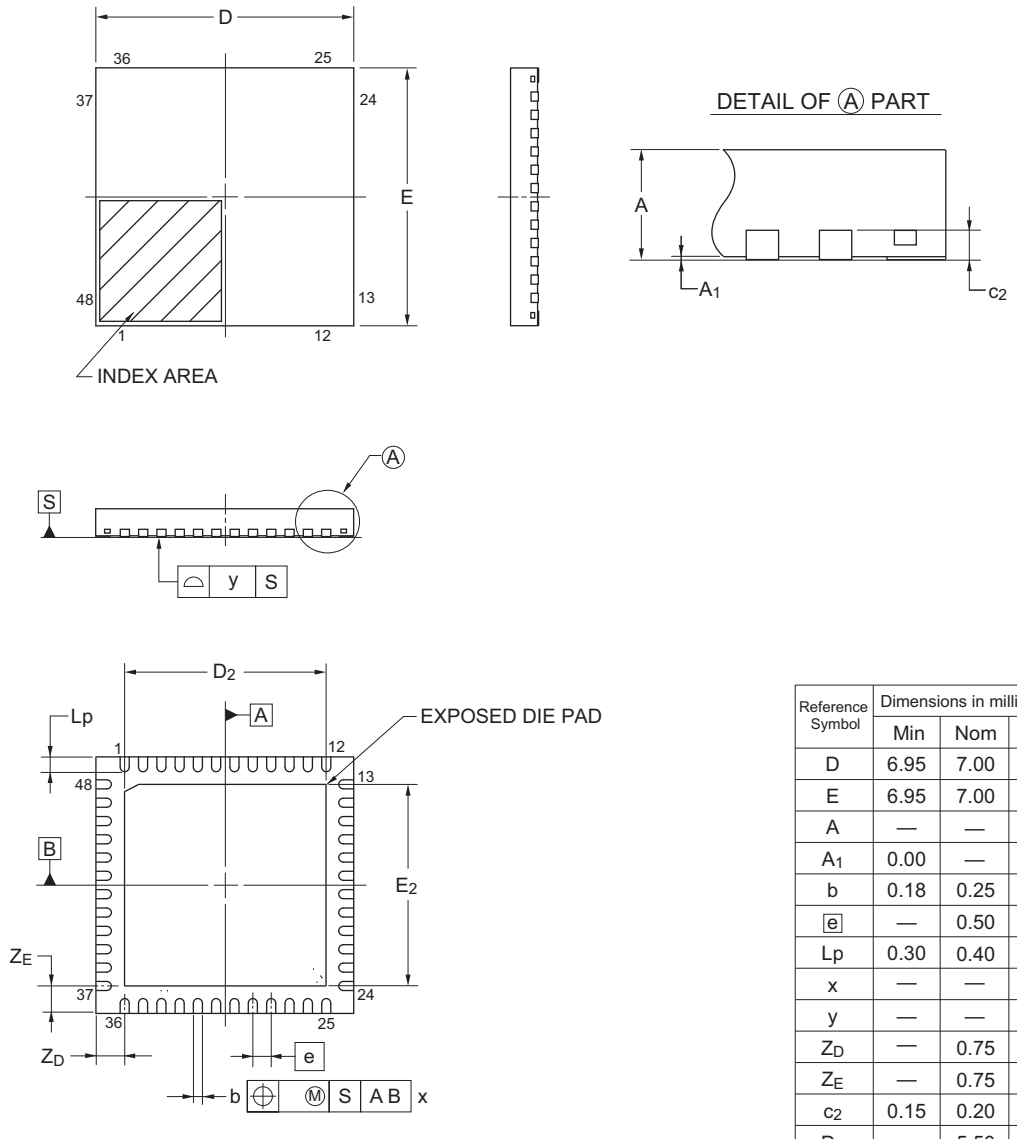
NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10JGCANA, R5F10KGCANA
R5F10JGCGNA, R5F10KGCGNA

<R>

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-7	0.13

Unit: mm



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

Revision History	RL78/G1A Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Sep 20, 2012	-	First Edition issued
1.00	Aug 08, 2013	Throughout	Deletion of the bar over SCK and SCKxx
			Renaming of f_{EXT} to f_{EXS}
			Renaming of interval timer (unit) to 12-bit interval timer
			Addition of products for G: Industrial applications (T_A = -40 to +105 °C)
		1	Change of **1.1 Features**
		2	Change of **1.2 List of Part Numbers**
		3	Modification of **Figure 1-1. Part Number, Memory Size, and Package of RL78/G1C**
		4, 5	Addition of remark to **1.3 Pin Configuration (Top View)**
		15, 16	Change of **1.6 Outline of Functions**
		17 to 76	Addition of a whole chapter
		77 to 131	Addition of a whole chapter
		132	Addition of products for G: Industrial applications (T_A = -40 to +105 °C)
1.10	Nov 15, 2013	77	Caution 3 added.
		79	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
1.20	Sep 30, 2016	4 to 7	Modification of pin configuration in **1.3.1 32-pin products**
		8 to 11	Modification of pin configuration in **1.3.2 48-pin products**
		15	Modification of description of main system clock in **1.6 Outline of Functions**
		74	Modification of title of **2.7 RAM Data Retention Characteristics** and figure
		74	Modification of table of **2.8 Flash Memory Programming Characteristics**
		129	Modification of title of **3.7 RAM Data Retention Characteristics** and figure
		129	Modification of table of **3.8 Flash Memory Programming Characteristics** and addition of **Note 4**
		132	Change of figure in **4.1 32-pin Products**
		134	Change of figure in **4.2 48-pin Products**

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