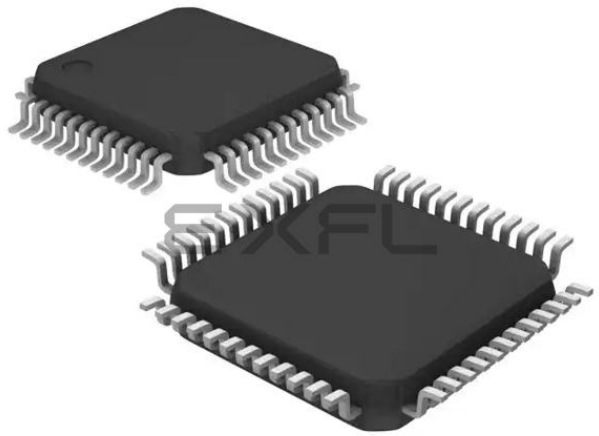
Renesas Electronics America Inc - R5F10KGCAFB#V0 Datasheet



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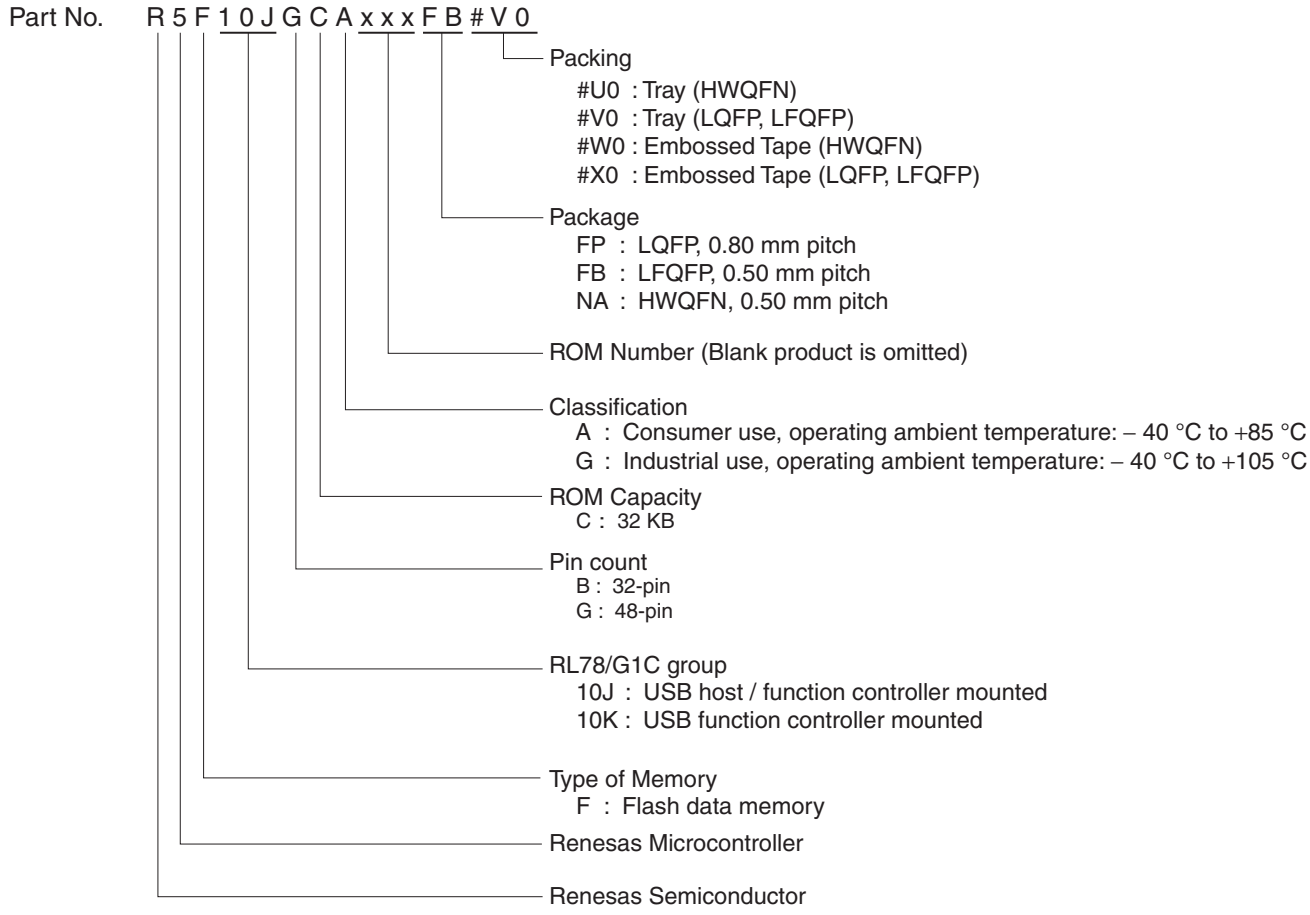
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

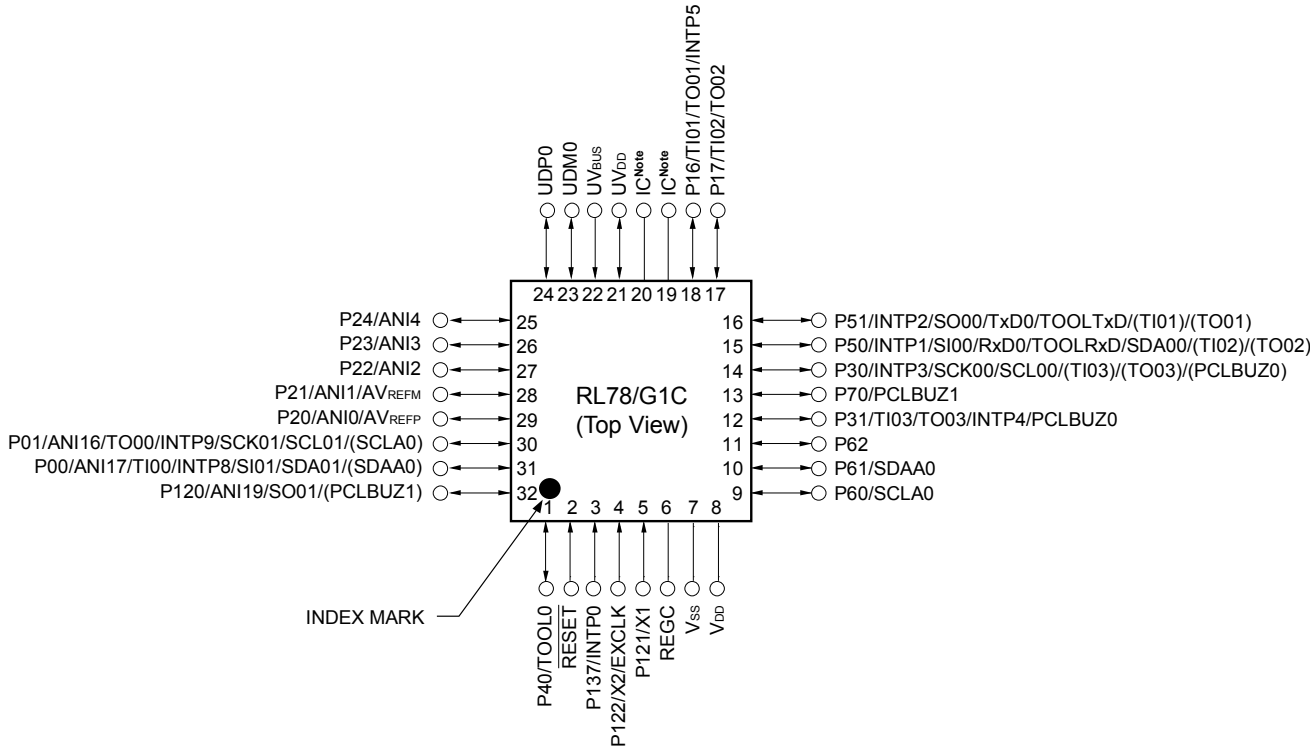
Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	5.5K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f10kgcafb-v0

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1C



(2) USB function: Function controller only (R5F10KBC)

<R>



Note IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

2. ELECTRICAL SPECIFICATIONS (A: T_A = -40 to +85°C)

This chapter describes the electrical specifications for the products "A: Consumer applications (T_A = -40 to +85°C)".

The target products A: Consumer applications ; T_A = -40 to +85°C
R5F10JBCANA, R5F10JBCAFP, R5F10JGCANA, R5F10JGCAFB,
R5F10KBCANA, R5F10KBCAFP, R5F10KGCANA, R5F10KGCAFB
G: Industrial applications ; when using T_A = -40 to +105°C specification products at T_A = -40 to +85°C.
R5F10JBCGNA, R5F10JBCGFP, R5F10JGCGNA, R5F10JGCGFB,
R5F10KBCGNA, R5F10KBCGFP, R5F10KGCGNA, R5F10KGCGFB

Cautions 1. The RL78 microcontrollers has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted depend on the product.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)Note	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f_{XT})Note	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

2.2.2 On-chip oscillator characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f_{HOCO}		1		48	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	–1.0		+1.0	%
		–40 to –20 °C	–1.5		+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.2.3 PLL oscillator characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
PLL input frequency Note	f_{PLLIN}	High-speed system clock	6.00		16.00	MHz
PLL output frequency Note	f_{PLL}			48.00		MHz
Lock up time		From PLL output enable to stabilization of the output frequency	40.00			μs
Interval time		From PLL stop to PLL re-operation setteing Wait time	4.00			μs
Setting wait time		From after PLL input clock stabilization and PLL setting is fixed to start setting Wait time required	1.00			μs

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4 V ≤ V_{DD} ≤ 5.5 V			–10.0 [Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–55.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–10.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			–5.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P70 to P75 (When duty ≤ 70% [Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			–80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			–19.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			–10.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])	2.4 V ≤ V_{DD} ≤ 5.5 V			–135.0	mA
	I_{OH2}	Per pin for P20 to P27	2.4 V ≤ V_{DD} ≤ 5.5 V			–0.1 [Note 2]	mA
		Total of all pins (When duty ≤ 70% [Note 3])	2.4 V ≤ V_{DD} ≤ 5.5 V			–1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = –10.0 mA

Total output current of pins = (–10.0 × 0.7)/(80 × 0.01) ≅ –8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	2.4V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Per pin for P60 to P63	2.4V ≤ V_{DD} ≤ 5.5 V			20.0[Note 2]	mA
		Total of P00, P01, P40, P41, P120, P130, P140 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			70.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			15.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			9.0	mA
		Total of P14 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75 (When duty ≤ 70%[Note 3])	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			35.0	mA
			2.4 V ≤ V_{DD} < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4V ≤ V_{DD} ≤ 5.5 V			150.0	mA
	I_{OL2}	Per pin for P20 to P27	2.4V ≤ V_{DD} ≤ 5.5 V			0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2.4V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty ratio to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –10.0 mA	V_{DD} – 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –3.0 mA	V_{DD} – 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –2.0 mA	V_{DD} – 0.6			V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.5 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P14 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V

Caution P00, P01, P30, and P74 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. When Operating frequency setting of option byte = 48 MHz. When f_{HOCO} is divided by HOCODIV. When RDIV[1:0] = 00 (divided by 2: default).

6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

Remarks 1. f_{HOCO}: High-speed on-chip oscillator clock frequency (Max. 48 MHz)

2. f_{IH}: Main system clock source frequency obtained by dividing the high-speed on-chip oscillator clock by 2, 4, or 8 (Max. 24 MHz)

3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

4. f_{PLL}: PLL oscillation frequency

5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

6. f_{CLK}: CPU/peripheral hardware clock frequency

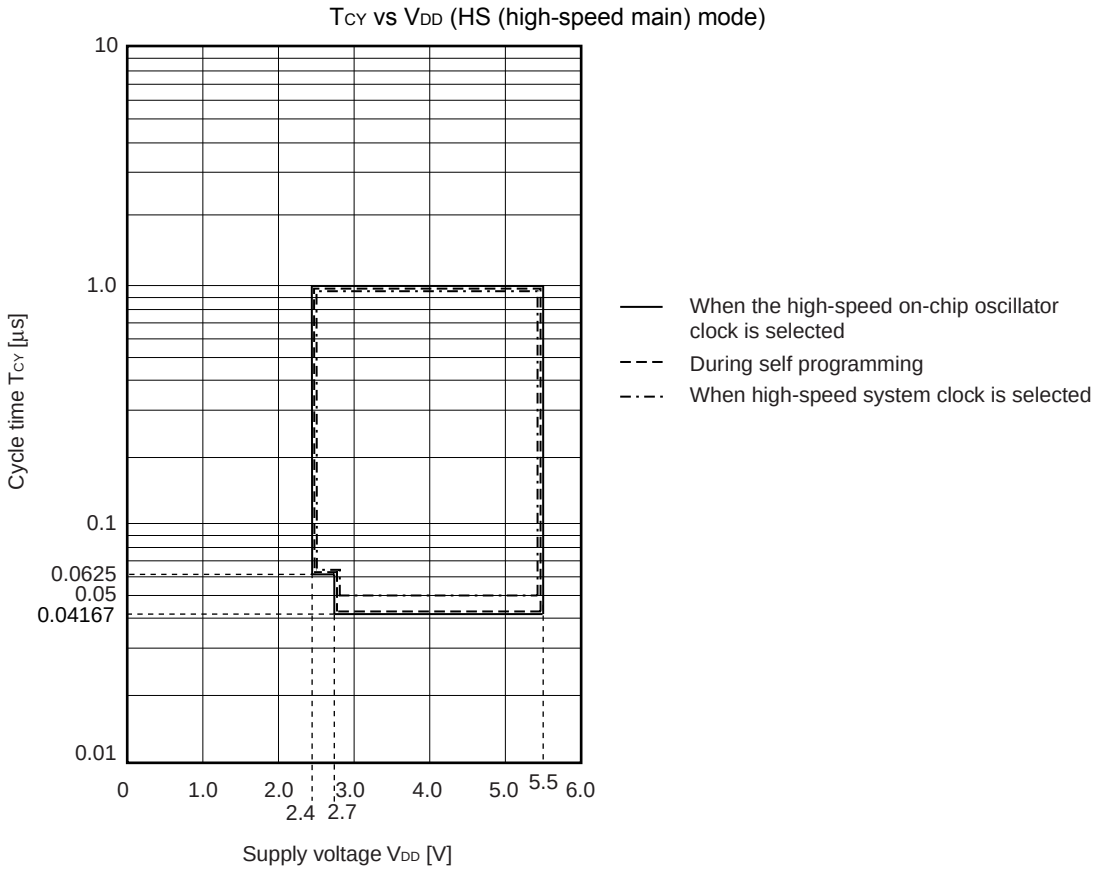
7. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C.

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) (2/2)

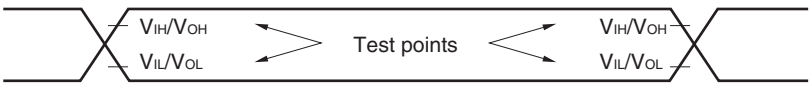
Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (High-speed main) mode Note 9	f_{HOCO} = 48 MHz, f_{IH} = 24 MHz Note 4	V_{DD} = 5.0 V		0.67	1.25	mA
					V_{DD} = 3.0 V		0.67	1.25	mA
				f_{HOCO} = 24 MHz Note 7, f_{IH} = 12 MHz Note 4	V_{DD} = 5.0 V		0.50	0.86	mA
					V_{DD} = 3.0 V		0.50	0.86	mA
				f_{HOCO} = 12 MHz Note 7, f_{IH} = 6 MHz Note 4	V_{DD} = 5.0 V		0.41	0.67	mA
					V_{DD} = 3.0 V		0.41	0.67	mA
				f_{HOCO} = 6 MHz Note 7, f_{IH} = 3 MHz Note 4	V_{DD} = 5.0 V		0.37	0.58	mA
					V_{DD} = 3.0 V		0.37	0.58	mA
			HS (High-speed main) mode Note 9	f_{MX} = 20 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			HS (High-speed main) mode (PLL operation) Note 9	f_{PLL} = 48 MHz, f_{CLK} = 24 MHz Note 3	V_{DD} = 5.0 V		0.91	1.52	mA
					V_{DD} = 3.0 V		0.91	1.52	mA
				f_{PLL} = 48 MHz, f_{CLK} = 12 MHz Note 3	V_{DD} = 5.0 V		0.85	1.28	mA
					V_{DD} = 3.0 V		0.85	1.28	mA
				f_{PLL} = 48 MHz, f_{CLK} = 6 MHz Note 3	V_{DD} = 5.0 V		0.82	1.15	mA
					V_{DD} = 3.0 V		0.82	1.15	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = –40°C	Square wave input		0.25	0.57	µA
					Resonator connection		0.44	0.76	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.30	0.57	µA
					Resonator connection		0.49	0.76	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		0.33	1.17	µA
					Resonator connection		0.63	1.36	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		0.46	1.97	µA
					Resonator connection		0.76	2.16	µA
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		0.97	3.37	µA
					Resonator connection		1.16	3.56	µA
	I_{DD3} Note 6	STOP mode Note 8	T_A = –40°C				0.18	0.50	µA
			T_A = +25°C				0.23	0.50	µA
			T_A = +50°C				0.26	1.10	µA
			T_A = +70°C				0.29	1.90	µA
			T_A = +85°C				0.90	3.30	µA

(**Notes** and **Remarks** are listed on the next page.)

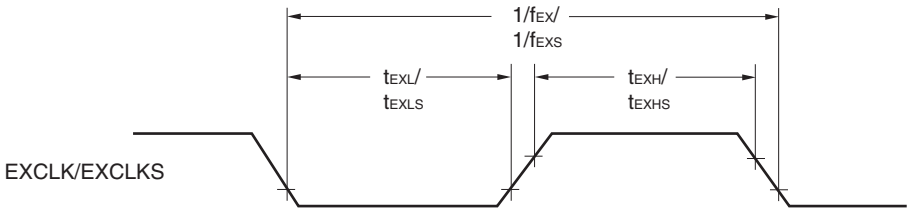
Minimum Instruction Execution Time during Main System Clock Operation



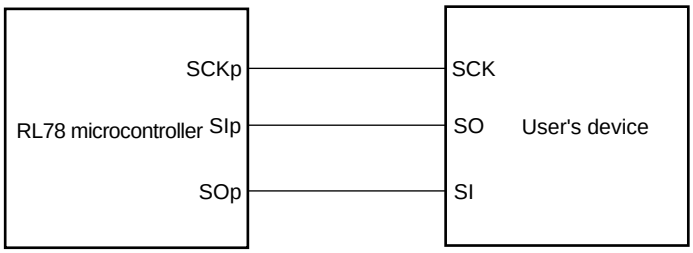
AC Timing Test Points



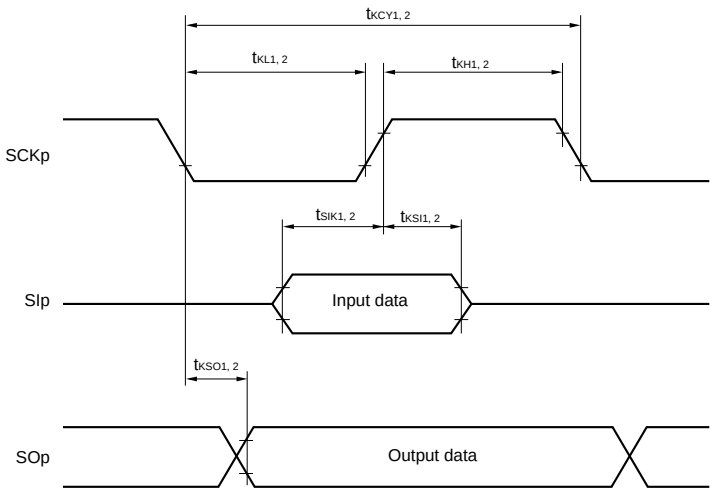
External System Clock Timing



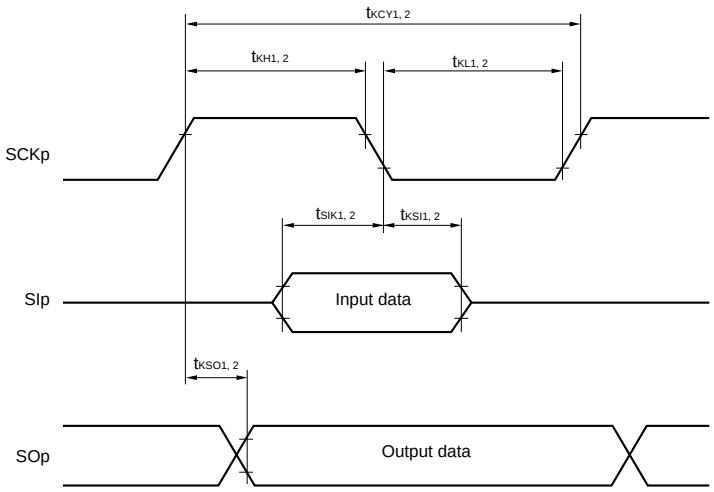
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01)

2. m: Unit number, n: Channel number (mn = 00, 01)

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SOp) pull-up resistance, C_b[F]: Communication line (SCKp, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00)

4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/2)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300			ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500			ns
			2.4 V ≤ V_{DD} < 3.3 V, 2.4 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150			ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458			ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18			ns
		2.4 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50			ns

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

2. Use it with $V_{DD} \geq V_b$.

(**Remarks** are listed two pages after the next page.)

2.5.2 Serial interface IICA

(1) I^2C standard mode

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	2.7 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
			2.4 V ≤ V_{DD} ≤ 5.5 V	0	100	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		250		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		250		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V		0	3.45	μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		0	3.45	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.0		μs
Bus-free time	t_{BUF}	2.7 V ≤ V_{DD} ≤ 5.5 V		4.7		μs
		2.4 V ≤ V_{DD} ≤ 5.5 V		4.7		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(4) BC option standard (Function)

(T_A = –40 to +85°C, 4.35 V ≤ UV_{BUS} ≤ 5.25 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi/UDMi input reference voltage (UV_{BUS} divider ratio) • VDOUEi = 0 (i = 0))	VDSELi [3:0] (i = 0)	0000	V_{DDET0}		27	32	37	% UV_{BUS}
		0001	V_{DDET1}		29	34	39	% UV_{BUS}
		0010	V_{DDET2}		32	37	42	% UV_{BUS}
		0011	V_{DDET3}		35	40	45	% UV_{BUS}
		0100	V_{DDET4}		38	43	48	% UV_{BUS}
		0101	V_{DDET5}		41	46	51	% UV_{BUS}
		0110	V_{DDET6}		44	49	54	% UV_{BUS}
		0111	V_{DDET7}		47	52	57	% UV_{BUS}
		1000	V_{DDET8}		51	56	61	% UV_{BUS}
		1001	V_{DDET9}		55	60	65	% UV_{BUS}
		1010	V_{DDET10}		59	64	69	% UV_{BUS}
		1011	V_{DDET11}		63	68	73	% UV_{BUS}
		1100	V_{DDET12}		67	72	77	% UV_{BUS}
		1101	V_{DDET13}		71	76	81	% UV_{BUS}
		1110	V_{DDET14}		75	80	85	% UV_{BUS}
		1111	V_{DDET15}		79	84	89	% UV_{BUS}

(4) When Reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), Reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0 to ANI7, ANI16, ANI17, ANI19

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}				8		Bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

2.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

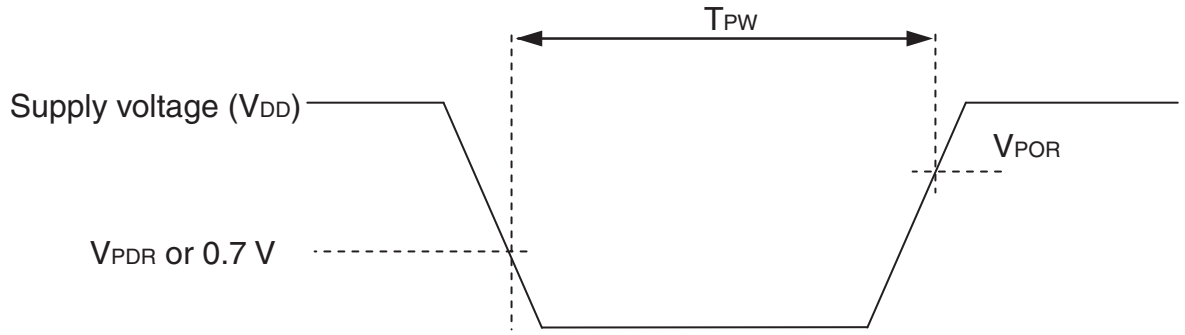
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.47	1.51	1.55	V
	V_{PDR}	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR}. This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock (f_{MAIN}) is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
UV_{DD} pin input voltage	V_{IUVDD}	UV_{DD}	−0.3 to V_{DD} +0.3	V
Input voltage	V_{I1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P70 to P75, P120 to P124, P137, P140, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	UDP0, UDM0, UDP1, UDM1	−0.3 to +6.5	V
	V_{I4}	UV_{BUS}	−0.3 to +6.5	V
Output voltage	V_{O1}	P00, P01, P14 to P17, P20 to P27, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140	−0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	UDP0, UDM0, UDP1, UDM1	−0.3 to +6.5	V
Analog input voltage	V_{AI1}	ANI16, ANI17, ANI19	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF} (+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI7	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF} (+) +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF} (+) : The + side reference voltage of the A/D converter. This can be selected from AV_{REFP}, the internal reference voltage (1.45 V), and V_{DD}.

3. V_{SS} : Reference voltage

3.5.2 Serial interface IICA

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f_{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}		4.0		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		μs
Bus-free time	t_{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

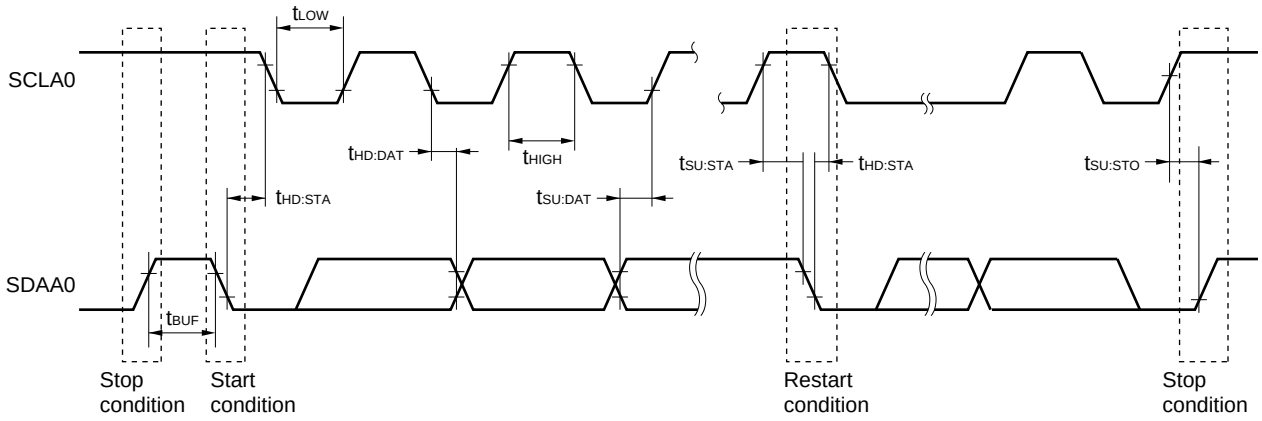
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Caution The values in the above table are applied even when bit 1 (PIOR1) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



(3) BC option standard (Host)

(T_A = –40 to +105°C, 4.75 V ≤ UV_{BUS} ≤ 5.25 V, 3.0 V ≤ UV_{DD} ≤ 3.6 V, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter			Symbol	Conditions	MIN.	TYP.	MAX.	Unit
UDPi output voltage (UV_{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{P20}		38	40	42	% UV_{BUS}
		1001	V_{P27}		51.6	53.6	55.6	% UV_{BUS}
		1010	V_{P20}		38	40	42	% UV_{BUS}
		1100	V_{P33}		60	66	72	% UV_{BUS}
UDMi output voltage (UV_{BUS} divider ratio) • VDOUEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{M20}		38	40	42	% UV_{BUS}
		1001	V_{M20}		38	40	42	% UV_{BUS}
		1010	V_{M27}		51.6	53.6	55.6	% UV_{BUS}
		1100	V_{M33}		60	66	72	% UV_{BUS}
UDPi comparing voltage Note 1 (UV_{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{HDETP_UP0}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETP_DWN0}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1001	V_{HDETP_UP1}	The rise of pin voltage detection voltage	60.5			% UV_{BUS}
			V_{HDETP_DWN1}	The fall of pin voltage detection voltage			45.0	% UV_{BUS}
		1010	V_{HDETP_UP2}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETP_DWN2}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
UDMi comparing voltage Note 1 (UV_{BUS} divider ratio) • VDOUEi = 1 • CUSDETEi = 1	VDSELi [3:0] (i = 0, 1)	1000	V_{HDETM_UP0}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETM_DWN0}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1001	V_{HDETM_UP1}	The rise of pin voltage detection voltage	56.2			% UV_{BUS}
			V_{HDETM_DWN1}	The fall of pin voltage detection voltage			29.4	% UV_{BUS}
		1010	V_{HDETM_UP2}	The rise of pin voltage detection voltage	60.5			% UV_{BUS}
			V_{HDETM_DWN2}	The fall of pin voltage detection voltage			45.0	% UV_{BUS}
UDPi pull-up detection Note 2 Connect detection with the full speed function (pull-up resistor)		1000 1001 1010	R_{HDET_PULL}	In full-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
UDMi pull-up detection Note 2 Connect detection with the low-speed (pull-up resistor)		1000 1001 1010	R_{HDET_PULL}	In low-speed mode, the power supply voltage range of pull-up resistors connected to the USB function module is between 3.0 V and 3.6 V.			1.575	kΩ
UDMi sink current detection Note 2 Connect detection with the BC1.2 portable device (sink resistor)		1000 1001 1010	I_{HDET_SINK}		25			μA

Notes 1. If the voltage output from UDPi or UDMi (i = 0, 1) exceeds the range of the MAX and MIN values prescribed in this specification, DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

2. If the pull-up resistance or sink current prescribed in this specification is applied to UDPi or UDMi (i = 0, 1), DPCUSDETi (bit 8) and DMCUSDETi (bit 9) of the USBBCOPTi register are set to 1.

Remark i = 0, 1