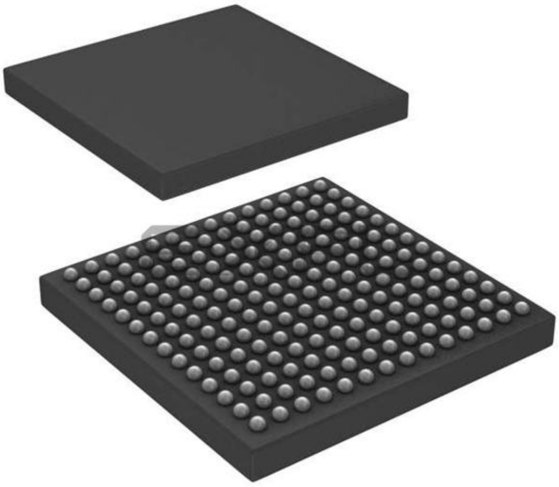

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	352K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	PG-LFBGA-196-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4700e196f2048aaxqma1

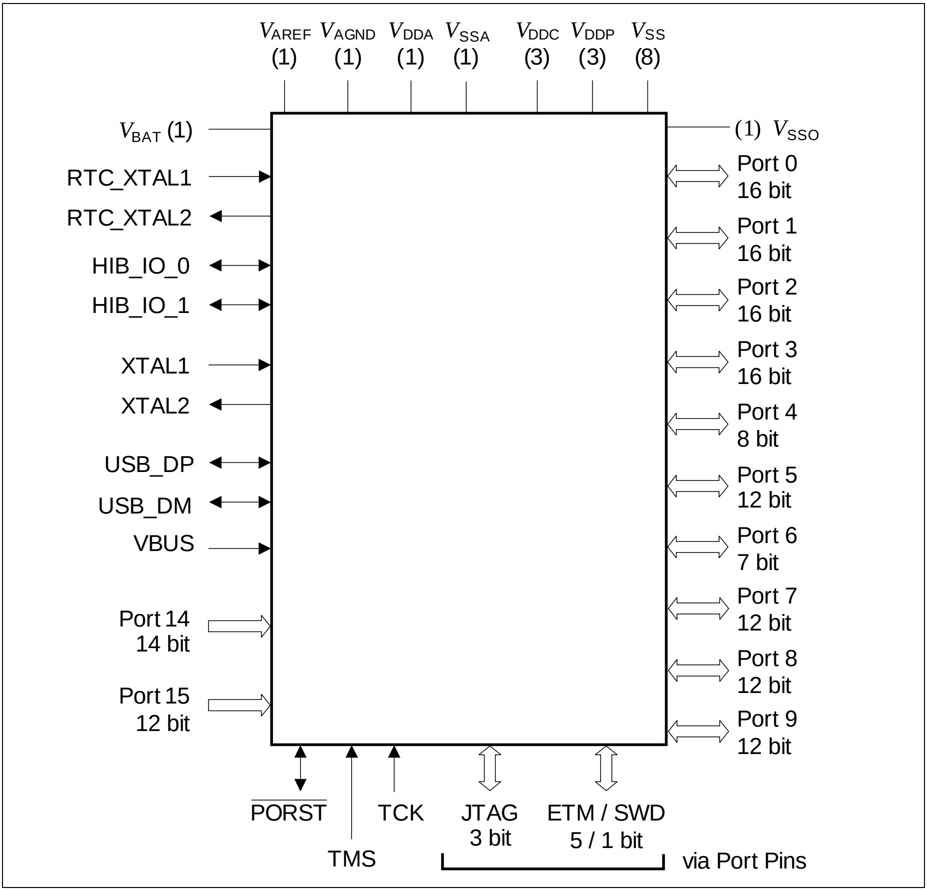

Figure 3 **XMC4[78]00 Logic Symbol PG-LFBGA-196**

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

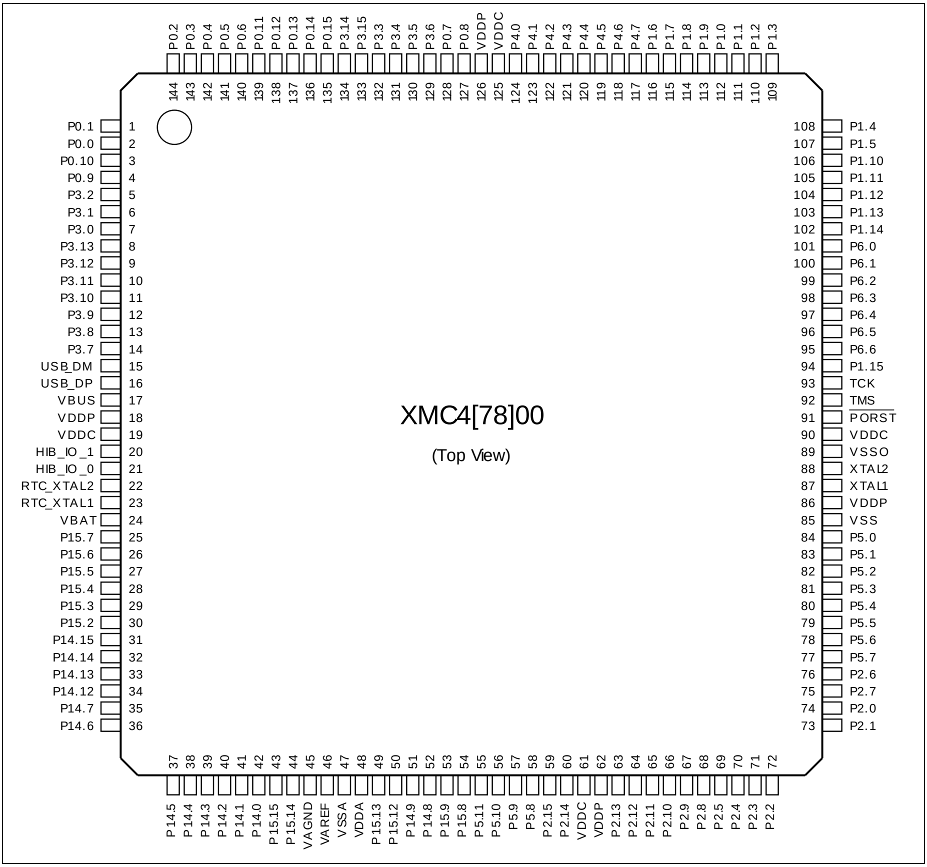

Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 9 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the "Function" column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The "Pad Type" indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the "Notes", special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 10 Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.0	E4	2	2	A1+	
P0.1	E3	1	1	A1+	
P0.2	C3	144	100	A2	
P0.3	C4	143	99	A2	
P0.4	D5	142	98	A2	
P0.5	C5	141	97	A2	
P0.6	C6	140	96	A2	
P0.7	D7	128	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	C8	127	88	A2	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	F4	4	4	A2	
P0.10	D4	3	3	A1+	

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P5.3	L10	81	-	A2	
P5.4	M10	80	-	A2	
P5.5	L8	79	-	A2	
P5.6	M8	78	-	A2	
P5.7	L7	77	55	A1+	
P5.8	K6	58	-	A2	
P5.9	M6	57	-	A2	
P5.10	K5	56	-	A1+	
P5.11	L5	55	-	A1+	
P6.0	J10	101	-	A2	
P6.1	H9	100	-	A2	
P6.2	K10	99	-	A2	
P6.3	J9	98	-	A1+	
P6.4	H10	97	-	A2	
P6.5	H11	96	-	A2	
P6.6	H12	95	-	A2	
P7.0	L13	-	-	A2	
P7.1	M13	-	-	A2	
P7.2	N13	-	-	A2	
P7.3	M14	-	-	A2	
P7.4	N14	-	-	A1+	
P7.5	L14	-	-	A1+	
P7.6	K14	-	-	A1+	
P7.7	J14	-	-	A1+	
P7.8	H14	-	-	A2	
P7.9	G13	-	-	A1+	
P7.10	G14	-	-	A1+	
P7.11	F14	-	-	A1+	
P8.0	B7	-	-	A2	
P8.1	A7	-	-	A2	
P8.2	B3	-	-	A2	
P8.3	B2	-	-	A2	
P8.4	B6	-	-	A1+	

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P14.14	K3	32	21	AN/DIG_IN	
P14.15	K2	31	20	AN/DIG_IN	
P15.2	K1	30	19	AN/DIG_IN	
P15.3	J2	29	18	AN/DIG_IN	
P15.4	J4	28	-	AN/DIG_IN	
P15.5	J3	27	-	AN/DIG_IN	
P15.6	J5	26	-	AN/DIG_IN	
P15.7	J6	25	-	AN/DIG_IN	
P15.8	P6	54	39	AN/DIG_IN	
P15.9	N6	53	38	AN/DIG_IN	
P15.12	M5	50	-	AN/DIG_IN	
P15.13	P4	49	-	AN/DIG_IN	
P15.14	N4	44	-	AN/DIG_IN	
P15.15	M4	43	-	AN/DIG_IN	
USB_DP	G1	16	9	special	
USB_DM	F1	15	8	special	
HIB_IO_0	H4	21	14	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as open-drain output and drives "0". As output the medium driver mode is active.
HIB_IO_1	H3	20	13	A1 special	At the first power-up and with every reset of the hibernate domain this pin is configured as input with no pull device active. As output the medium driver mode is active.
TCK	J8	93	67	A1	Weak pull-down active.
TMS	J7	92	66	A1+	Weak pull-up active. As output the strong-soft driver mode is active.

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	**ALTn**	**HWO0**	**HWI0**	**Input**	**Input**
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

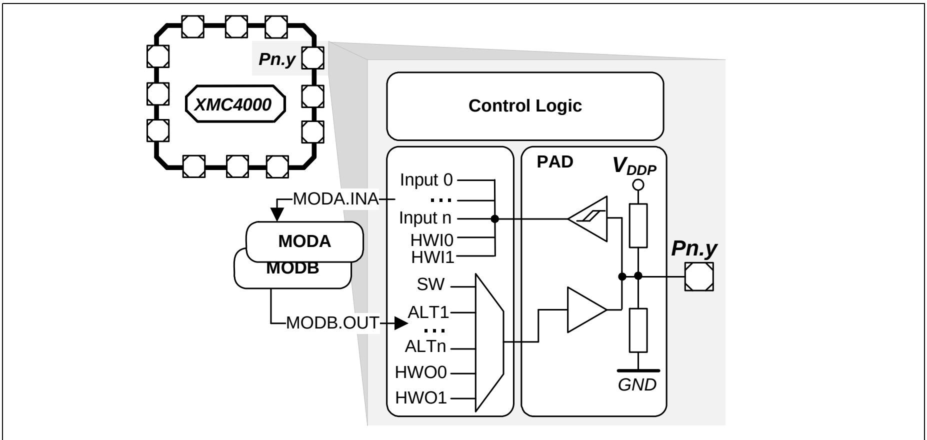

Figure 8 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware "masters" (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 12 Port I/O Functions

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ECAT0.PHY_RST	CAN.N0_TXD	CCU80.OUT21	LEDTS0.COL2					U1C1.DX0D	ETH0.CLK_RMIIB	ERU0.0B0					ETH0.CLKRXB
P0.1	USB.DRIVEVBUS	U1C1.DOUT0	CCU80.OUT11	LEDTS0.COL3						ETH0.CRS_DVB	ERU0.0A0				ECAT0.P1_RX_CLKA	ETH0.RXDVB
P0.2	ECAT0.P1_TXD2	U1C1.SELO1	CCU80.OUT01		U1C0.DOUT3	EBU.AD0	U1C0.HWIN3	EBU.D0	ETH0.RXD0B		ERU0.3B3					
P0.3	ECAT0.P1_TXD3		CCU80.OUT20		U1C0.DOUT2	EBU.AD1	U1C0.HWIN2	EBU.D1	ETH0.RXD1B			ERU1.3B0				
P0.4	ETH0.TX_EN		CCU80.OUT10		U1C0.DOUT1	EBU.AD2	U1C0.HWIN1	EBU.D2		U1C0.DX0A	ERU0.2B3				ECAT0.P1_RXD3A	
P0.5	ETH0.TXD0	U1C0.DOUT0	CCU80.OUT00		U1C0.DOUT0	EBU.AD3	U1C0.HWIN0	EBU.D3		U1C0.DX0B		ERU1.3A0			ECAT0.P1_RXD2A	
P0.6	ETH0.TXD1	U1C0.SELO0	CCU80.OUT30			EBU.$\overline{\text{ADV}}$				U1C0.DX2A	ERU0.3B2		CCU80.IN2B		ECAT0.P1_RXD1A	
P0.7	WWDT.SERVICE_OUT	U0C0.SELO0	ECAT0.LED_ERR			EBU.AD6	DB.TDI	EBU.D6	U0C0.DX2B	DSD.DIN1A	ERU0.2B1		CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A
P0.8	SCU.EXTCLK	U0C0.SCLKOUT	ECAT0.LED_RUN			EBU.AD7	DB.$\overline{\text{TRST}}$	EBU.D7	U0C0.DX1B	DSD.DIN0A	ERU0.2A1	CAN.N3_RXDA	CCU80.IN1B			
P0.9		U1C1.SELO0	CCU80.OUT12	LEDTS0.COL0	ETH0.MDO	EBU.$\overline{\text{CS1}}$	ETH0.MDIA		U1C1.DX2A	USB.ID	ERU0.1B0				ECAT0.P1_RX_DVA	
P0.10	ETH0.MDC	U1C1.SCLKOUT	CCU80.OUT02	LEDTS0.COL1					U1C1.DX1A		ERU0.1A0				ECAT0.P1_TX_CLKA	
P0.11	ECAT0.P1_LINK_ACT	U1C0.SCLKOUT	CCU80.OUT31		SDMMC.$\overline{\text{RST}}$	EBU.$\overline{\text{BREQ}}$			ETH0.RXERB	U1C0.DX1A	ERU0.3A2				ECAT0.P1_RXD0A	
P0.12		U1C1.SELO0	CCU40.OUT3		ECAT0.MDO	EBU.$\overline{\text{HLDA}}$	ECAT0.MDIA	EBU.$\overline{\text{HLDA}}$		U1C1.DX2B	ERU0.2B2					
P0.13		U1C1.SCLKOUT	CCU40.OUT2							U1C1.DX1B	ERU0.2A2					
P0.14		U1C0.SELO1	CCU40.OUT1		U1C1.DOUT3		U1C1.HWIN3						CCU42.IN3C			
P0.15		U1C0.SELO2	CCU40.OUT0		U1C1.DOUT2		U1C1.HWIN2						CCU42.IN2C			
P1.0	DSD.CGPWMN	U0C0.SELO0	CCU40.OUT3	ERU1.PDOUT3					U0C0.DX2A		ERU0.3B0		CCU40.IN3A			ECAT0.P0_TX_CLKA
P1.1	DSD.CGPWMP	U0C0.SCLKOUT	CCU40.OUT2	ERU1.PDOUT2			SDMMC.SDWC		U0C0.DX1A	POSIF0.IN2A	ERU0.3A0		CCU40.IN2A			ECAT0.P0_RX_CLKA
P1.2	ECAT0.P0_TXD3		CCU40.OUT1	ERU1.PDOUT1	U0C0.DOUT3	EBU.AD14	U0C0.HWIN3	EBU.D14		POSIF0.IN1A		ERU1.2B0	CCU40.IN1A			
P1.3	ECAT0.P0_TX_ENA	U0C0.MCLKOUT	CCU40.OUT0	ERU1.PDOUT0	U0C0.DOUT2	EBU.AD15	U0C0.HWIN2	EBU.D15		POSIF0.IN0A		ERU1.2A0	CCU40.IN0A			
P1.4	WWDT.SERVICE_OUT	CAN.N0_TXD	CCU80.OUT33	CCU81.OUT20	U0C0.DOUT1		U0C0.HWIN1		U0C0.DX0B	CAN.N1_RXDD	ERU0.2B0		CCU41.IN0C			ECAT0.P0_RXD0A

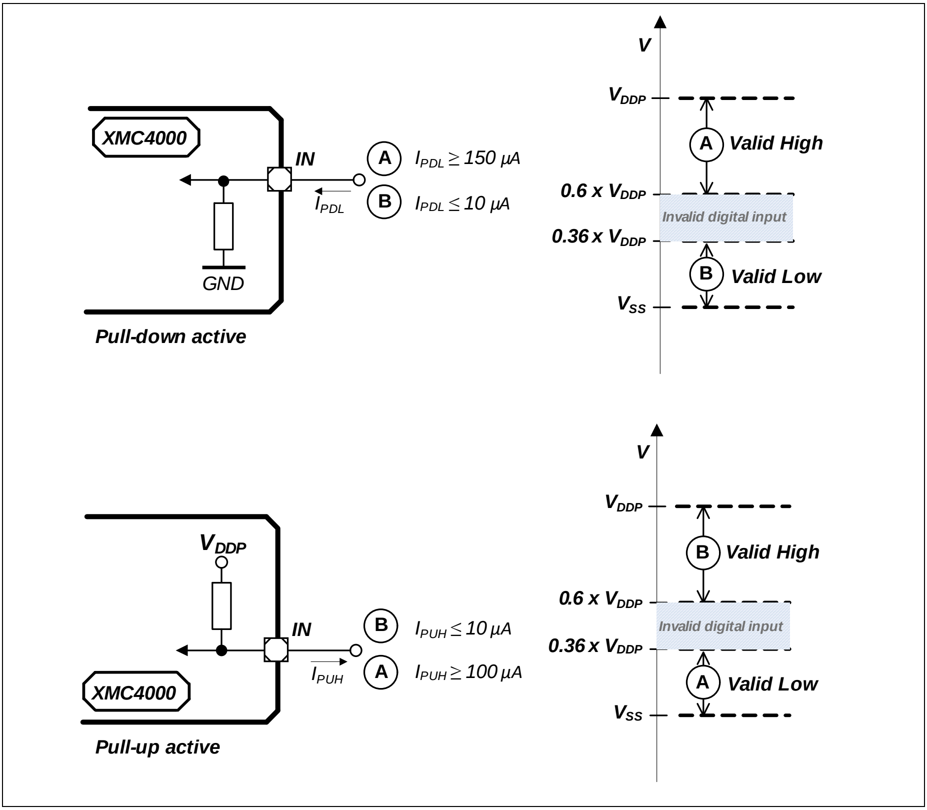

Figure 13 Pull Device Input Characteristics

Figure 13 visualizes the input characteristics with an active internal pull device:

- in the cases "A" the internal pull device is overridden by a strong external driver;
- in the cases "B" the internal pull device defines the input logical state against a weak external load.

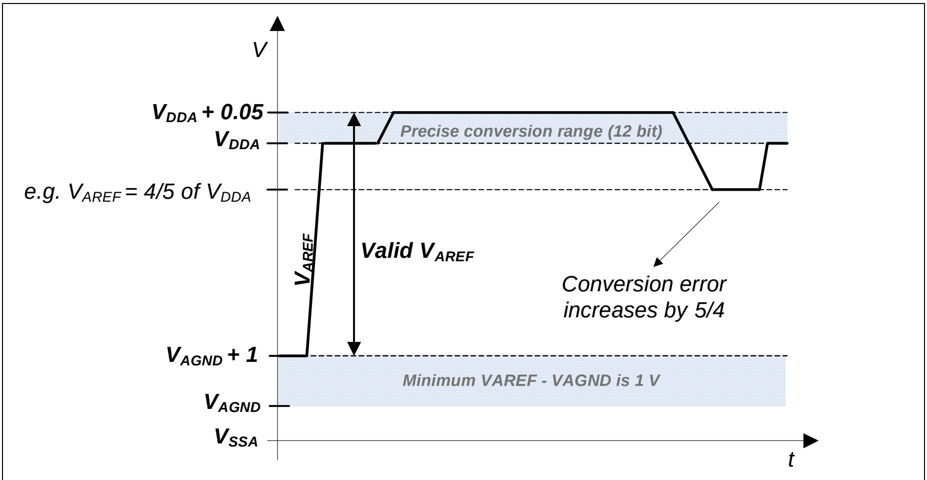

Figure 14 VADC Reference Voltage Range

The power-up calibration of the VADC requires a maximum number of 4 352 f_{ADCI} cycles.

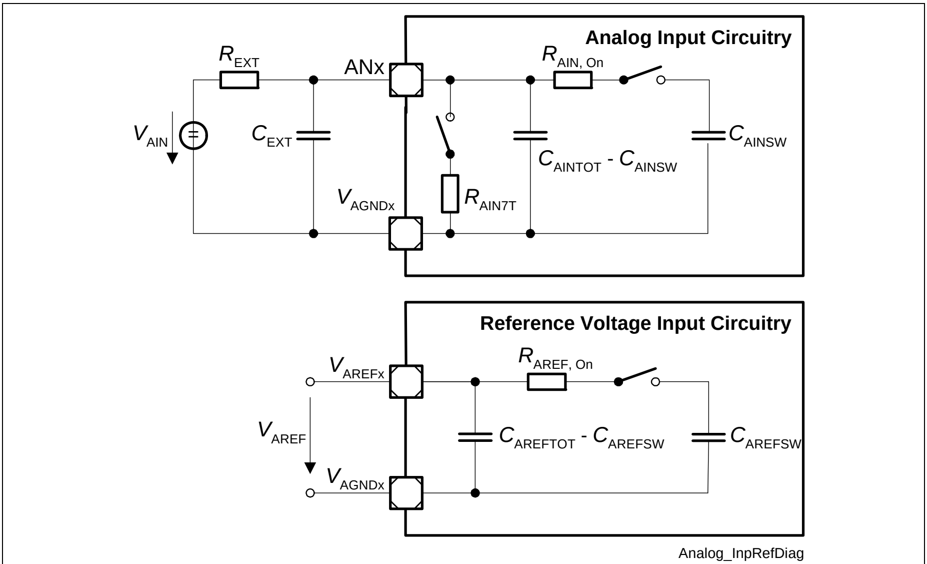

Figure 15 VADC Input Circuits

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE}	CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1)]
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	10	µs	

1) At V_{DDP_max} = 3.63 V the typical offset error increases by an additional ΔT_{OE} = ±1 °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

$$\text{Temperature } T_{DTS} = (\text{RESULT} - 605) / 2.05 \ [°\text{C}]$$

This formula and the values defined in **Table 29** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.7 Oscillator Pins

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The oscillator pins can be operated with an external crystal (see **Figure 20**) or in direct input mode (see **Figure 21**).

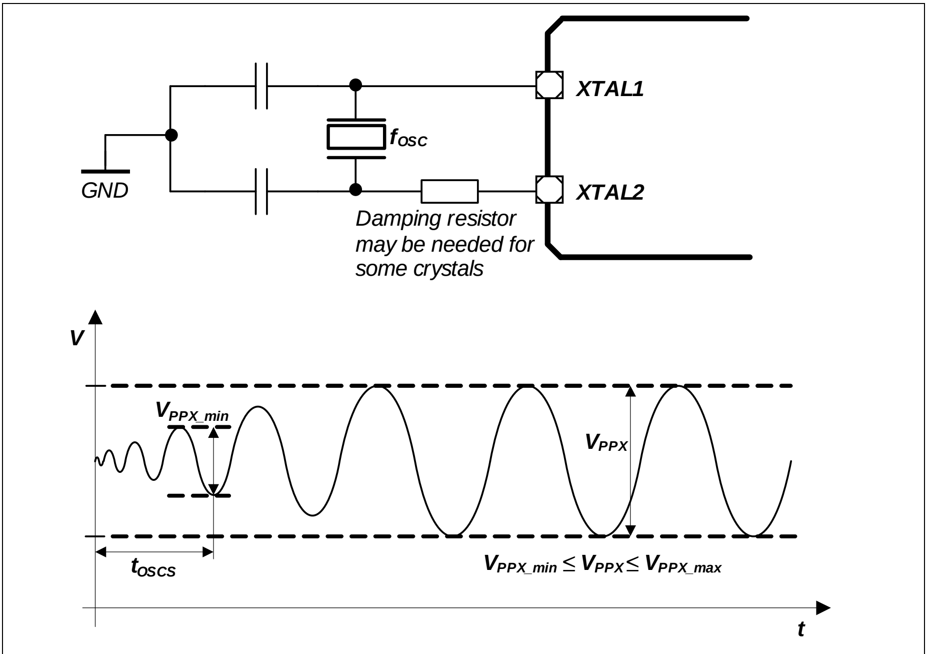

Figure 20 Oscillator in Crystal Mode

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

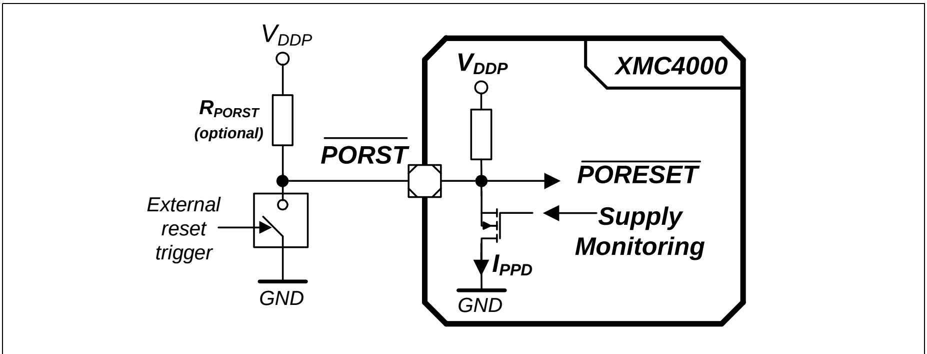

Figure 25 $\overline{\text{PORST}}$ Circuit

Table 37 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	[4]
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4[78]00 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 44 ETM Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TRACECLK period	t_1	CC	13.8	–	–	ns	–
TRACECLK high time	t_2	CC	2	–	–	ns	–
TRACECLK low time	t_3	CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4	CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5	CC	–	–	3	ns	–
TRACEDATA output valid time	t_6	CC	-2	–	3	ns	–

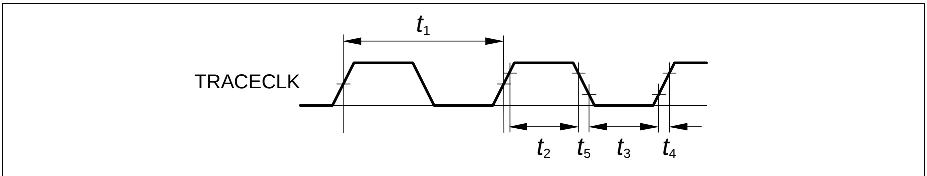

Figure 30 ETM Clock Timing

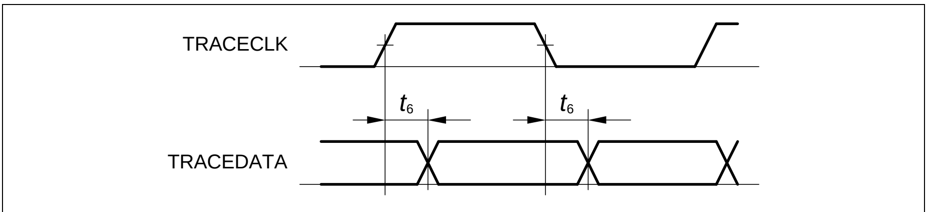

Figure 31 ETM Data Timing

3.3.9 Peripheral Timing

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 45 DSD Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MCLK period in master mode	t_1	CC	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in master mode	t_2	CC	9	–	–	ns	$t_2 > t_{PERIPH}$ [1]
MCLK low time in master mode	t_3	CC	9	–	–	ns	$t_3 > t_{PERIPH}$ [1]
MCLK period in slave mode	t_1	SR	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in slave mode	t_2	SR	t_{PERIPH}	–	–	ns	[1]
MCLK low time in slave mode	t_3	SR	t_{PERIPH}	–	–	ns	[1]
DIN input setup time to the active clock edge	t_4	SR	t_{PERIPH} + 4	–	–	ns	[1]
DIN input hold time from the active clock edge	t_5	SR	t_{PERIPH} + 3	–	–	ns	[1]

1) $t_{PERIPH} = 1 / f_{PERIPH}$

With clock delay:

(2)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(3)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} < t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 10$$

$$t_{DATA\_DELAY} < 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of t_{WL}= 20 ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(4)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} < 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5$$

$$t_{DATA\_DELAY} < 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of t_{WL}= 20 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

High-Speed Input Path (Read)

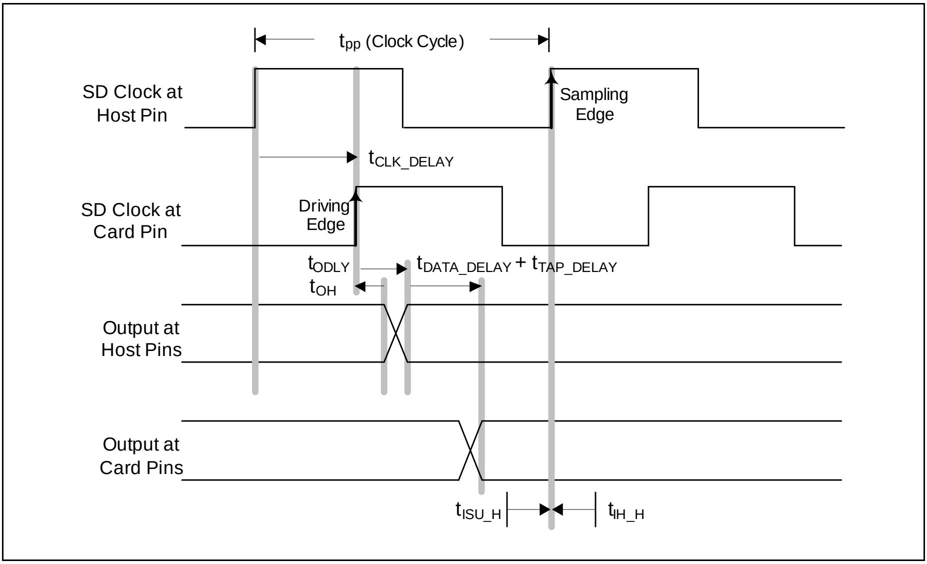

Figure 40 High-Speed Input Path

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(11)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_H} < t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{pp} - t_{ODLY} - t_{ISU\_H} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values Min.	Limit Values Max.	Unit
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS}(3:0)}$ low		CC	t_8	–	9	
$\overline{\text{CS}(3:0)}$ high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC}(3:0)}$ low		CC	t_{16}	–	9	
$\overline{\text{BC}(3:0)}$ high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1)]		CC	t_{22}	–	7	
CKE output hold[1)]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 63 USB Timing Parameters (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	t_R	CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F	CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F	CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS}	CC	1.3	–	2.0	V	C_L = 50 pF

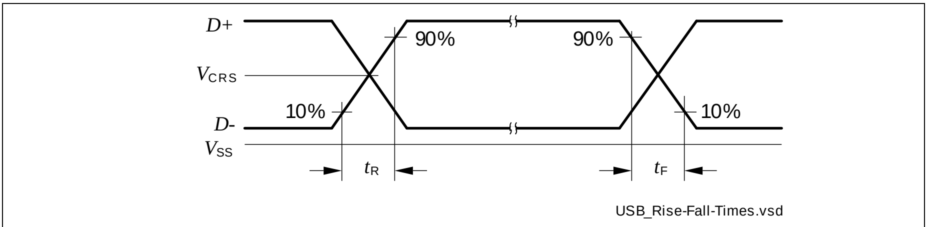

Figure 50 USB Signal Timing

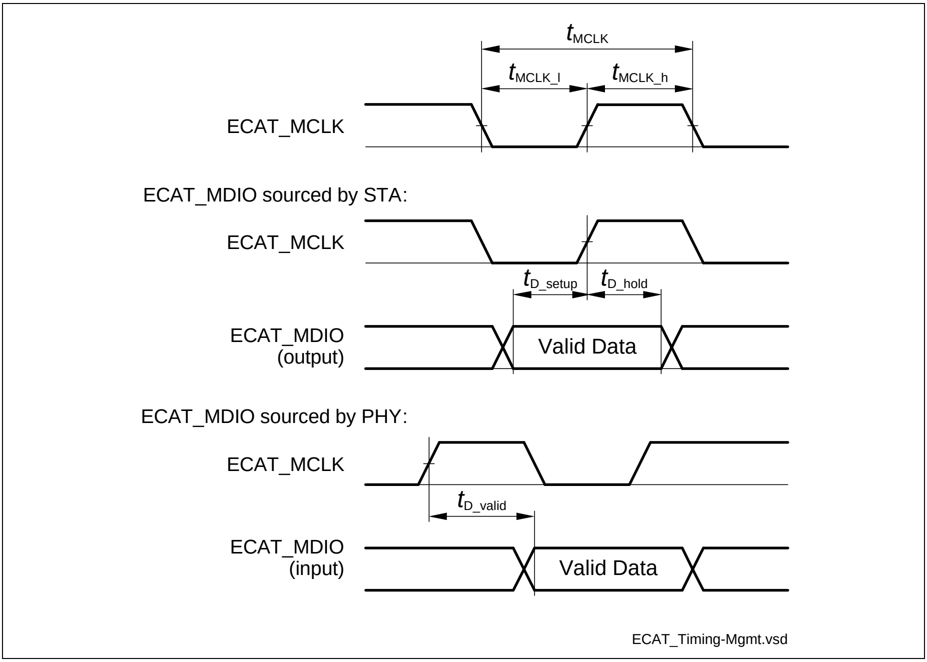

Figure 56 ECAT Management Signal Timing

3.3.13.3 MII Timing TX Characteristics

Table 68 ETH MII TX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PHY_CLK25, TX_CLK period	t_{TX_CLK} SR	–	40	–	ns	
Delay between PHY clock source PHY_CLK25 and TX_CLK output of the PHY	t_{PHY_delay} SR	–	–	–	ns	PHY dependent

www.infineon.com

Published by Infineon Technologies AG