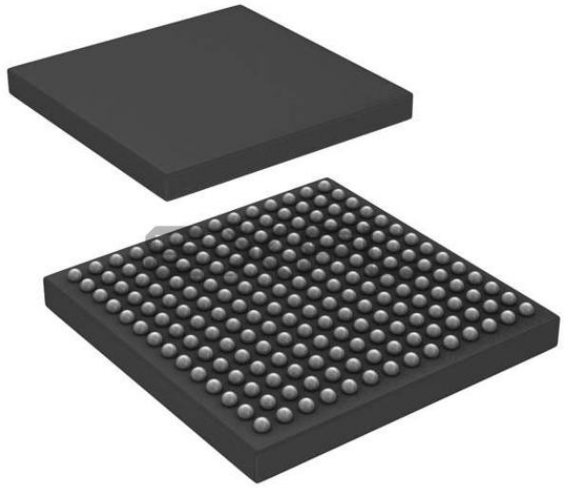
Infineon Technologies - XMC4700E196K1536AAXQMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	155
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	PG-LFBGA-196-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4700e196k1536aaxqma1

XMC4[78]00 Data Sheet

Revision History: V1.0 2016-01

Previous Versions:
V0.7 2015-10 (preliminary)

Page	Subjects
8	Corrected EtherCAT features to 8 Fieldbus Memory Management Units (FMMU) and 8 Sync Manager.
46	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
53	Added HIBIO characteristics.
58	Corrected DAC INL and gain error.
70	Changed frequency dependency of the current consumption.
73	Added peripheral idle current overview.
127ff	Updated package parameters and drawings.
132	Higher HBM and CDM ESD limits.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
200 Kbytes	1FFE E000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2001 FFFF$_H$	–
276 Kbytes	1FFE 8000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2001 FFFF$_H$	2002 0000$_H$ – 2002 CFFF$_H$
352 Kbytes	1FFE 8000$_H$ – 1FFF FFFF$_H$	2000 0000$_H$ – 2001 FFFF$_H$	2002 0000$_H$ – 2003 FFFF$_H$

Table 6 ADC Channels[1)]

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144 PG-LFBGA-196	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4700 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 7001$_H$	EES-AA, ES-AA, AA
JTAG IDCODE	101D F083$_H$	EES-AA, ES-AA, AA

Table 8 XMC4800 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 8001$_H$	EES-AA, ES-AA, AA
JTAG IDCODE	101D F083$_H$	EES-AA, ES-AA, AA

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

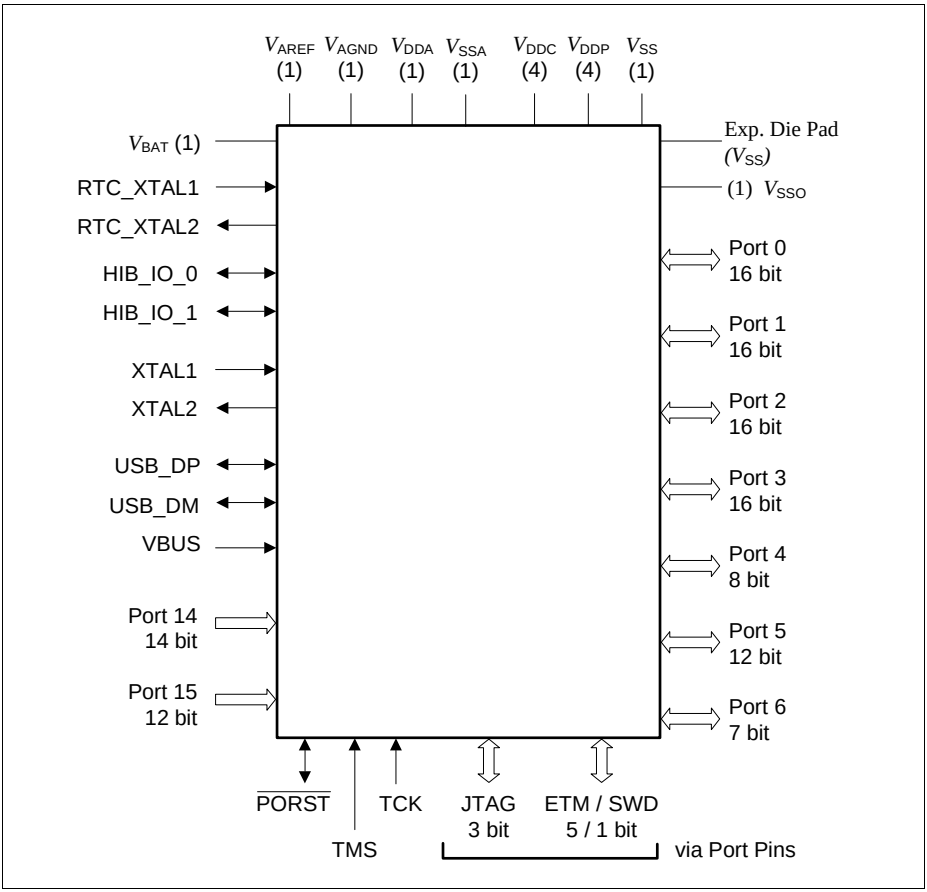

Figure 2 XMC4[78]00 Logic Symbol PG-LQFP-144

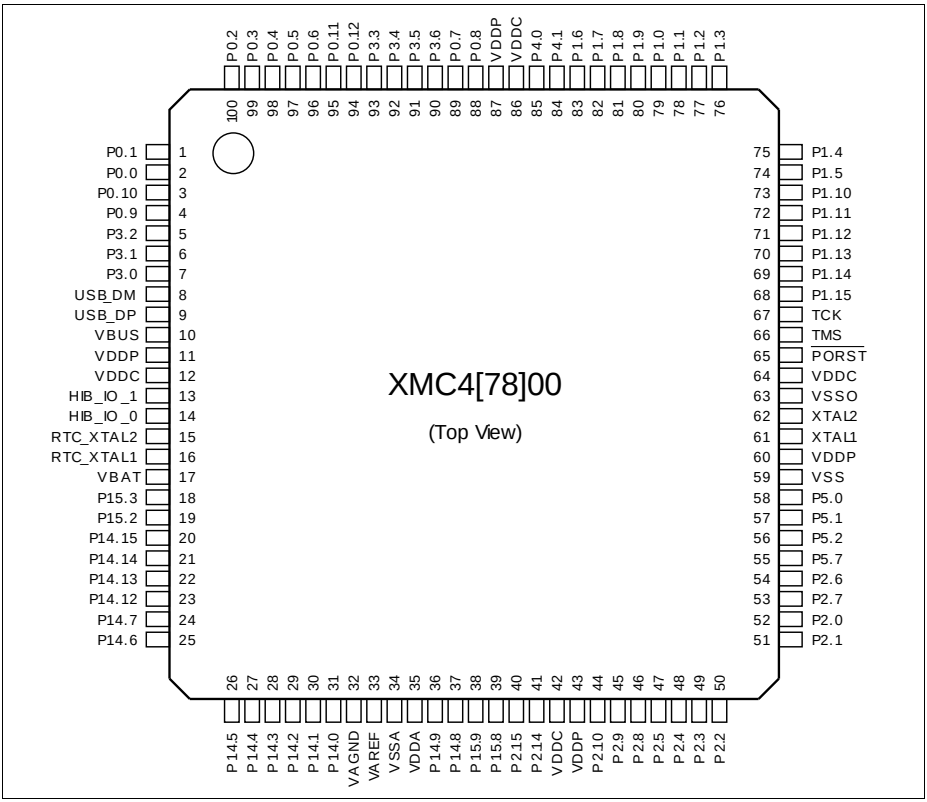

Figure 7 XMC4[78]00 PG-LQFP-100 Pin Configuration (top view)

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P2.10	N8	66	44	A2	
P2.11	P8	65	-	A2	
P2.12	N7	64	-	A2	
P2.13	P7	63	-	A2	
P2.14	M7	60	41	A2	
P2.15	L6	59	40	A2	
P3.0	E1	7	7	A2	
P3.1	D2	6	6	A2	
P3.2	D3	5	5	A2	
P3.3	H7	132	93	A1+	
P3.4	G7	131	92	A1+	
P3.5	D6	130	91	A2	
P3.6	C7	129	90	A2	
P3.7	G4	14	-	A1+	
P3.8	G3	13	-	A1+	
P3.9	H5	12	-	A1+	
P3.10	H6	11	-	A1+	
P3.11	F3	10	-	A1+	
P3.12	F2	9	-	A2	
P3.13	E2	8	-	A2	
P3.14	F6	134	-	A1+	
P3.15	F7	133	-	A1+	
P4.0	D8	124	85	A2	
P4.1	C9	123	84	A2	
P4.2	G8	122	-	A1+	
P4.3	H8	121	-	A1+	
P4.4	E7	120	-	A1+	
P4.5	F8	119	-	A1+	
P4.6	E8	118	-	A1+	
P4.7	E9	117	-	A1+	
P5.0	K9	84	58	A1+	
P5.1	K8	83	57	A1+	
P5.2	K7	82	56	A1+	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P2.12	ETH0. TXD2	ECAT0. P1_TXD1	CCU81. OUT33	ETH0. TXD0	DB. ETM_TRACEDATA1	EBU. AD30		EBU. D30					CCU43. IN3C			
P2.13	ETH0. TXD3	ECAT0. P1_TXD2		ETH0. TXD1	DB. ETM_TRACEDATA0	EBU. AD31		EBU. D31					CCU43. IN2C			
P2.14	VADC. EMUX11	U1C0. DOUT0	CCU80. OUT21	CAN. N4_TXD	DB. ETM_TRACECLK	EBU. BC0				U1C0. DX0D			CCU43. IN0B	CCU43. IN1B	CCU43. IN2B	CCU43. IN3B
P2.15	VADC. EMUX12	ECAT0. P1_TXD3	CCU80. OUT11	LEDTS0. LINE6	LEDTS0. EXTENDED6	EBU. BC1	LEDTS0. TSIN6A		ETH0. COLA	U1C0. DX0C	CAN. N4_RXDA		CCU42. IN0B	CCU42. IN1B	CCU42. IN2B	CCU42. IN3B
P3.0	U2C1. SELO0	U0C1. SCLKOUT	CCU42. OUT0	ECAT0. P1_TX_ENA		EBU. RD			U0C1. DX1B				CCU80. IN2C	CCU81. IN0C		
P3.1		U0C1. SELO0	ECAT0. P1_TXD0			EBU. RD_WR			U0C1. DX2B		ERU0. 0B1		CCU80. IN1C			
P3.2	USB. DRIVEVBUS	CAN. N0_TXD	ECAT0. P1_TXD1	LEDTS0. COLA		EBU. CS0					ERU0. 0A1		CCU80. IN0C			
P3.3		U1C1. SELO1	CCU42. OUT3	ECAT0. MCLK	SDMMC. LED			EBU. WAIT		DSD. DIN3B			CCU42. IN3A	CCU80. IN3B		
P3.4	U2C1. MCLKOUT	U1C1. SELO2	CCU42. OUT2	DSD. MCLK3	SDMMC. BUS_POWER			EBU. HOLD	U2C1. DX0B	DSD. MCLK3B			CCU42. IN2A	CCU80. IN0B	ECAT0. P1_LINKA	
P3.5	U2C1. DOUT0	U1C1. SELO3	CCU42. OUT1	U0C1. DOUT0	SDMMC. CMD_OUT	EBU. AD4	SDMMC. CMD_IN	EBU. D4	U2C1. DX0A		ERU0. 3B1		CCU42. IN1A		ECAT0. P1_RX_ERRA	
P3.6	U2C1. SCLKOUT	U1C1. SELO4	CCU42. OUT0	U0C1. SCLKOUT	SDMMC. CLK_OUT	EBU. AD5	SDMMC. CLK_IN	EBU. D5	U2C1. DX1B		ERU0. 3A1		CCU42. IN0A			
P3.7	ECAT0. SYNC0	CAN. N2_TXD	CCU41. OUT3	LEDTS0. LINE0					U2C0. DX0C							
P3.8	U2C0. DOUT0	U0C1. SELO3	CCU41. OUT2	LEDTS0. LINE1					CAN. N2_RXDB				POSIF1. IN2B			
P3.9	U2C0. SCLKOUT	CAN. N1_TXD	CCU41. OUT1	LEDTS0. LINE2									POSIF1. IN1B			
P3.10	U2C0. SELO0	CAN. N0_TXD	CCU41. OUT0	LEDTS0. LINE3	U0C1. DOUT3		U0C1. HWIN3						POSIF1. IN0B			
P3.11	U2C1. DOUT0	U0C1. SELO2	CCU42. OUT3	LEDTS0. LINE4	U0C1. DOUT2		U0C1. HWIN2		CAN. N1_RXDB					CCU81. IN3C		
P3.12	ECAT0. P1_LINK_ACT	U0C1. SELO1	CCU42. OUT2	LEDTS0. LINE5	U0C1. DOUT1		U0C1. HWIN1		CAN. N0_RXDC	U2C1. DX0D				CCU81. IN2C		
P3.13	U2C1. SCLKOUT	U0C1. DOUT0	CCU42. OUT1	LEDTS0. LINE6	U0C1. DOUT0		U0C1. HWIN0		U0C1. DX0D				CCU80. IN3C	CCU81. IN1C		
P3.14		U1C0. SELO3			U1C1. DOUT1		U1C1. HWIN1			U1C1. DX0B			CCU42. IN1C			
P3.15		U1C1. DOUT0			U1C1. DOUT0		U1C1. HWIN0			U1C1. DX0A			CCU42. IN0C			
P4.0	CAN. N3_TXD	ECAT0. PHY_CLK25	DSD. MCLK1	U1C0. SCLKOUT	SDMMC. DATA0_OUT	EBU. AD8	SDMMC. DATA0_IN	EBU. D8	U1C1. DX1C	DSD. MCLK1B	U0C1. DX0E	U2C1. DX0C				ECAT0. P0_RX_ERRA
P4.1	U2C1. SELO0	U1C1. MCLKOUT	DSD. MCLK0	U0C1. SELO0	SDMMC. DATA3_OUT	EBU. AD9	SDMMC. DATA3_IN	EBU. D9	U2C1. DX2B	DSD. MCLK0B		U2C1. DX2A	DSD. MCLK1D			ECAT0. P0_LINKA
P4.2	U2C1. SELO1	U1C1. DOUT0		U2C1. SCLKOUT	ECAT0. MDO		ECAT0. MDIB		U1C1. DX0C			U2C1. DX1A	CCU43. IN1C			

2.3 Power Connection Scheme

Figure 9. shows a reference power connection scheme for the XMC4[78]00.

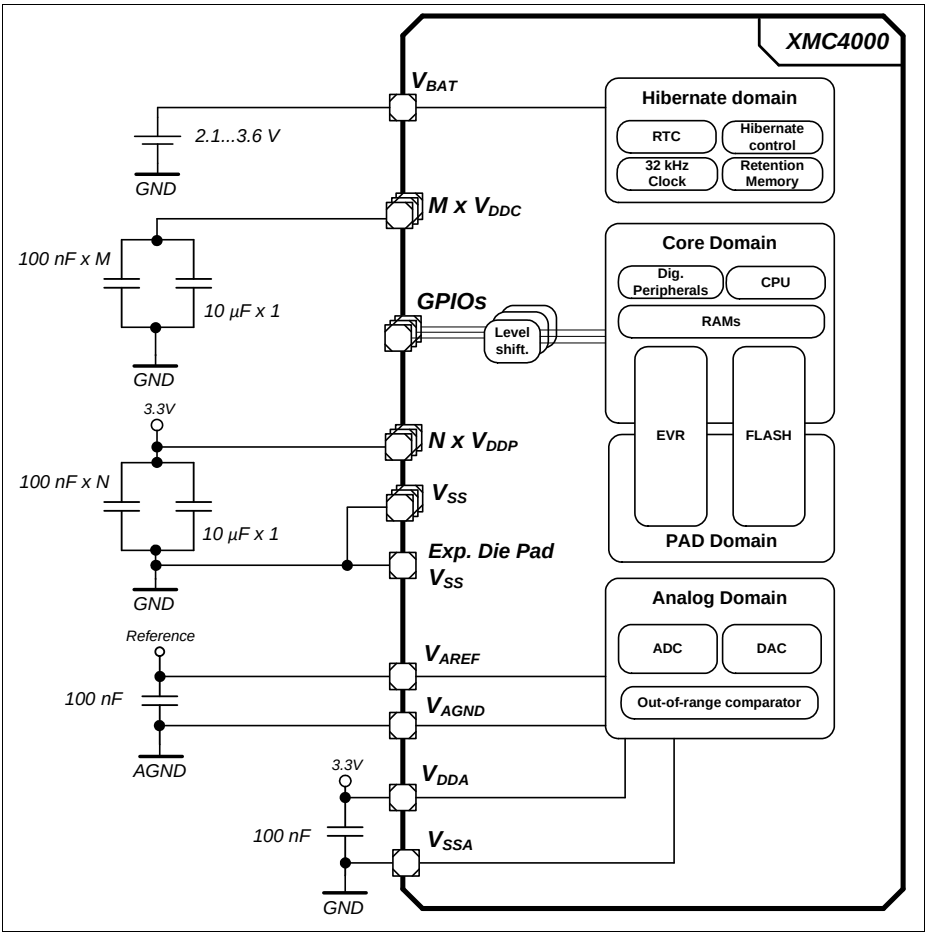

Figure 9 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 10 uF capacitor to the V_{DDC} nets.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$ 7)
Differential Non-Linearity Error 8)	EA_{DNL} CC	-3	–	3	LSB	
Gain Error 8)	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity 8)	EA_{INL} CC	-3	–	3	LSB	
Offset Error 8)	EA_{OFF} CC	-4	–	4	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion 5)	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA} 9)
ON resistance of the analog input path	R_{AIN} CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 16**).

4) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from V_{AREF}/2.

5) Applies to AINx, when used as alternate reference input.

6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.

7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.

8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 459 ns results in a typical average current of I_{AREF} = 65.4 µA.

Table 38 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 144 MHz, main PLL f_{VCO} = 288 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 72 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 4 - 3 - 2)
24 MHz - 48 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 3 - 2)
24 MHz - 72 MHz - 144 MHz (K2 steps 12 - 4 - 2)

3.3.5 Internal Clock Source Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Fast Internal Clock Source

Table 40 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V ≤ V_{DDP} ≤ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

Slow Internal Clock Source

Table 41 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	V_{BAT} = const. 0 °C ≤ T_A ≤ 85 °C
		-5	–	5	%	V_{BAT} = const. T_A < 0 °C or T_A > 85 °C
		-5	–	5	%	2.4 V ≤ V_{BAT}, T_A = 25 °C
		-10	–	10	%	1.95 V ≤ V_{BAT} < 2.4 V, T_A = 25 °C
Start-up time	t_{OSIS} CC	–	50	–	µs	

3.3.9 Peripheral Timing

3.3.9.1 Delta-Sigma Demodulator Digital Interface Timing

The following parameters are applicable for the digital interface of the Delta-Sigma Demodulator (DSD).
The data timing is relative to the active clock edge. Depending on the operation mode of the connected modulator that can be the rising and falling clock edge.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 45 DSD Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MCLK period in master mode	t_1	CC	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in master mode	t_2	CC	9	–	–	ns	$t_2 > t_{PERIPH}$ [1]
MCLK low time in master mode	t_3	CC	9	–	–	ns	$t_3 > t_{PERIPH}$ [1]
MCLK period in slave mode	t_1	SR	33.3	–	–	ns	$t_1 \geq 4 \times t_{PERIPH}$ [1]
MCLK high time in slave mode	t_2	SR	t_{PERIPH}	–	–	ns	[1]
MCLK low time in slave mode	t_3	SR	t_{PERIPH}	–	–	ns	[1]
DIN input setup time to the active clock edge	t_4	SR	t_{PERIPH} + 4	–	–	ns	[1]
DIN input hold time from the active clock edge	t_5	SR	t_{PERIPH} + 3	–	–	ns	[1]

1) $t_{PERIPH} = 1 / f_{PERIPH}$

High-Speed Input Path (Read)

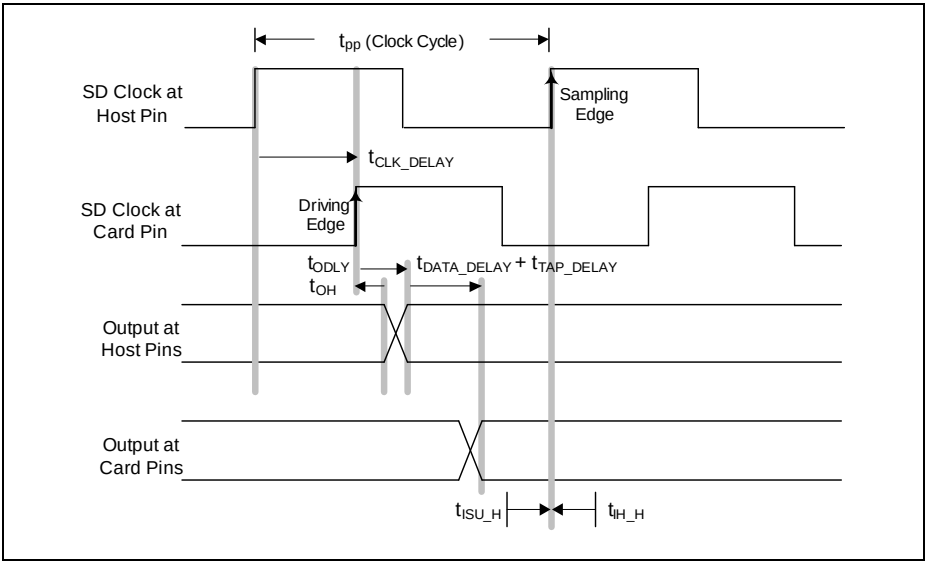

Figure 40 High-Speed Input Path

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(11)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_H} < t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{pp} - t_{ODLY} - t_{ISU\_H} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

Write Timing

Table 58 Asynchronous Write Timing, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:0) output delay	to RD/$\overline{WR}$ rising edge, deviation from the ideal programmed value.	CC	t_{30}	-2.5	2.5	ns
A(24:0) output delay		CC	t_{31}	-2.5	2.5	
$\overline{CS}$ rising edge		CC	t_{32}	-2	2	
$\overline{ADV}$ rising edge		CC	t_{33}	-2	4.5	
$\overline{BC}$ rising edge		CC	t_{34}	-2.5	2	
$\overline{WAIT}$ input setup		SR	t_{35}	12	–	
$\overline{WAIT}$ input hold		SR	t_{36}	0	–	
Data output delay		CC	t_{37}	-5.5	2	
Data output delay		CC	t_{38}	-5.5	2	
RD / $\overline{WR}$ output delay		CC	t_{39}	-2.5	1.5	

Demultiplexed Write Timing

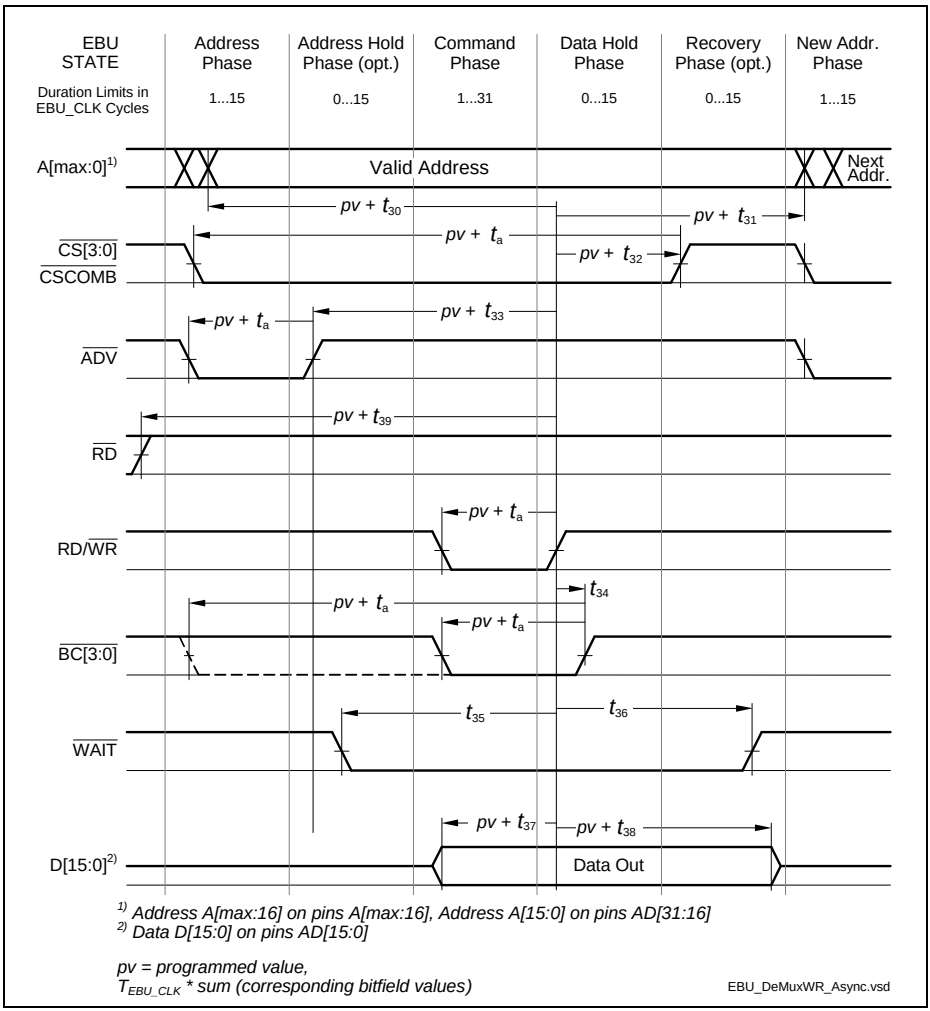

Figure 44 Demultiplexed Write Access

3.3.10.2 EBU Burst Mode Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and C_L = 16 pF.

Table 59 EBU Burst Mode Read / Write Access Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_{10}	CC	-2	–	2	ns	–
$\overline{RD}$ and RD/$\overline{WR}$ active/inactive after BFCLKO active edge[1]	t_{12}	CC	-2	–	2	ns	–
$\overline{CS}$x output delay from BFCLKO active edge[1]	t_{21}	CC	-2.5	–	1.5	ns	–
$\overline{ADV}$ active/inactive after BFCLKO active edge[2]	t_{22}	CC	-2	–	2	ns	–
$\overline{BAA}$ active/inactive after BFCLKO active edge[2]	t_{22a}	CC	-2.5	–	1.5	ns	–
Data setup to BFCLKI rising edge[3]	t_{23}	SR	3	–	–	ns	–
Data hold from BFCLKI rising edge[3]	t_{24}	SR	0	–	–	ns	–
$\overline{WAIT}$ setup (low or high) to BFCLKI rising edge[3]	t_{25}	SR	3	–	–	ns	–
$\overline{WAIT}$ hold (low or high) from BFCLKI rising edge[3]	t_{26}	SR	0	–	–	ns	–

1) An active edge can be a rising or falling edge, depending on the settings of bits BFCON.EBSE / ECSE and the clock divider ratio.
Negative minimum values for these parameters mean that the last data read during a burst may be corrupted. However, with clock feedback enabled, this value is an oversampling not required for the internal bus transaction, and will be discarded.

2) This parameter is valid for BUSCONx.EBSE = 1 and BUSAPx.EXTCLK = 00_B.
For BUSCONx.EBSE = 1 and other values of BUSAPx.EXTCLK, ADV and BAA will be delayed by 1/2 of the internal bus clock period $T_{CPU} = 1 / f_{CPU}$.
For BUSCONx. EBSE = 0 and BUSAPx.EXTCLK = 11_B, add 2 internal bus clock periods.
For BUSCONx. EBSE = 0 and other values of BUSAPx.EXTCLK, add 1 internal bus clock period.

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS}}$(3:0) low		CC	t_8	–	9	
$\overline{\text{CS}}$(3:0) high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC}}$(3:0) low		CC	t_{16}	–	9	
$\overline{\text{BC}}$(3:0) high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1)]		CC	t_{22}	–	7	
CKE output hold[1)]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 63 USB Timing Parameters (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	t_R	CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F	CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F	CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS}	CC	1.3	–	2.0	V	C_L = 50 pF

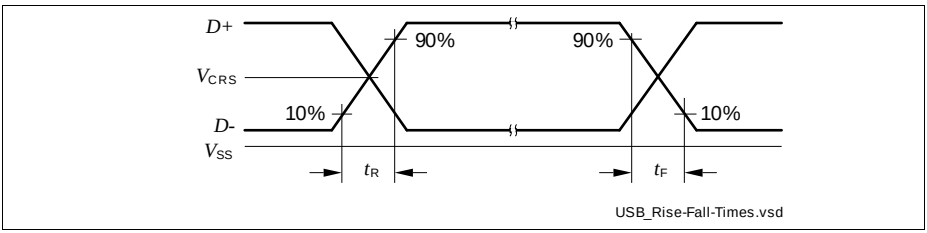

Figure 50 USB Signal Timing

Table 68 ETH MII TX Signal Timing Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PHY setup requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_setup} SR	15	–	0	ns	PHY dependent IEEE802.3 limit is 15 ns
PHY hold requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_hold} CC	0	–	25	ns	PHY dependent IEEE802.3 limit is 0 ns

Note: ECAT0_CONPx.TX_SHIFT can be adjusted by displaying TX_CLK of a PHY and TXEN/TXD[3:0] on an oscilloscope. TXEN/TXD[3:0] is allowed to change between 0 ns and 25 ns after a rising edge of TX_CLK (according to IEEE802.3 – check your PHY's documentation). Configure TX_SHIFT so that TXEN/TXD[3:0] change near the middle of this range. It is sufficient to check just one of the TXEN/TXD[3:0] signals, because they are nearly generated at the same time.

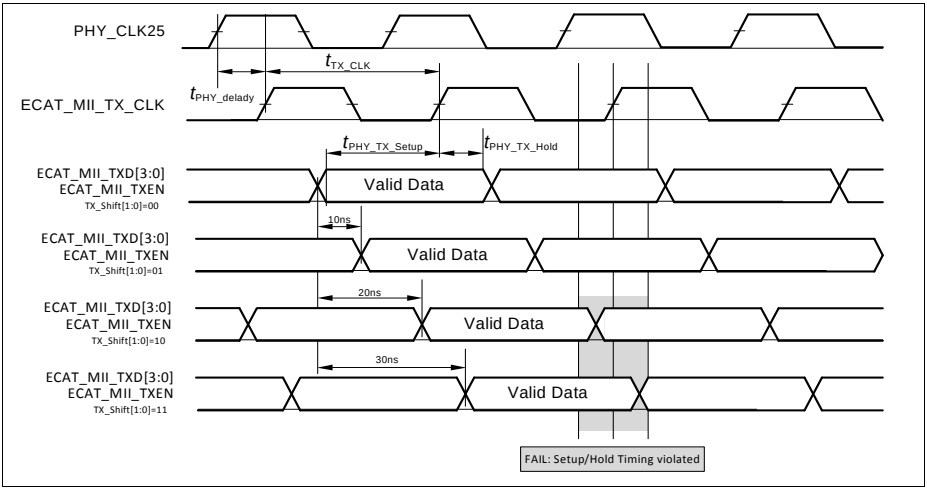

Figure 57 MII TX Characteristics