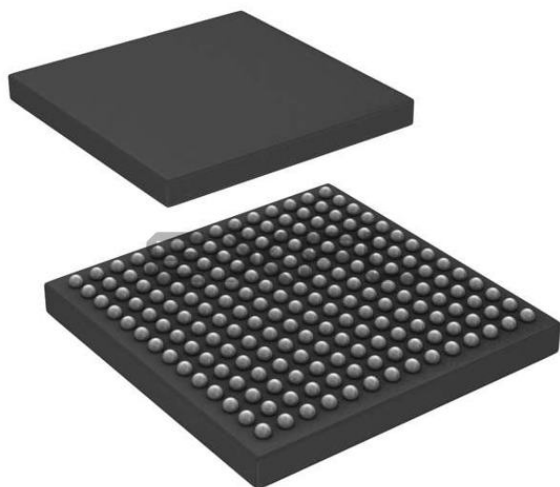




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I ² S, LED, POR, Touch-Sense, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	352K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	PG-LFBGA-196-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4700e196k2048aaxqma1

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

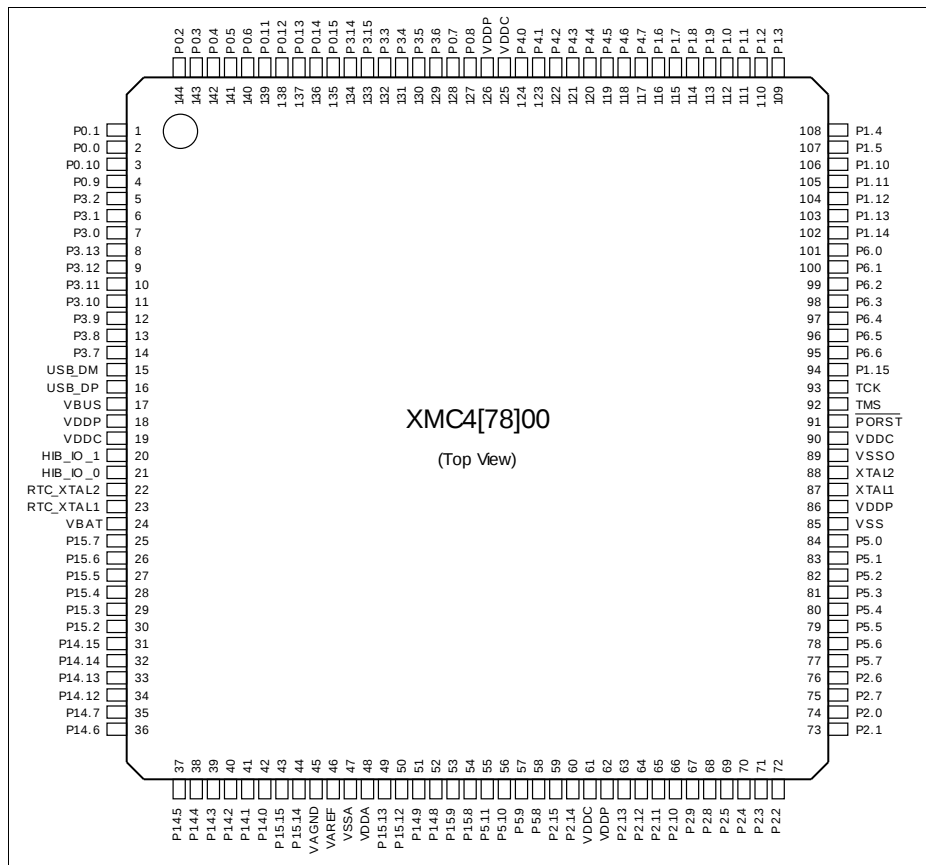


Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)

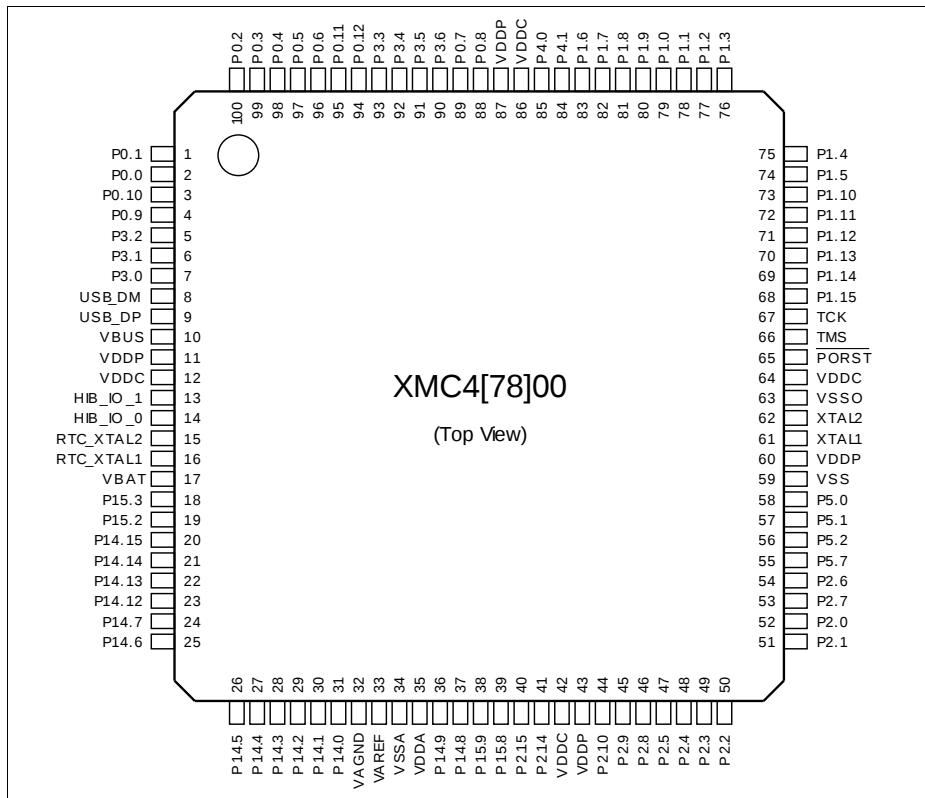


Figure 7 XMC4[78]00 PG-LQFP-100 Pin Configuration (top view)

General Device Information
Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P2.10	N8	66	44	A2	
P2.11	P8	65	-	A2	
P2.12	N7	64	-	A2	
P2.13	P7	63	-	A2	
P2.14	M7	60	41	A2	
P2.15	L6	59	40	A2	
P3.0	E1	7	7	A2	
P3.1	D2	6	6	A2	
P3.2	D3	5	5	A2	
P3.3	H7	132	93	A1+	
P3.4	G7	131	92	A1+	
P3.5	D6	130	91	A2	
P3.6	C7	129	90	A2	
P3.7	G4	14	-	A1+	
P3.8	G3	13	-	A1+	
P3.9	H5	12	-	A1+	
P3.10	H6	11	-	A1+	
P3.11	F3	10	-	A1+	
P3.12	F2	9	-	A2	
P3.13	E2	8	-	A2	
P3.14	F6	134	-	A1+	
P3.15	F7	133	-	A1+	
P4.0	D8	124	85	A2	
P4.1	C9	123	84	A2	
P4.2	G8	122	-	A1+	
P4.3	H8	121	-	A1+	
P4.4	E7	120	-	A1+	
P4.5	F8	119	-	A1+	
P4.6	E8	118	-	A1+	
P4.7	E9	117	-	A1+	
P5.0	K9	84	58	A1+	
P5.1	K8	83	57	A1+	
P5.2	K7	82	56	A1+	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs								
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input
P6.6	U0C0. DOUT0		DSD. MCLK3	ECAT0. P0_TXD3	DB. ETM_TRACEDA TA0	EBU. BC3			DSD. MCLK3A	ETH0. CLK_TXB		CAN. N3_RXDB			
P7.0		CAN. N3_TXD		ECAT0. P0_TXD0	EBU. A19										
P7.1				ECAT0. P0_TXD1	EBU. A20					CAN. N3_RXDC					
P7.2		CAN. N4_TXD		ECAT0. P0_TXD2	EBU. A21										
P7.3				ECAT0. P0_TXD3	EBU. A22					CAN. N4_RXDC					
P7.4			CCU42. OUT0						ECAT0. P0_RXD0C						
P7.5			CCU42. OUT1						ECAT0. P0_RXD1C						
P7.6			CCU42. OUT2						ECAT0. P0_RXD2C						
P7.7			CCU42. OUT3						ECAT0. P0_RXD3C						
P7.8		CAN. N5_TXD		ECAT0. P0_TX_ENA	DB. ETM_TRACECLK										
P7.9			CCU80. OUT22						ECAT0. P0_RX_ERRC						
P7.10			CCU80. OUT32						ECAT0. P0_RX_CLKC						
P7.11			CCU80. OUT33						ECAT0. P0_RX_DVC						
P8.0				ECAT0. P1_TXD0	DB. ETM_TRACEDA TA0					CAN. N5_RXDC					
P8.1				ECAT0. P1_TXD1	DB. ETM_TRACEDA TA1					U0C0. DX2C					
P8.2				ECAT0. P1_TXD2	DB. ETM_TRACEDA TA2										
P8.3				ECAT0. P1_TXD3	DB. ETM_TRACEDA TA3					U0C0. DX1C					
P8.4		U0C0. SEL01							ECAT0. P1_RXD0C						
P8.5		U0C0. SCLKOUT							ECAT0. P1_RXD1C						
P8.6		U0C0. SEL00							ECAT0. P1_RXD2C						
P8.7		U0C0. DOUT8							ECAT0. P1_RXD3C						
P8.8				ECAT0. P1_TX_ENA						U0C0. DX0E					

Electrical Parameters
Table 22 Standard Pads Class_A1+

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Output high voltage, POD ¹⁾ = weak	V _{OHA1+} CC	V _{DDP} - 0.4	—	V	I _{OH} ≥ -400 μA
		2.4	—	V	I _{OH} ≥ -500 μA
Output high voltage, POD ¹⁾ = medium		V _{DDP} - 0.4	—	V	I _{OH} ≥ -1.4 mA
		2.4	—	V	I _{OH} ≥ -2 mA
Output high voltage, POD ¹⁾ = strong		V _{DDP} - 0.4	—	V	I _{OH} ≥ -1.4 mA
		2.4	—	V	I _{OH} ≥ -2 mA
Output low voltage	V _{OLA1+} CC	—	0.4	V	I _{OL} ≤ 500 μA; POD ¹⁾ = weak
		—	0.4	V	I _{OL} ≤ 2 mA; POD ¹⁾ = medium
		—	0.4	V	I _{OL} ≤ 2 mA; POD ¹⁾ = strong
Fall time	t _{FA1+} CC	—	150	ns	C _L = 20 pF; POD ¹⁾ = weak
		—	50	ns	C _L = 50 pF; POD ¹⁾ = medium
		—	28	ns	C _L = 50 pF; POD ¹⁾ = strong; edge = slow
		—	16	ns	C _L = 50 pF; POD ¹⁾ = strong; edge = soft;
Rise time	t _{RA1+} CC	—	150	ns	C _L = 20 pF; POD ¹⁾ = weak
		—	50	ns	C _L = 50 pF; POD ¹⁾ = medium
		—	28	ns	C _L = 50 pF; POD ¹⁾ = strong; edge = slow
		—	16	ns	C _L = 50 pF; POD ¹⁾ = strong; edge = soft

1) POD = Pin Out Driver

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage ⁵⁾	V_{AREF} SR	$V_{AGND} + 1$	–	$V_{DDA} + 0.05^{1)}$	V	
Analog reference ground ⁵⁾	V_{AGND} SR	$V_{SSM} - 0.05$	–	$V_{AREF} - 1$	V	
Analog reference voltage range ²⁾⁵⁾	$V_{AREF} - V_{AGND}$ SR	1	–	$V_{DDA} + 0.1$	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs ³⁾	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0 \text{ V} \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	μA	$0 \text{ V} \leq V_{AREF} \leq V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	μA	$0 \text{ V} \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	36	MHz	$V_{DDA} = 3.3 \text{ V}$
Switched capacitance at the analog voltage inputs ⁴⁾	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input ⁵⁾⁶⁾	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs ⁵⁾	$C_{AREFTOT}$ CC	–	20	40	pF	

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 30 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
VBUS input voltage range	V_{IN}	CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1}	CC	4.4	–	–	V	
A-device session valid threshold	V_{B2}	CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3}	CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4}	CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN}	CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU}	CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD}	CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU}	CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN}	CC	–	–	150	μA	$0\text{ V} \leq V_{IN} \leq 5.25\text{ V}$: $T_{AVG} = 1\text{ ms}$

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 36 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page ¹⁾	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	$t_{\text{FL_ErSusp}}$ CC	–	–	15	ms	
Wait time after margin change	$t_{\text{FL_Margin Del}}$ CC	10	–	–	μs	
Wake-up time	t_{WU} CC	–	–	270	μs	
Read access time	t_{a} CC	22	–	–	ns	For operation with $1 / f_{\text{CPU}} < t_{\text{a}}$ wait states must be configured ²⁾
Data Retention Time, Physical Sector ³⁾⁴⁾	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector ³⁾⁴⁾	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB) ³⁾⁴⁾	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	Cycling distributed over life time ⁵⁾

Electrical Parameters

- 1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.
- 2) The following formula applies to the wait state configuration: $FCON.WSPFLASH \times (1 / f_{CPU}) \geq t_a$.
- 3) Storage and inactive time included.
- 4) Values given are valid for an average weighted junction temperature of $T_j = 110^{\circ}\text{C}$.
- 5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

Slow Internal Clock Source
Table 41 Slow Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OSI} CC	–	32.768	–	kHz	
Accuracy	Δf_{OSI} CC	-4	–	4	%	$V_{BAT} = \text{const.}$ $0\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$
		-5	–	5	%	$V_{BAT} = \text{const.}$ $T_A < 0\text{ }^{\circ}\text{C}$ or $T_A > 85\text{ }^{\circ}\text{C}$
		-5	–	5	%	$2.4\text{ V} \leq V_{BAT}$, $T_A = 25\text{ }^{\circ}\text{C}$
		-10	–	10	%	$1.95\text{ V} \leq V_{BAT} < 2.4\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$
Start-up time	t_{OSIS} CC	–	50	–	μs	

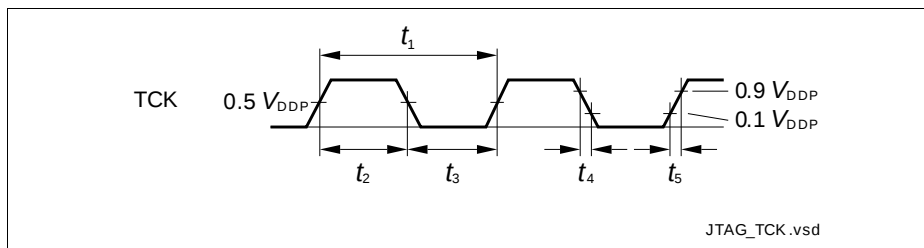


Figure 27 Test Clock Timing (TCK)

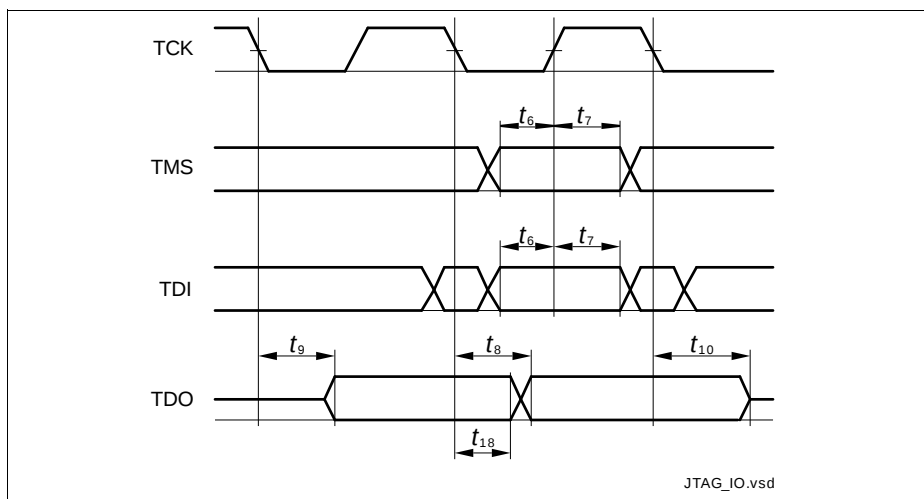


Figure 28 JTAG Timing

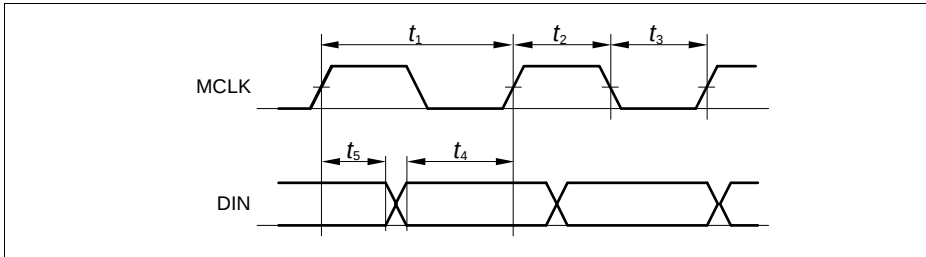


Figure 32 DSD Data Timing

3.3.9.2 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 46 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK} CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	$t_{PB} - 6.5^{1)}$	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	$t_{PB} - 8.5^{1)}$	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	1	–	–	ns	

1) $t_{PB} = 1 / f_{PB}$

Table 49 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + $0.1 \cdot C_b$ ²⁾	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + $0.1 \cdot C_b$ ²⁾	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

3.3.9.5 SDMMC Interface Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, total external capacitive load $C_L = 40$ pF.

AC Timing Specifications (Full-Speed Mode)

Table 52 SDMMC Timing for Full-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in full speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	24	MHz	
Clock cycle in full speed transfer mode	t_{pp}	CC	40	–	ns	
Clock low time	t_{WL}	CC	10	–	ns	
Clock high time	t_{WH}	CC	10	–	ns	
Clock rise time	t_{TLH}	CC	–	10	ns	
Clock fall time	t_{THL}	CC	–	10	ns	
Inputs setup to clock rising edge	t_{ISU_F}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_F}	SR	2	–	ns	
Outputs valid time in full speed mode	t_{ODLY_F}	CC	–	10	ns	
Outputs hold time in full speed mode	t_{OH_F}	CC	0	–	ns	

Table 53 SD Card Bus Timing for Full-Speed Mode¹⁾

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	5	–	ns	
SD card input hold time	t_{IH}	5	–	ns	

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(6)

$$t_{\text{CLK_DELAY}} + t_{\text{OH}} + t_{\text{DATA_DELAY}} + t_{\text{TAP_DELAY}} > t_{\text{IH_F}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > t_{\text{IH_F}} - t_{\text{OH}} - t_{\text{TAP_DELAY}}$$

$$t_{\text{CLK_DELAY}} + t_{\text{DATA_DELAY}} > 2 - t_{\text{TAP_DELAY}}$$

The data + clock delay must be greater than 2 ns if $t_{\text{TAP_DELAY}}$ is not used.

If the $t_{\text{TAP_DELAY}}$ is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 54 SDMMC Timing for High-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in high speed transfer mode ($1/t_{\text{pp}}$)	f_{pp}	CC	0	48	MHz	
Clock cycle in high speed transfer mode	t_{pp}	CC	20	–	ns	
Clock low time	t_{WL}	CC	7	–	ns	
Clock high time	t_{WH}	CC	7	–	ns	
Clock rise time	t_{TLH}	CC	–	3	ns	
Clock fall time	t_{THL}	CC	–	3	ns	
Inputs setup to clock rising edge	$t_{\text{ISU_H}}$	SR	2	–	ns	
Inputs hold after clock rising edge	$t_{\text{IH_H}}$	SR	2	–	ns	
Outputs valid time in high speed mode	$t_{\text{ODLY_H}}$	CC	–	14	ns	
Outputs hold time in high speed mode	$t_{\text{OH_H}}$	CC	2	–	ns	

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{CLK_DELAY} + t_{OH} + t_{DATA_DELAY} + t_{TAP_DELAY} > t_{IH_H}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} > t_{IH_H} - t_{OH} - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} > 2 - 2,5 - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} > -0,5 - t_{TAP_DELAY}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3.3.10 EBU Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16$ pF.

3.3.10.1 EBU Asynchronous Timing

Note: For each timing, the accumulated PLL jitter must be added separately.

Table 56 Common Timing Parameters for all Asynchronous Timings

Parameter		Symbol	Limit Values		Unit	Edge Setting
			Min.	Max.		
Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. $C_L = 16$ pF.	CC	t_a	-1	1.5	ns	sharp
			-2	1		medium
AD(24:16) output delay	to ADV rising edge, multiplexed read / write	CC t_{13}	-5.5	2		—
AD(24:16) output delay		CC t_{14}	-5.5	2		—

Write Timing

Table 58 Asynchronous Write Timing, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:0) output delay	to RD/ $\overline{\text{WR}}$ rising edge, deviation from the ideal programmed value.	CC	t_{30}	-2.5	2.5	ns
A(24:0) output delay		CC	t_{31}	-2.5	2.5	
$\overline{\text{CS}}$ rising edge		CC	t_{32}	-2	2	
$\overline{\text{ADV}}$ rising edge		CC	t_{33}	-2	4.5	
$\overline{\text{BC}}$ rising edge		CC	t_{34}	-2.5	2	
$\overline{\text{WAIT}}$ input setup		SR	t_{35}	12	–	
$\overline{\text{WAIT}}$ input hold		SR	t_{36}	0	–	
Data output delay		CC	t_{37}	-5.5	2	
Data output delay		CC	t_{38}	-5.5	2	
RD / $\overline{\text{WR}}$ output delay		CC	t_{39}	-2.5	1.5	

Electrical Parameters

- 3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, t_5 , t_6 , t_7 and t_8 from the asynchronous timing apply.

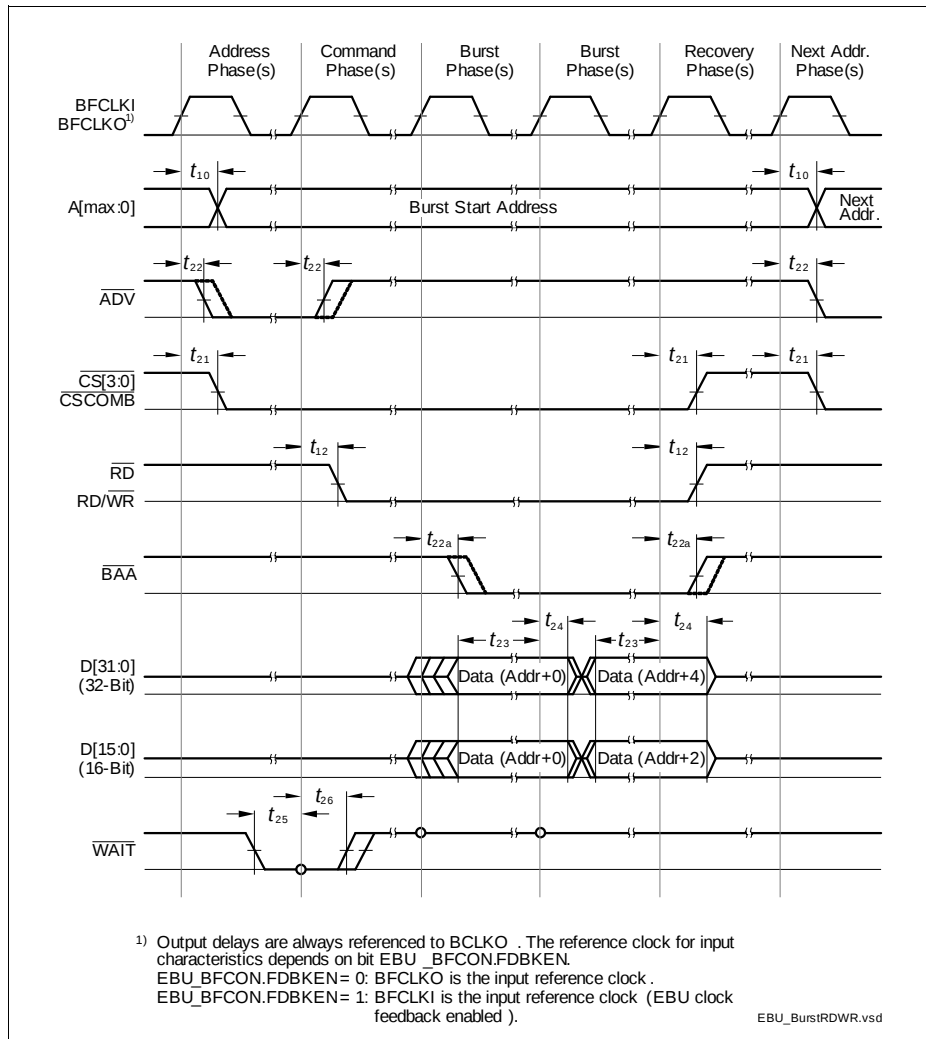


Figure 45 EBU Burst Mode Read / Write Access Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 65 ETH MII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7	SR	400	–	–	ns	$C_L = 25 \text{ pF}$
Clock high time, 10 Mbps	t_8	SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9	SR	140	–	260	ns	
Clock period, 100 Mbps	t_7	SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8	SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9	SR	14	–	26	ns	
Input setup time	t_{10}	SR	10	–	–	ns	
Input hold time	t_{11}	SR	10	–	–	ns	
Output valid time	t_{12}	CC	0	–	25	ns	

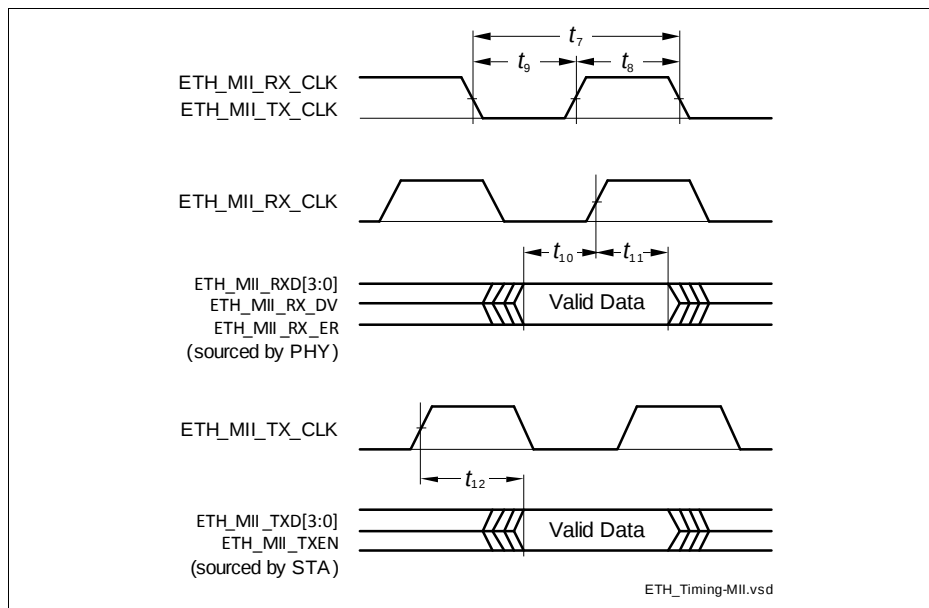


Figure 53 ETH MII Signal Timing

Table 68 **ETH MII TX Signal Timing Parameters (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PHY setup requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_setup} SR	15	—	0	ns	PHY dependent IEEE802.3 limit is 15 ns
PHY hold requirement: TXEN/TXD[3:0] with respect to TX_CLK	t_{TX_hold} CC	0	—	25	ns	PHY dependent IEEE802.3 limit is 0 ns

Note: ECAT0_CONPx.TX_SHIFT can be adjusted by displaying TX_CLK of a PHY and TXEN/TXD[3:0] on an oscilloscope. TXEN/TXD[3:0] is allowed to change between 0 ns and 25 ns after a rising edge of TX_CLK (according to IEEE802.3 – check your PHY's documentation). Configure TX_SHIFT so that TXEN/TXD[3:0] change near the middle of this range. It is sufficient to check just one of the TXEN/TXD[3:0] signals, because they are nearly generated at the same time.

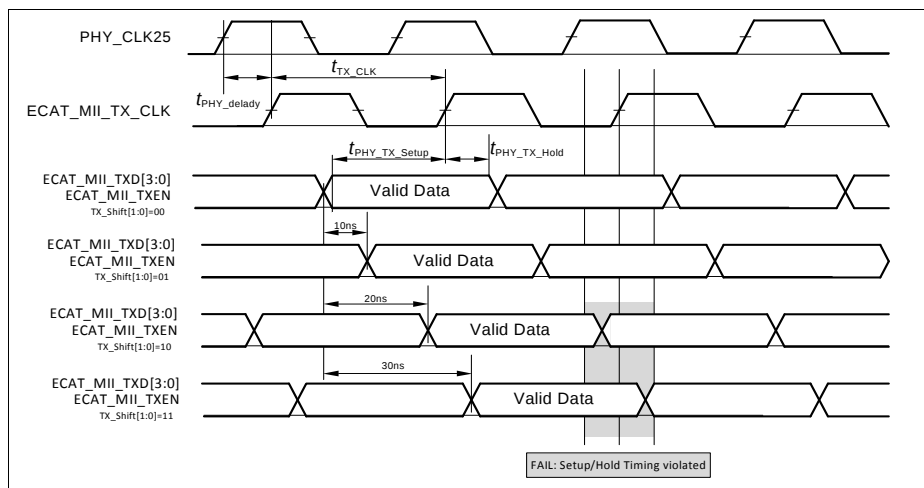


Figure 57 **MII TX Characteristics**