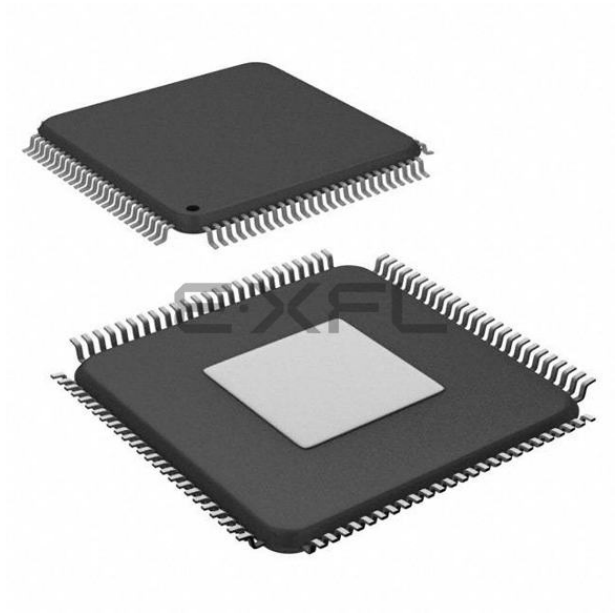
Infineon Technologies - XMC4700F100F1536AAXQMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	75
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-25
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4700f100f1536aaxqma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

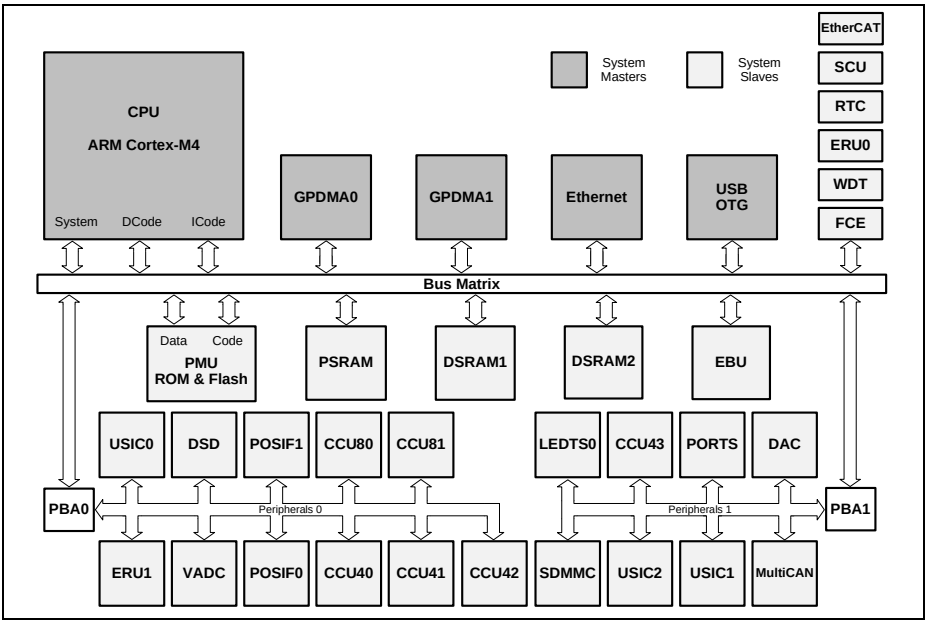

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

Table 2 Features of XMC4[78]00 Device Types (cont'd)

Derivative[1]	LEDTS Intf.	SDMMC Intf.	EBU Intf.[2]	ETH Intf.[3]	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4800-E196x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x2048	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1536	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1024	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]

1) x is a placeholder for the supported temperature range.

2) Memory types supported S=SDRAM, D=DEMUX, M=MUX 16-bit and 32-bit, M16=MUX 16-bit

3) Supported interfaces, M=MII, R=RMII.

Table 3 Features of XMC4[78]00 Device Types

Derivative[1]	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4700-E196x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4700-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x2048	32	4	2	4 x 4	2 x 4	2

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.11	G5	139	95	A1+	
P0.12	F5	138	94	A1+	
P0.13	E5	137	-	A1+	
P0.14	G6	136	-	A1+	
P0.15	E6	135	-	A1+	
P1.0	F9	112	79	A1+	
P1.1	G9	111	78	A1+	
P1.2	E11	110	77	A2	
P1.3	E12	109	76	A2	
P1.4	E10	108	75	A1+	
P1.5	F10	107	74	A1+	
P1.6	D9	116	83	A2	
P1.7	D10	115	82	A2	
P1.8	C10	114	81	A2	
P1.9	D11	113	80	A2	
P1.10	F12	106	73	A1+	
P1.11	F11	105	72	A1+	
P1.12	G11	104	71	A2	
P1.13	G12	103	70	A2	
P1.14	G10	102	69	A2	
P1.15	J12	94	68	A2	
P2.0	L11	74	52	A2	
P2.1	M12	73	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	M11	72	50	A2	
P2.3	N11	71	49	A2	
P2.4	N10	70	48	A2	
P2.5	P10	69	47	A2	
P2.6	L9	76	54	A1+	
P2.7	M9	75	53	A1+	
P2.8	N9	68	46	A2	
P2.9	P9	67	45	A2	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
XTAL1									U0C0.DX0F	U0C1.DX0F	U1C0.DX0F	U1C1.DX0F	U2C0.DX0F	U2C1.DX0F		
XTAL2																
RTC_XTAL1											ERU0.1B1					
RTC_XTAL2																

3 Electrical Parameters

Attention: All parameters in this chapter are preliminary target values and may change based on characterization results.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[78]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[78]00 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[78]00 is designed in.

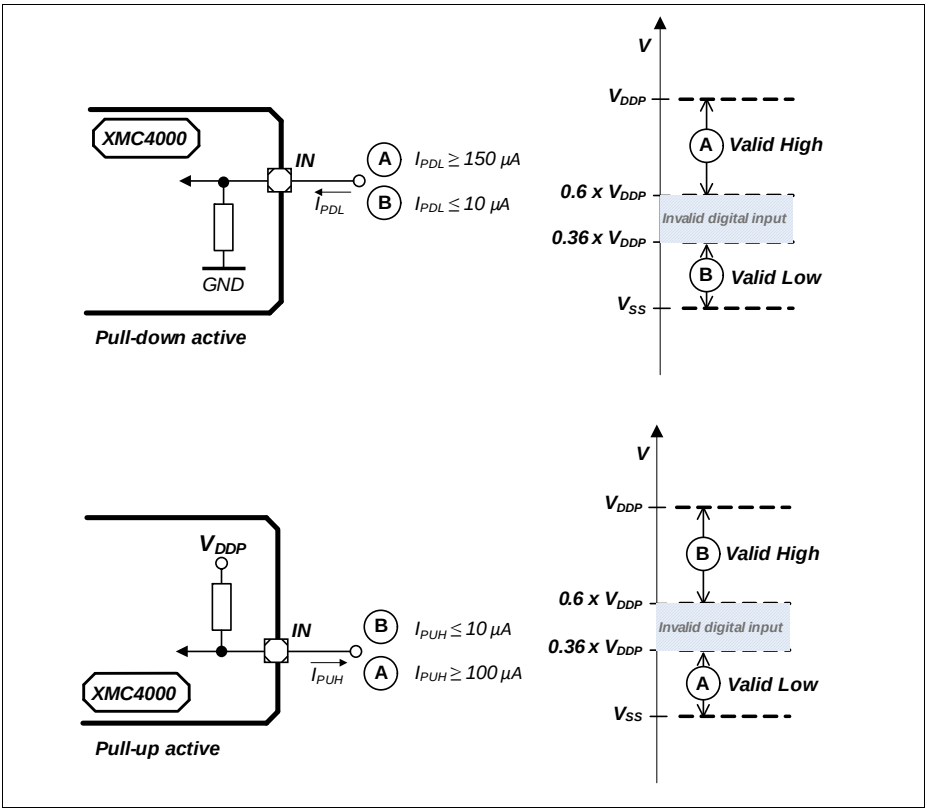

Figure 13 Pull Device Input Characteristics

Figure 13 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$ 7)
Differential Non-Linearity Error 8)	EA_{DNL} CC	-3	–	3	LSB	
Gain Error 8)	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity 8)	EA_{INL} CC	-3	–	3	LSB	
Offset Error 8)	EA_{OFF} CC	-4	–	4	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion 5)	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA} 9)
ON resistance of the analog input path	R_{AIN} CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 16**).

4) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from V_{AREF}/2.

5) Applies to AINx, when used as alternate reference input.

6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.

7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.

8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 459 ns results in a typical average current of I_{AREF} = 65.4 µA.

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	210	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	50	–	450	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	45	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

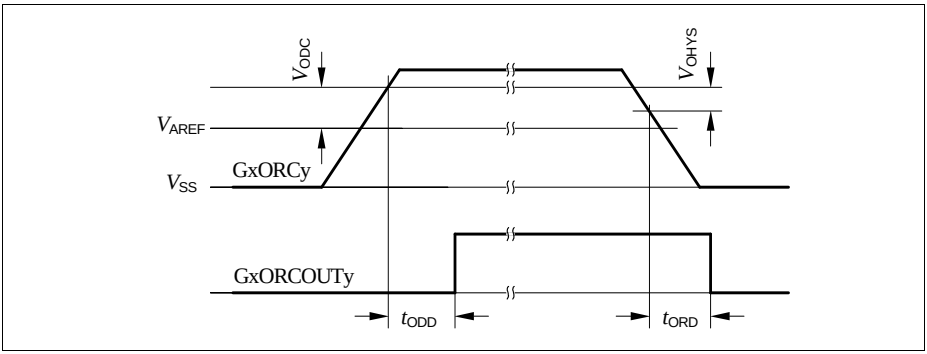

Figure 18 GxORCOUTy Trigger Generation

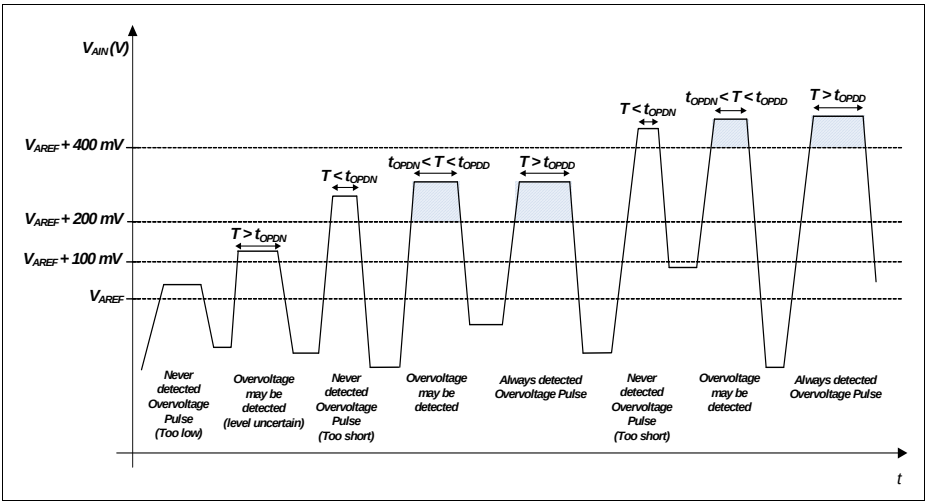

Figure 19 ORC Detection Ranges

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 34 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)11)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	135	–	mA	144 / 144 / 144
			–	125	–		144 / 72 / 72
			–	97	–		72 / 72 / 144
			–	80	–		24 / 24 / 24
			–	68	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA}	CC	–	108	–	mA	144 / 144 / 144
			–	98	–		144 / 72 / 72
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	86	–	mA	144 / 144 / 144
			–	85	–		144 / 72 / 72
			–	70	–		72 / 72 / 144
			–	55	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	127	–	mA	144 / 144 / 144
			–	115	–		144 / 72 / 72
			–	93	–		72 / 72 / 144
			–	57	–		24 / 24 / 24
			–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	48	–		100 / 100 / 100

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.
4) If t_{PR} is not met, low spikes on $\overline{PORST}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping V_{DDP}).

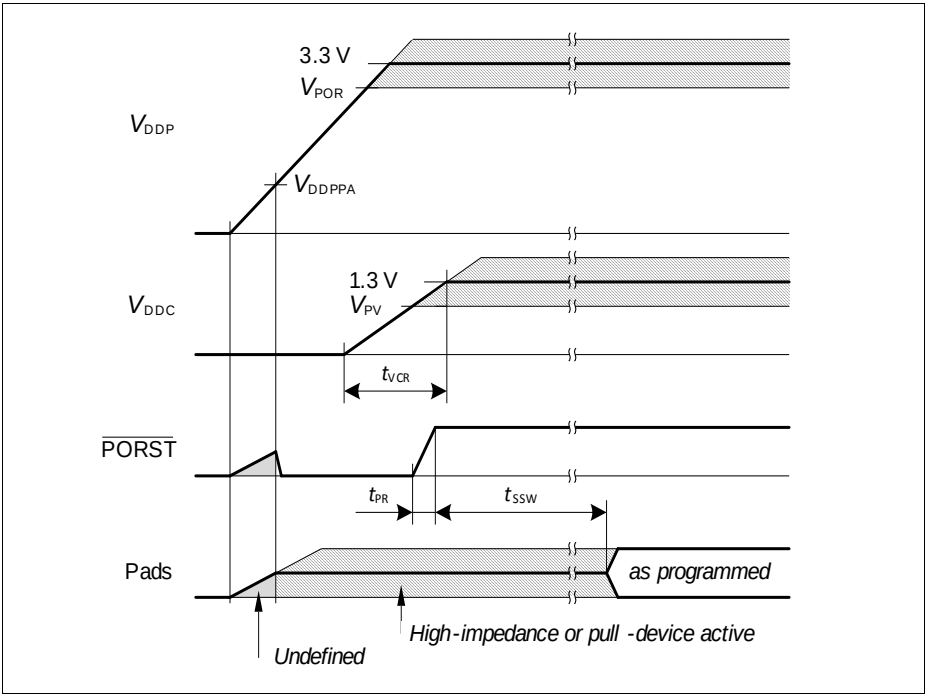

Figure 26 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 47 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

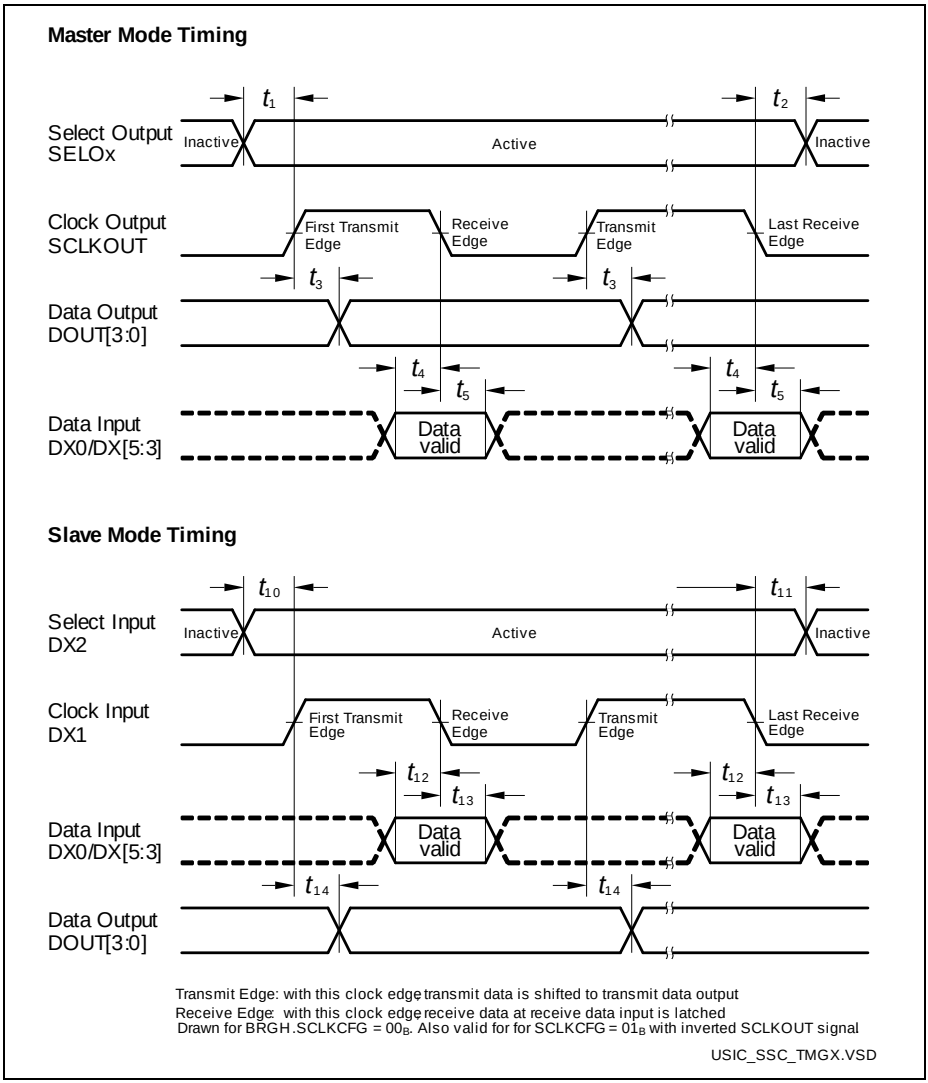

Figure 33 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

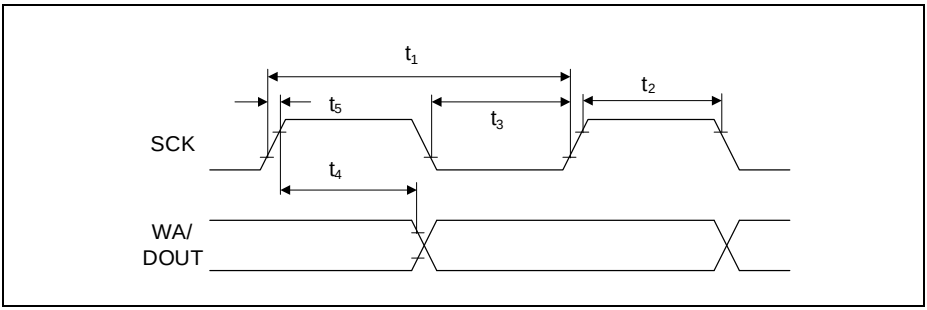

Figure 35 USIC IIS Master Transmitter Timing

Table 51 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock low time	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

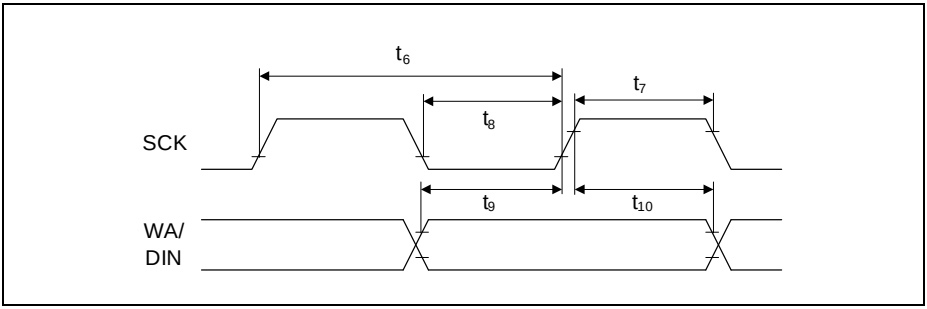

Figure 36 USIC IIS Slave Receiver Timing

Full-Speed Input Path (Read)

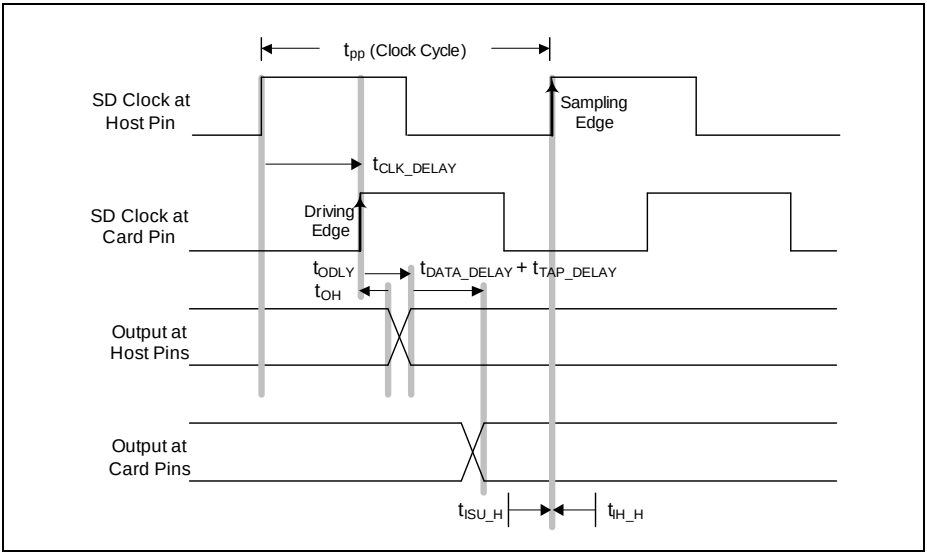

Figure 38 Full-Speed Input Path

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(5)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_F} < 0{,}5 \times t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 0{,}5 \times t_{pp} - t_{ODLY} - t_{ISU\_F} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Write Timing

Table 58 Asynchronous Write Timing, Multiplexed and Demultiplexed

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(24:0) output delay	to RD/$\overline{WR}$ rising edge, deviation from the ideal programmed value.	CC	t_{30}	-2.5	2.5	ns
A(24:0) output delay		CC	t_{31}	-2.5	2.5	
$\overline{CS}$ rising edge		CC	t_{32}	-2	2	
$\overline{ADV}$ rising edge		CC	t_{33}	-2	4.5	
$\overline{BC}$ rising edge		CC	t_{34}	-2.5	2	
$\overline{WAIT}$ input setup		SR	t_{35}	12	–	
$\overline{WAIT}$ input hold		SR	t_{36}	0	–	
Data output delay		CC	t_{37}	-5.5	2	
Data output delay		CC	t_{38}	-5.5	2	
RD / $\overline{WR}$ output delay		CC	t_{39}	-2.5	1.5	

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 64 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

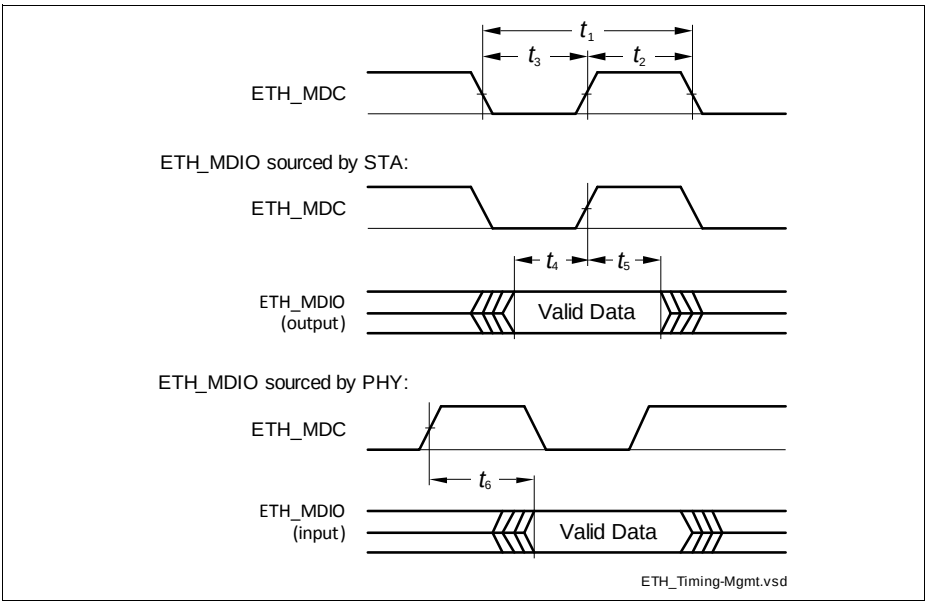

Figure 52 ETH Management Signal Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 65 ETH MII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7	SR	400	–	–	ns	C_L = 25 pF
Clock high time, 10 Mbps	t_8	SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9	SR	140	–	260	ns	
Clock period, 100 Mbps	t_7	SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8	SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9	SR	14	–	26	ns	
Input setup time	t_{10}	SR	10	–	–	ns	
Input hold time	t_{11}	SR	10	–	–	ns	
Output valid time	t_{12}	CC	0	–	25	ns	

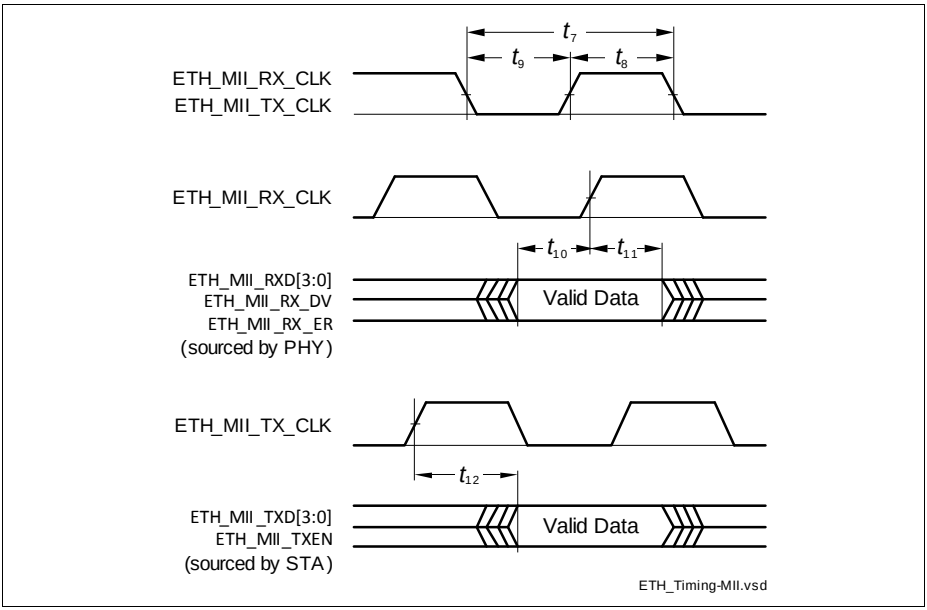

Figure 53 ETH MII Signal Timing

5 Quality Declarations

The qualification of the XMC4[78]00 is executed according to the JEDEC standard JESD47I.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 72 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	3 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	1 000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D