Infineon Technologies - XMC4700F144F1536AAXQMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	119
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-24
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4700f144f1536aaxqma1

On-Chip Memories

- 16 KB on-chip boot ROM
- 96 KB on-chip high-speed program memory
- 128 KB on-chip high speed data memory
- 128 KB on-chip high-speed communication memory
- 2,048 KB on-chip Flash Memory with 8 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- EtherCATSlave interface (ECAT) capable of 100 Mbit/s transfer rates with 2 MII ports, 8 Fieldbus Memory Management Units (FMMU), 8 Sync Manager, 64 bit distributed clocks
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 6 nodes, 256 message objects (MO), data rate up to 1 MBaud
- Six Universal Serial Interface Channels (USIC),providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability

Table 1 Synopsis of XMC4[78]00 Device Types (cont'd)

Derivative[1)]	Package	Flash Kbytes	SRAM Kbytes
XMC4700-F144x1536	PG-LQFP-144	1536	276
XMC4700-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x2048	PG-LFBGA-196	2048	352
XMC4800-F144x2048	PG-LQFP-144	2048	352
XMC4800-F100x2048	PG-LQFP-100	2048	352
XMC4800-E196x1536	PG-LFBGA-196	1536	276
XMC4800-F144x1536	PG-LQFP-144	1536	276
XMC4800-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x1024	PG-LFBGA-196	1024	200
XMC4800-F144x1024	PG-LQFP-144	1024	200
XMC4800-F100x1024	PG-LQFP-100	1024	200

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4[78]00 Device Types

Derivative[1)]	LEDTS Intf.	SDMMC Intf.	EBU Intf.[2)]	ETH Intf.[3)]	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4700-E196x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x2048	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-E196x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x1536	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

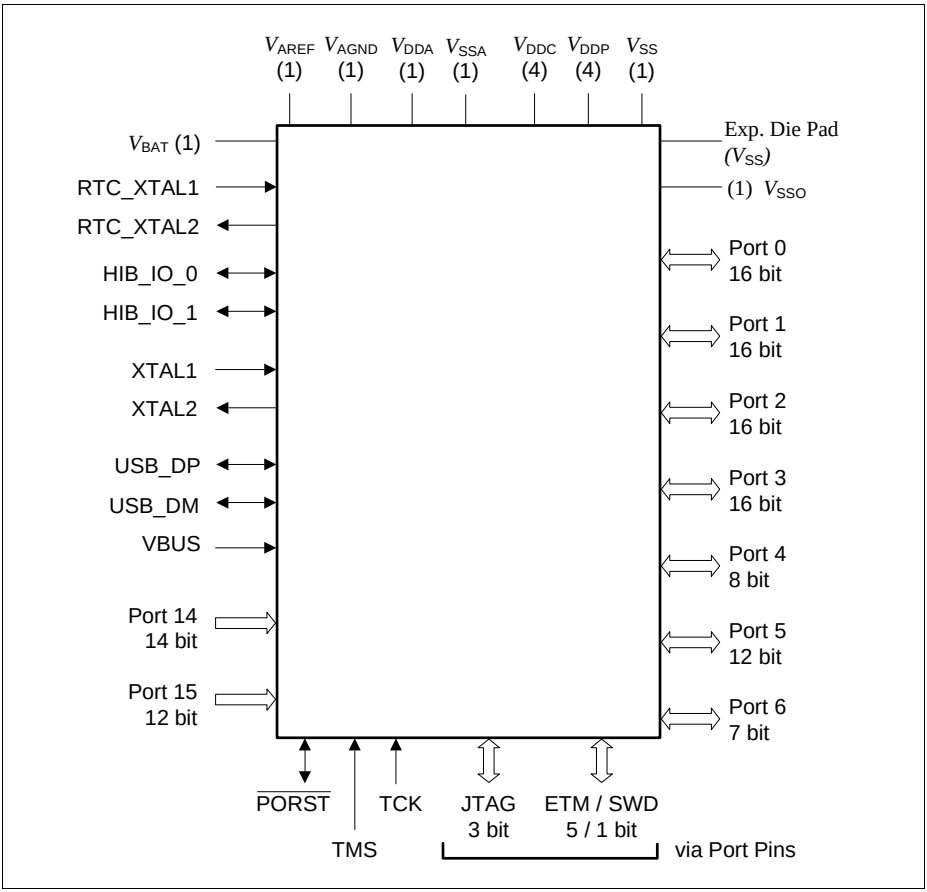


Figure 2 XMC4[78]00 Logic Symbol PG-LQFP-144

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

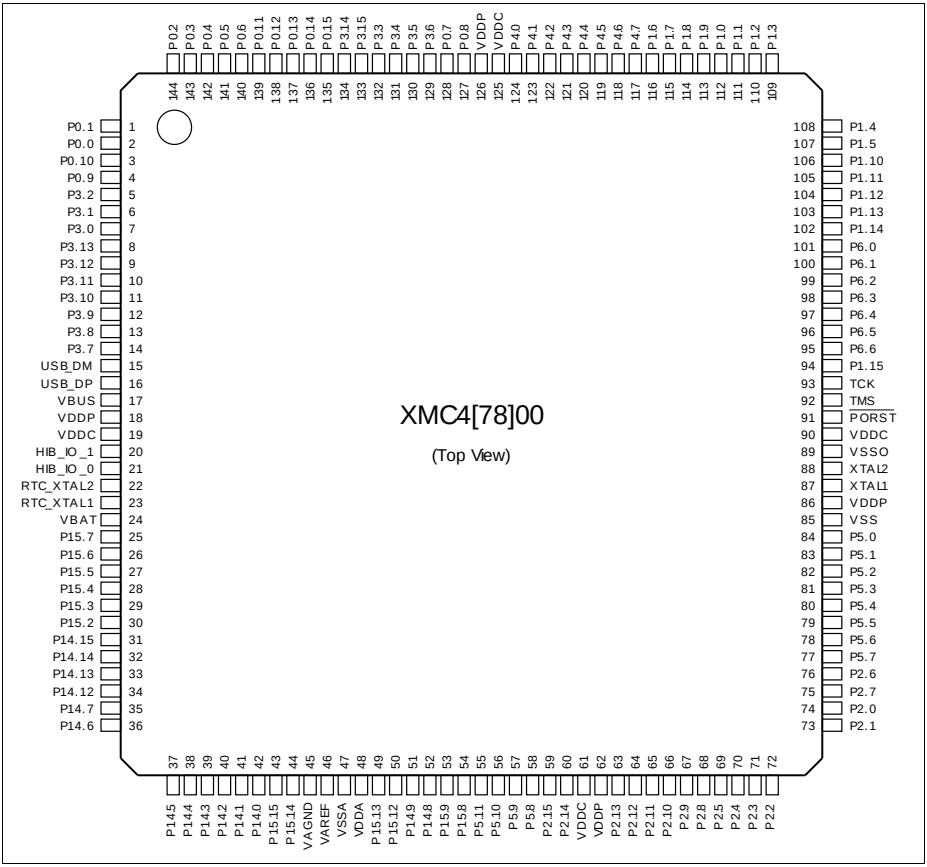
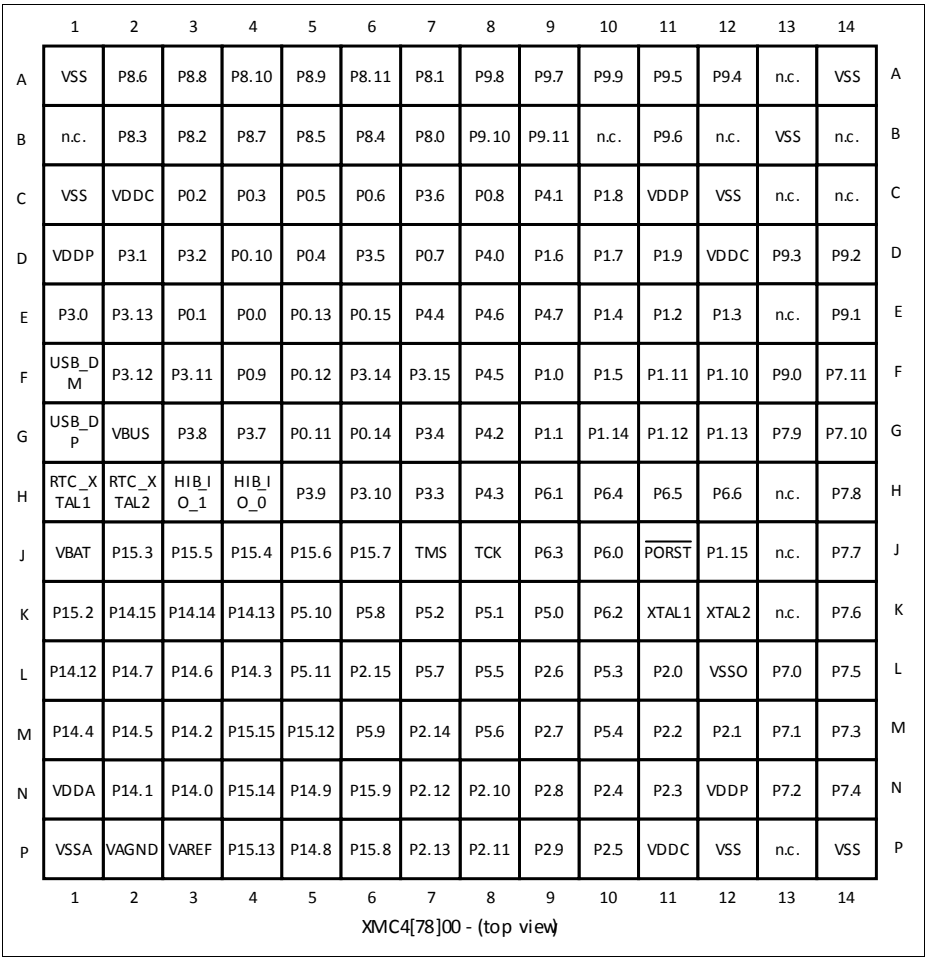


Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	P8.6	P8.8	P8.10	P8.9	P8.11	P8.1	P9.8	P9.7	P9.9	P9.5	P9.4	n.c.	VSS	A
B	n.c.	P8.3	P8.2	P8.7	P8.5	P8.4	P8.0	P9.10	P9.11	n.c.	P9.6	n.c.	VSS	n.c.	B
C	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	n.c.	n.c.	C
D	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	P9.3	P9.2	D
E	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	n.c.	P9.1	E
F	USB_DM	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	P9.0	P7.11	F
G	USB_DP	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	P7.9	P7.10	G
H	RTC_XTAL1	RTC_XTAL2	HIB_IO_1	HIB_IO_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	n.c.	P7.8	H
J	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	$\overline{\text{PORST}}$	P1.15	n.c.	P7.7	J
K	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	n.c.	P7.6	K
L	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	P7.0	P7.5	L
M	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	P7.1	P7.3	M
N	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	P7.2	P7.4	N
P	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	n.c.	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

XMC4[78]00 - (top view)

Figure 6 XMC4[78]00 PG-LFBGA-196 Pin Configuration (top view)

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.11	G5	139	95	A1+	
P0.12	F5	138	94	A1+	
P0.13	E5	137	-	A1+	
P0.14	G6	136	-	A1+	
P0.15	E6	135	-	A1+	
P1.0	F9	112	79	A1+	
P1.1	G9	111	78	A1+	
P1.2	E11	110	77	A2	
P1.3	E12	109	76	A2	
P1.4	E10	108	75	A1+	
P1.5	F10	107	74	A1+	
P1.6	D9	116	83	A2	
P1.7	D10	115	82	A2	
P1.8	C10	114	81	A2	
P1.9	D11	113	80	A2	
P1.10	F12	106	73	A1+	
P1.11	F11	105	72	A1+	
P1.12	G11	104	71	A2	
P1.13	G12	103	70	A2	
P1.14	G10	102	69	A2	
P1.15	J12	94	68	A2	
P2.0	L11	74	52	A2	
P2.1	M12	73	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	M11	72	50	A2	
P2.3	N11	71	49	A2	
P2.4	N10	70	48	A2	
P2.5	P10	69	47	A2	
P2.6	L9	76	54	A1+	
P2.7	M9	75	53	A1+	
P2.8	N9	68	46	A2	
P2.9	P9	67	45	A2	

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	ALTn	HWO0	HWI0	Input	Input
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

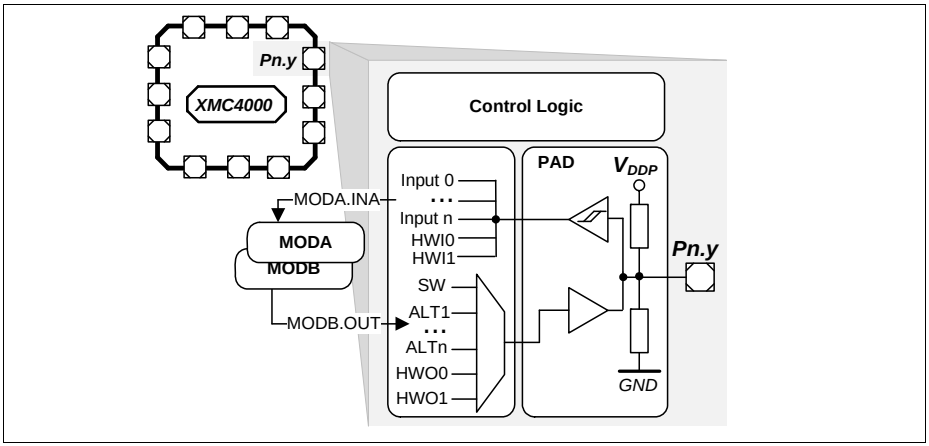


Figure 8 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

2.2.2.1 Port I/O Function Table

Table 12 Port I/O Functions

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ECAT0. PHY_RST	CAN. N0_TXD	CCU80. OUT21	LEDTS0. COL2					U1C1. DX0D	ETH0. CLK_RMIIB	ERU0. 0B0					ETH0. CLKRXB
P0.1	USB. DRIVEVBUS	U1C1. DOUT0	CCU80. OUT11	LEDTS0. COL3						ETH0. CRS_DVB	ERU0. 0A0				ECAT0. P1_RX_CLKA	ETH0. RXDVB
P0.2	ECAT0. P1_TXD2	U1C1. SELO1	CCU80. OUT01		U1C0. DOUT3	EBU. AD0	U1C0. HWIN3	EBU. D0	ETH0. RXD0B		ERU0. 3B3					
P0.3	ECAT0. P1_TXD3		CCU80. OUT20		U1C0. DOUT2	EBU. AD1	U1C0. HWIN2	EBU. D1	ETH0. RXD1B			ERU1. 3B0				
P0.4	ETH0. TX_EN		CCU80. OUT10		U1C0. DOUT1	EBU. AD2	U1C0. HWIN1	EBU. D2		U1C0. DX0A	ERU0. 2B3				ECAT0. P1_RXD3A	
P0.5	ETH0. TXD0	U1C0. DOUT0	CCU80. OUT00		U1C0. DOUT0	EBU. AD3	U1C0. HWIN0	EBU. D3		U1C0. DX0B		ERU1. 3A0			ECAT0. P1_RXD2A	
P0.6	ETH0. TXD1	U1C0. SELO0	CCU80. OUT30			EBU. ADV				U1C0. DX2A	ERU0. 3B2		CCU80. IN2B		ECAT0. P1_RXD1A	
P0.7	WWDT. SERVICE_OUT	U0C0. SELO0	ECAT0. LED_ERR			EBU. AD6	DB. TDI	EBU. D6	U0C0. DX2B	DSD. DIN1A	ERU0. 2B1		CCU80. IN0A	CCU80. IN1A	CCU80. IN2A	CCU80. IN3A
P0.8	SCU. EXTCLK	U0C0. SCLKOUT	ECAT0. LED_RUN			EBU. AD7	DB. TRST	EBU. D7	U0C0. DX1B	DSD. DIN0A	ERU0. 2A1	CAN. N3_RXDA	CCU80. IN1B			
P0.9		U1C1. SELO0	CCU80. OUT12	LEDTS0. COL0	ETH0. MDO	EBU. CS1	ETH0. MDIA		U1C1. DX2A	USB. ID	ERU0. 1B0				ECAT0. P1_RX_DVA	
P0.10	ETH0. MDC	U1C1. SCLKOUT	CCU80. OUT02	LEDTS0. COL1					U1C1. DX1A		ERU0. 1A0				ECAT0. P1_TX_CLKA	
P0.11	ECAT0. P1_LINK_ACT	U1C0. SCLKOUT	CCU80. OUT31		SDMMC. RST	EBU. BREQ			ETH0. RXERB	U1C0. DX1A	ERU0. 3A2				ECAT0. P1_RXD0A	
P0.12		U1C1. SELO0	CCU40. OUT3		ECAT0. MDO	EBU. HLDA	ECAT0. MDIA	EBU. HLDA		U1C1. DX2B	ERU0. 2B2					
P0.13		U1C1. SCLKOUT	CCU40. OUT2							U1C1. DX1B	ERU0. 2A2					
P0.14		U1C0. SELO1	CCU40. OUT1		U1C1. DOUT3		U1C1. HWIN3						CCU42. IN3C			
P0.15		U1C0. SELO2	CCU40. OUT0		U1C1. DOUT2		U1C1. HWIN2						CCU42. IN2C			
P1.0	DSD. CGPWMN	U0C0. SELO0	CCU40. OUT3	ERU1. PDOUT3					U0C0. DX2A		ERU0. 3B0		CCU40. IN3A			ECAT0. P0_TX_CLKA
P1.1	DSD. CGPWMP	U0C0. SCLKOUT	CCU40. OUT2	ERU1. PDOUT2			SDMMC. SDWC		U0C0. DX1A	POSIF0. IN2A	ERU0. 3A0		CCU40. IN2A			ECAT0. P0_RX_CLKA
P1.2	ECAT0. P0_TXD3		CCU40. OUT1	ERU1. PDOUT1	U0C0. DOUT3	EBU. AD14	U0C0. HWIN3	EBU. D14		POSIF0. IN1A		ERU1. 2B0	CCU40. IN1A			
P1.3	ECAT0. P0_TX_ENA	U0C0. MCLKOUT	CCU40. OUT0	ERU1. PDOUT0	U0C0. DOUT2	EBU. AD15	U0C0. HWIN2	EBU. D15		POSIF0. IN0A		ERU1. 2A0	CCU40. IN0A			
P1.4	WWDT. SERVICE_OUT	CAN. N0_TXD	CCU80. OUT33	CCU81. OUT20	U0C0. DOUT1		U0C0. HWIN1		U0C0. DX0B	CAN. N1_RXDD	ERU0. 2B0		CCU41. IN0C			ECAT0. P0_RXD0A

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P4.3	U2C1. SELO2	U0C0. SELO5	CCU43. OUT3	ECAT0. MCLK									CCU43. IN3A			
P4.4		U0C0. SELO4	CCU43. OUT2		U2C1. DOUT3		U2C1. HWIN3						CCU43. IN2A			
P4.5		U0C0. SELO3	CCU43. OUT1		U2C1. DOUT2		U2C1. HWIN2						CCU43. IN1A			
P4.6		U0C0. SELO2	CCU43. OUT0		U2C1. DOUT1		U2C1. HWIN1		CAN. N2_RXDC			U2C1. DX0E	CCU43. IN0A			
P4.7	U2C1. DOUT0	CAN. N2_TXD			U2C1. DOUT0		U2C1. HWIN0		U0C0. DX0C				CCU43. IN0C			
P5.0	U2C0. DOUT0	DSD. CGPWMN	CCU81. OUT33	ERU1. PDOUT0	U2C0. DOUT0		U2C0. HWIN0		U2C0. DX0B	ETH0. RXD0D	U0C0. DX0D	ECAT0. P0_RXD0B	CCU81. IN0A	CCU81. IN1A	CCU81. IN2A	CCU81. IN3A
P5.1	U0C0. DOUT0	DSD. CGPWMP	CCU81. OUT32	ERU1. PDOUT1	U2C0. DOUT1		U2C0. HWIN1		U2C0. DX0A	ETH0. RXD1D		ECAT0. P0_RXD1B	CCU81. IN0B			
P5.2	U2C0. SCLKOUT	ECAT0. P0_LINK_ACT	CCU81. OUT23	ERU1. PDOUT2					U2C0. DX1A	ETH0. CRS_DVD		ECAT0. P0_RXD2B	CCU81. IN1B			ETH0. RXDVD
P5.3	U2C0. SELO0		CCU81. OUT22	ERU1. PDOUT3	EBU. CKE	EBU. A20			U2C0. DX2A	ETH0. RXERD			CCU81. IN2B			
P5.4	U2C0. SELO1		CCU81. OUT13		$\overline{\text{EBU.}}$ RAS	EBU. A21				ETH0. CRSD			CCU81. IN3B			ECAT0. P0_RX_CLKB
P5.5	U2C0. SELO2		CCU81. OUT12		$\overline{\text{EBU.}}$ CAS	EBU. A22				ETH0. COLD						ECAT0. P0_TX_CLKB
P5.6	U2C0. SELO3		CCU81. OUT03		EBU. BFCLKO	EBU. A23			EBU. BFCLKI							ECAT0. P0_RX_DVB
P5.7	ECAT0. SYNC0		CCU81. OUT02	LEDTS0. COLA	U2C0. DOUT2		U2C0. HWIN2					ECAT0. P0_RXD3B				
P5.8	ECAT0. P1_TX_ENA	U1C0. SCLKOUT	CCU80. OUT01	CAN. N4_TXD	EBU. SDCLKO	$\overline{\text{EBU.}}$ CS2			ETH0. RXD2A	U1C0. DX1B						
P5.9		U1C0. SELO0	CCU80. OUT20	ETH0. TX_EN	EBU. BFCLKO	$\overline{\text{EBU.}}$ CS3			ETH0. RXD3A	U1C0. DX2B					ECAT0. P1_TX_CLKB	
P5.10		U1C0. MCLKOUT	CCU80. OUT10	LEDTS0. LINE7	LEDTS0. EXTENDED7		LEDTS0. TSIN7A		ETH0. CLK_TXA		CAN. N5_RXDA					
P5.11		U1C0. SELO1	CCU80. OUT00	CAN. N5_TXD					ETH0. CRSA							
P6.0	ETH0. TXD2	U0C1. SELO1	CCU81. OUT31	ECAT0. PHY_CLK25	DB. ETM_TRACECLK	EBU. A16										
P6.1	ETH0. TXD3	U0C1. SELO0	CCU81. OUT30	ECAT0. P0_TX_ENA	DB. ETM_TRACEDATA3	EBU. A17			U0C1. DX2C							
P6.2	ETH0. TXER	U0C1. SCLKOUT	CCU43. OUT3	ECAT0. P0_TXD0	DB. ETM_TRACEDATA2	EBU. A18			U0C1. DX1C							
P6.3			CCU43. OUT2	ECAT0. P0_LINK_ACT					U0C1. DX0C	ETH0. RXD3B						
P6.4		U0C1. DOUT0	CCU43. OUT1	ECAT0. P0_TXD1	EBU. SDCLKO	EBU. A19			EBU. SDCLKI	ETH0. RXD2B						
P6.5	CAN. N3_TXD	U0C1. MCLKOUT	CCU43. OUT0	ECAT0. P0_TXD2	DB. ETM_TRACEDATA1	$\overline{\text{EBU.}}$ BC2			DSD. DIN3A	ETH0. CLK_RMIID		U2C0. DX0D				ETH0. CLKRXD

3 Electrical Parameters

Attention: All parameters in this chapter are preliminary target values and may change based on characterization results.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the XMC4[78]00 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with a two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are a distinctive feature of the XMC4[78]00 and must be regarded for system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC4[78]00 is designed in.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$ 7)
Differential Non-Linearity Error 8)	EA_{DNL} CC	-3	–	3	LSB	
Gain Error 8)	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity 8)	EA_{INL} CC	-3	–	3	LSB	
Offset Error 8)	EA_{OFF} CC	-4	–	4	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion 5)	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA} 9)
ON resistance of the analog input path	R_{AIN} CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 16**).

4) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from V_{AREF}/2.

5) Applies to AINx, when used as alternate reference input.

6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.

7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.

8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 459 ns results in a typical average current of I_{AREF} = 65.4 µA.

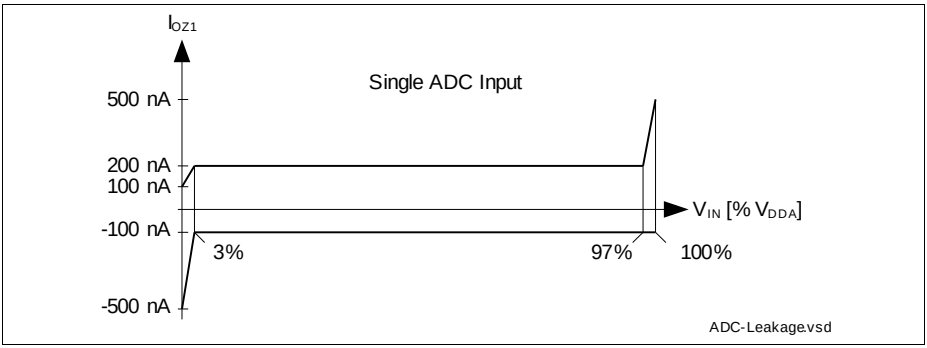


Figure 16 VADC Analog Input Leakage Current

Conversion Time

Table 26 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time	t_C CC	$2 \times T_{ADC}$ + $(2 + N + STC + PC + DM) \times T_{ADCI}$	µs	N = 8, 10, 12 for N-bit conversion $T_{ADC} = 1 / f_{PERIPH}$ $T_{ADCI} = 1 / f_{ADCI}$

- STC defines additional clock cycles to extend the sample time
- PC adds two cycles if post-calibration is enabled
- DM adds one cycle for an extended conversion time of the MSB

Conversion Time Examples

System assumptions:
f_{ADC} = 144 MHz i.e. t_{ADC} = 6.9 ns, DIVA = 3, f_{ADCI} = 36 MHz i.e. t_{ADCI} = 27.8 ns
According to the given formulas the following minimum conversion times can be achieved (STC = 0, DM = 0):

12-bit post-calibrated conversion (PC = 2):
$t_{CN12C} = (2 + 12 + 2) \times t_{ADCI} + 2 \times t_{ADC} = 16 \times 27.8$ ns $+ 2 \times 6.9$ ns = 459 ns
12-bit uncalibrated conversion:
$t_{CN12} = (2 + 12) \times t_{ADCI} + 2 \times t_{ADC} = 14 \times 27.8$ ns $+ 2 \times 6.9$ ns = 403 ns
10-bit uncalibrated conversion:
$t_{CN10} = (2 + 10) \times t_{ADCI} + 2 \times t_{ADC} = 12 \times 27.8$ ns $+ 2 \times 6.9$ ns = 348 ns
8-bit uncalibrated:
$t_{CN8} = (2 + 8) \times t_{ADCI} + 2 \times t_{ADC} = 10 \times 27.8$ ns $+ 2 \times 6.9$ ns = 292 ns

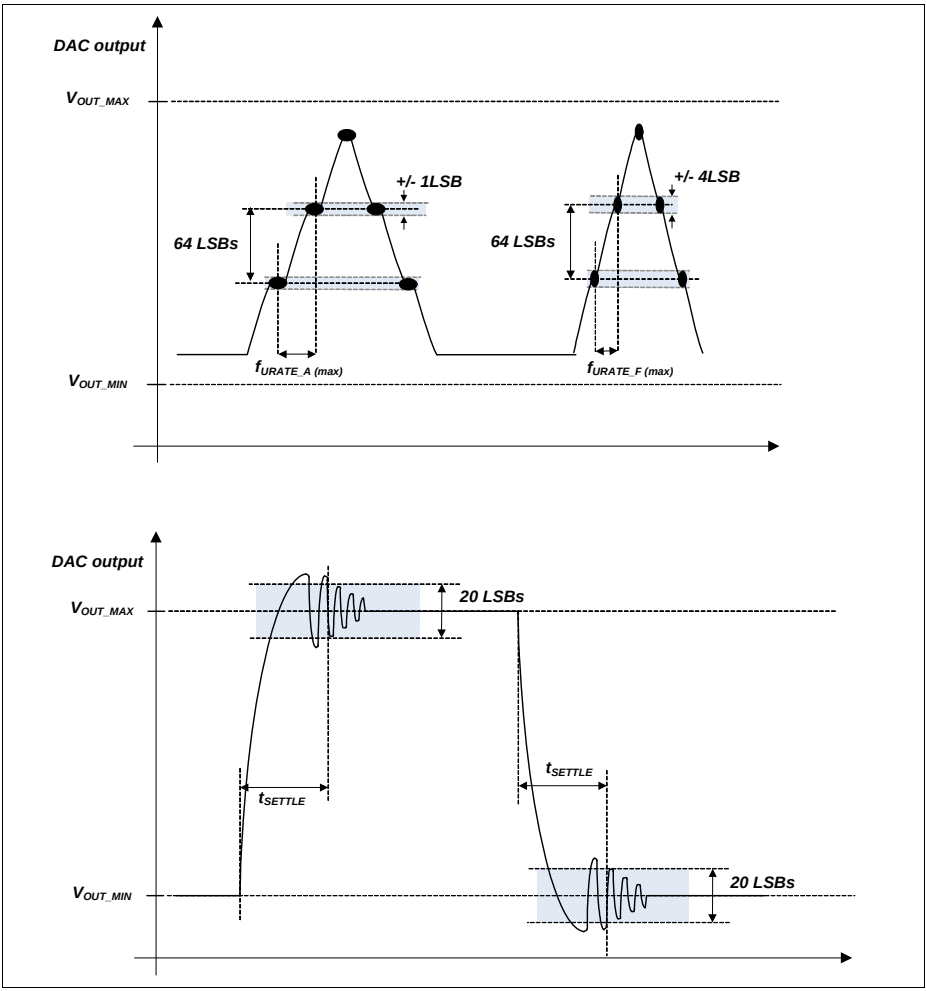


Figure 17 DAC Conversion Examples

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	210	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	50	–	450	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	45	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

Table 47 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 48 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

With clock delay:

(2)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(3)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} < t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 10$$

$$t_{DATA\_DELAY} < 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of t_{WL}= 20 ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(4)

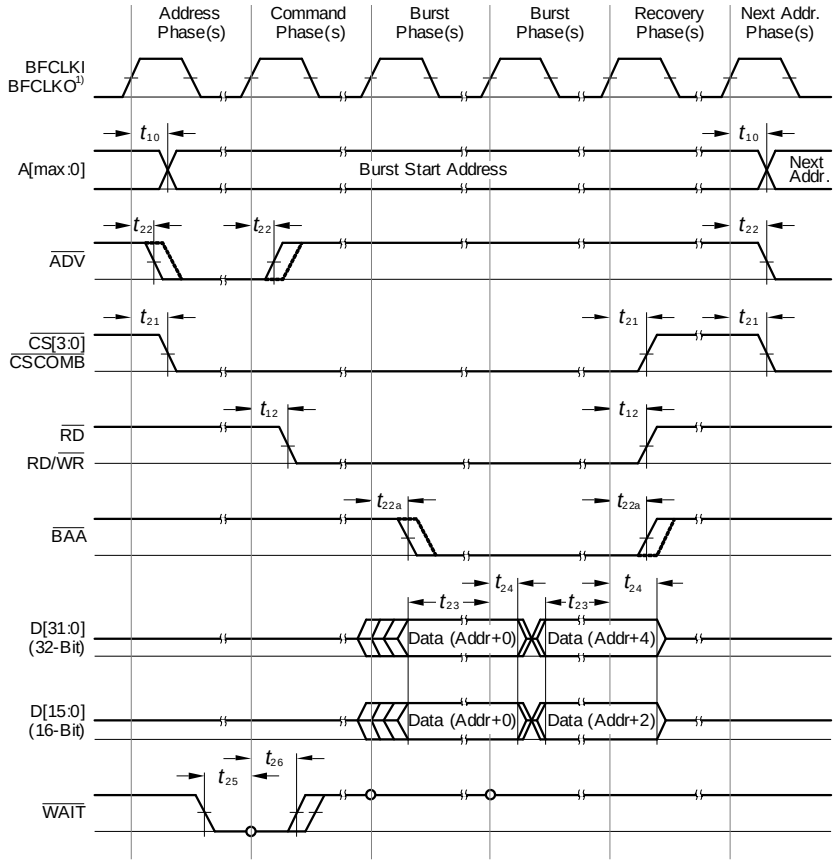
$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} < 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5$$

$$t_{DATA\_DELAY} < 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of t_{WL}= 20 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

3) If the clock feedback is not enabled, the input signals are latched using the internal clock in the same way as for asynchronous access. Thus, t_5, t_6, t_7 and t_8 from the asynchronous timing apply.



1) Output delays are always referenced to BCLKO . The reference clock for input characteristics depends on bit EBU _BFCON.FDBKEN.
EBU_BFCON.FDBKEN= 0: BFCLKO is the input reference clock .
EBU_BFCON.FDBKEN= 1: BFCLKI is the input reference clock (EBU clock feedback enabled).

EBU_BurstRDWR.vsd

Figure 45 EBU Burst Mode Read / Write Access Timing

3.3.13.5 Sync/Latch Timings

Table 70 Sync/Latch Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SYNC0/1	$t_{DC\_SYNC\_Jitter}$ SR	–	–	11 + m[1)]	ns	
LATCH0/1	t_{DC_LATCH} SR	12 + n[2)]	–	–	ns	

1) additional delay form logic and pad, number is added after characterization

2) additional shaping delay, number is added after characterization

Note: SYNC0/1 pulse length are initially loaded by EEPROM content ADR 0x0002. The actual used value can be read back from Register DC_PULSE_LEN.

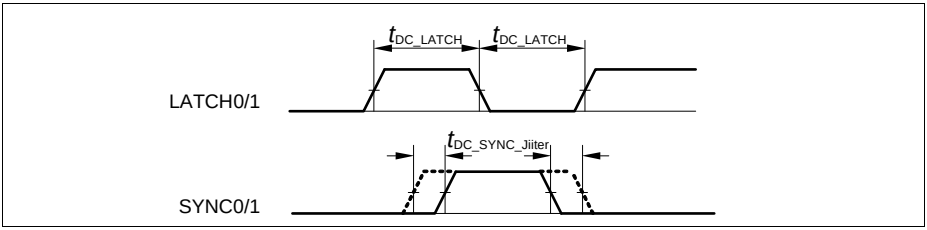


Figure 59 Sync/Latch Timings

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG