Infineon Technologies - XMC4700F144K1536AAXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	119
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-24
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4700f144k1536aaxqma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

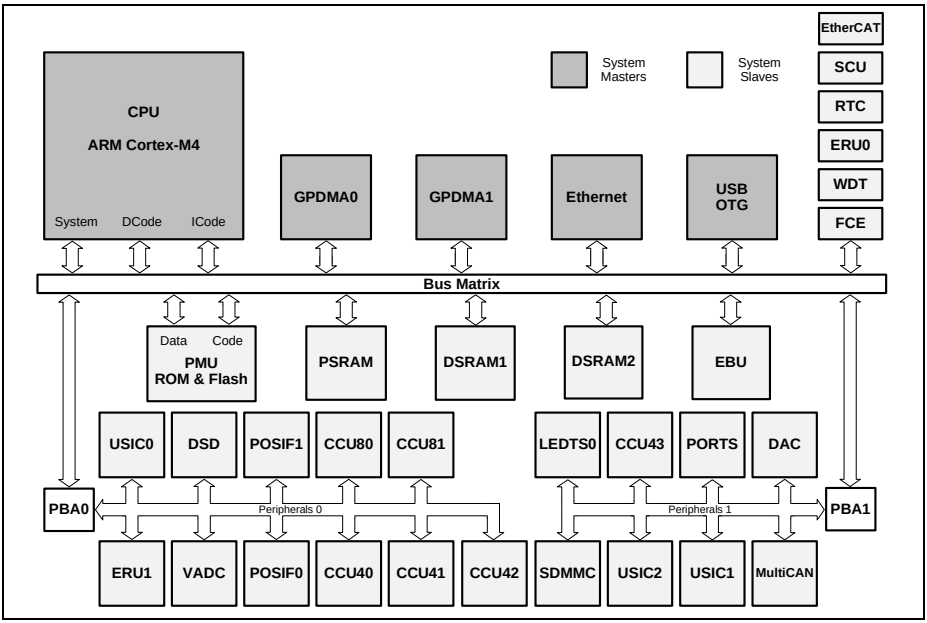

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

Table 1 Synopsis of XMC4[78]00 Device Types (cont'd)

Derivative[1)]	Package	Flash Kbytes	SRAM Kbytes
XMC4700-F144x1536	PG-LQFP-144	1536	276
XMC4700-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x2048	PG-LFBGA-196	2048	352
XMC4800-F144x2048	PG-LQFP-144	2048	352
XMC4800-F100x2048	PG-LQFP-100	2048	352
XMC4800-E196x1536	PG-LFBGA-196	1536	276
XMC4800-F144x1536	PG-LQFP-144	1536	276
XMC4800-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x1024	PG-LFBGA-196	1024	200
XMC4800-F144x1024	PG-LQFP-144	1024	200
XMC4800-F100x1024	PG-LQFP-100	1024	200

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4[78]00 Device Types

Derivative[1)]	LEDTS Intf.	SDMMC Intf.	EBU Intf.[2)]	ETH Intf.[3)]	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4700-E196x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x2048	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-E196x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x1536	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]

The XMC4[78]00 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF}. Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

Table 15 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V
A2	$V_{IN} = V_{DDP}$ + 0.7 V	$V_{IN} = V_{DDP}$ + 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V

Table 16 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS}$ - 1.0 V	$V_{IN} = V_{SS}$ - 0.75 V
A2	$V_{IN} = V_{SS}$ - 0.7 V	$V_{IN} = V_{SS}$ - 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ - 1.0 V	$V_{IN} = V_{DDP}$ - 0.75 V

Table 17 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[15:0], P3.[15:0], P8.[11:0]
2	P14.[15:0], P15.[15:0]
3	P2.[15:0], P5.[11:0], P7[11:0]
4	P1.[15:0], P4.[7:0], P6.[6:0], P9.[11:0]

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2][5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \le V_{AIN} \le 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \le V_{AIN} \le V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\ V \le V_{AREF} \le V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\ V \le V_{AGND} \le V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	36	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

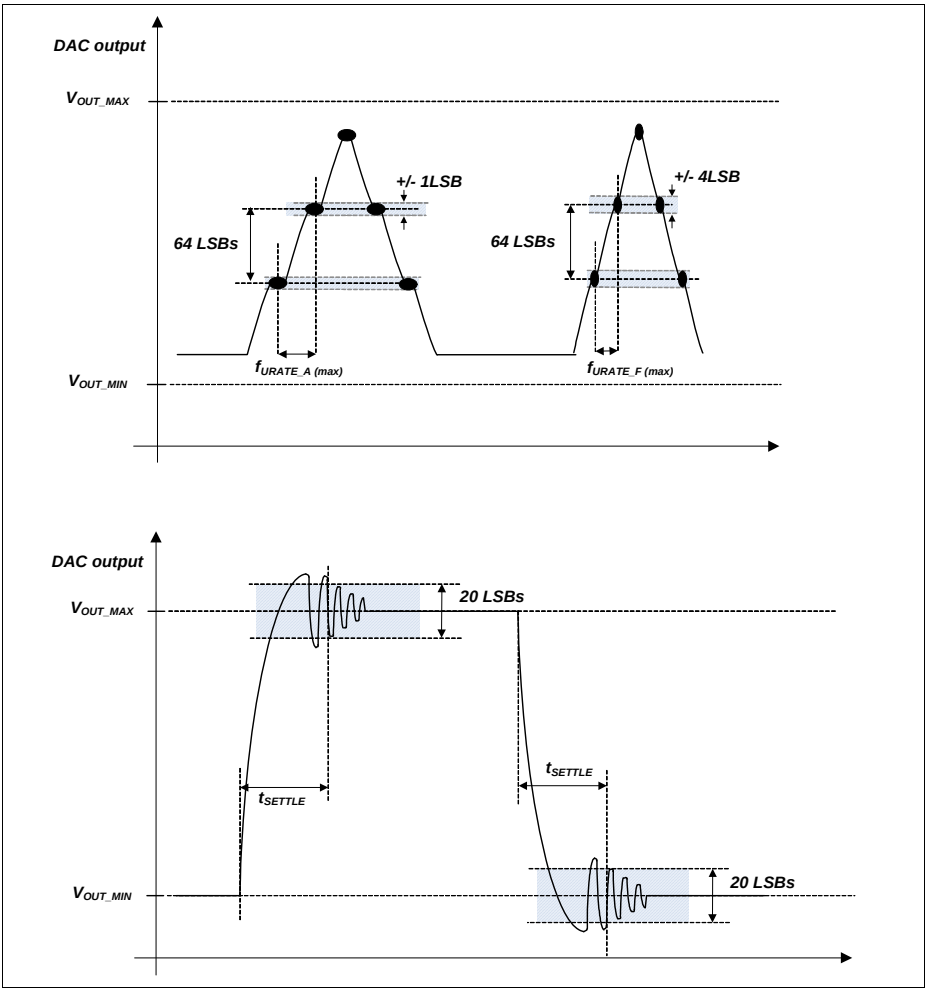

Figure 17 DAC Conversion Examples

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 30 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0\ V \le V_{IN} \le 5.25\ V$: T_{AVG} = 1 ms

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 34 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)11)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	135	–	mA	144 / 144 / 144
			–	125	–		144 / 72 / 72
			–	97	–		72 / 72 / 144
			–	80	–		24 / 24 / 24
			–	68	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA}	CC	–	108	–	mA	144 / 144 / 144
			–	98	–		144 / 72 / 72
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	86	–	mA	144 / 144 / 144
			–	85	–		144 / 72 / 72
			–	70	–		72 / 72 / 144
			–	55	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	127	–	mA	144 / 144 / 144
			–	115	–		144 / 72 / 72
			–	93	–		72 / 72 / 144
			–	57	–		24 / 24 / 24
			–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	48	–		100 / 100 / 100

Table 34 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sleep supply current[4] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS} CC	–	77	–	mA	144 / 144 / 144
		–	76	–		144 / 72 / 72
		–	65	–		72 / 72 / 144
		–	53	–		24 / 24 / 24
		–	46	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	47	–		100 / 100 / 100
Deep Sleep supply current[5] Flash in Sleep mode Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPD} CC	–	11	–	mA	24 / 24 / 24
		–	7.0	–		4 / 4 / 4
		–	6.6	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz		–	7.6	–		100 / 100 / 100 [6]
Hibernate supply current RTC on[7]	I_{DDPH} CC	–	8.7	–	µA	V_{BAT} = 3.3 V
		–	6.5	–		V_{BAT} = 2.4 V
		–	5.7	–		V_{BAT} = 2.0 V
Hibernate supply current RTC off[8]	I_{DDPH} CC	–	8.0	–	µA	V_{BAT} = 3.3 V
		–	6.0	–		V_{BAT} = 2.4 V
		–	5.0	–		V_{BAT} = 2.0 V
Hibernate off[9]	I_{DDPH} CC	–	4.4	–	µA	V_{BAT} = 3.3 V
		–	3.5	–		V_{BAT} = 2.4 V
		–	3.1	–		V_{BAT} = 2.0 V
Worst case active supply current[10]	I_{DDPA} CC	–	–	250 [11]	mA	V_{DDP} = 3.6 V, T_J = 150 °C
V_{DDA} power supply current	I_{DDA} CC	–	–	–[12]	mA	
I_{DDP} current at $\overline{\text{PORST}}$ Low	I_{DDP_PORST} CC	–	5	10	mA	V_{DDP} = 3.3 V, T_J = 25 °C
		–	13	55	mA	V_{DDP} = 3.6 V, T_J = 150 °C
Power Dissipation	P_{DISS} CC	–	–	1.4	W	V_{DDP} = 3.6 V, T_J = 150 °C

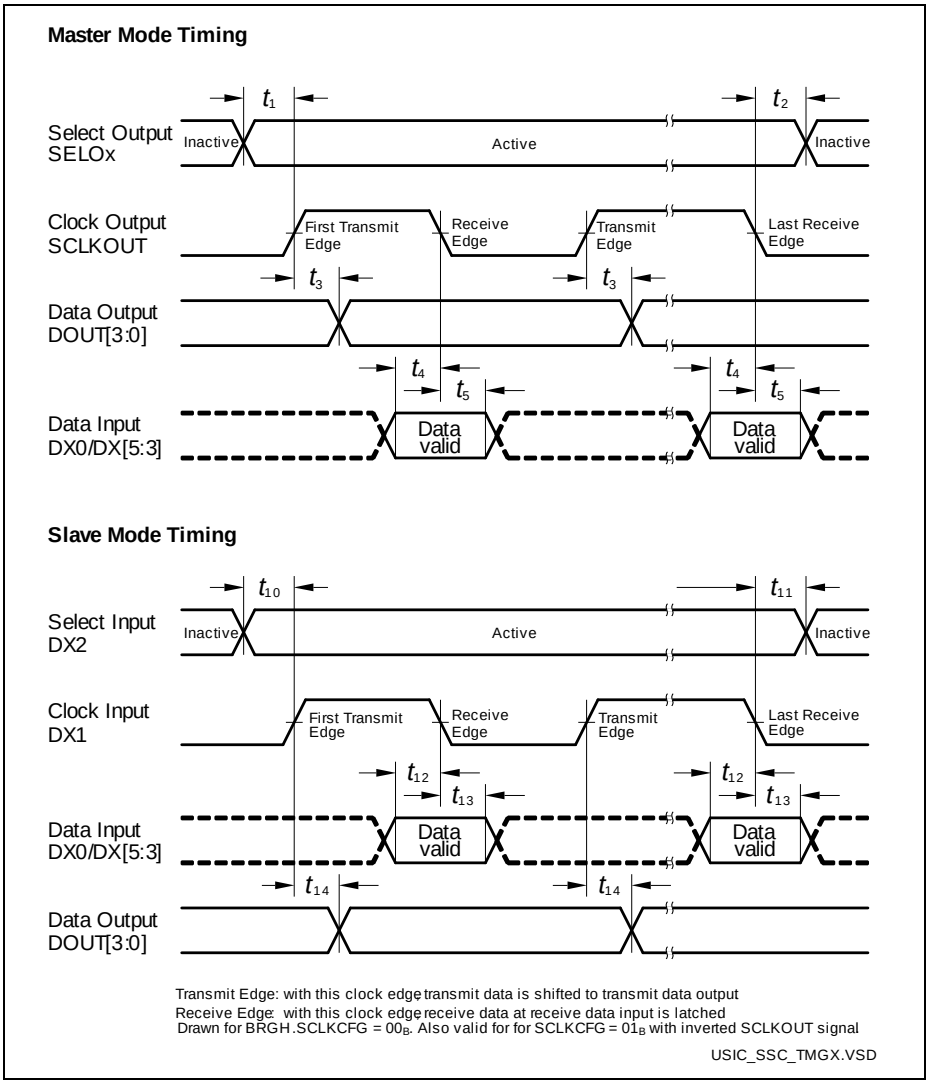

Figure 33 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 48 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 49 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

Table 55 SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	
SD card input hold time	t_{IH}	2	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	2.5	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

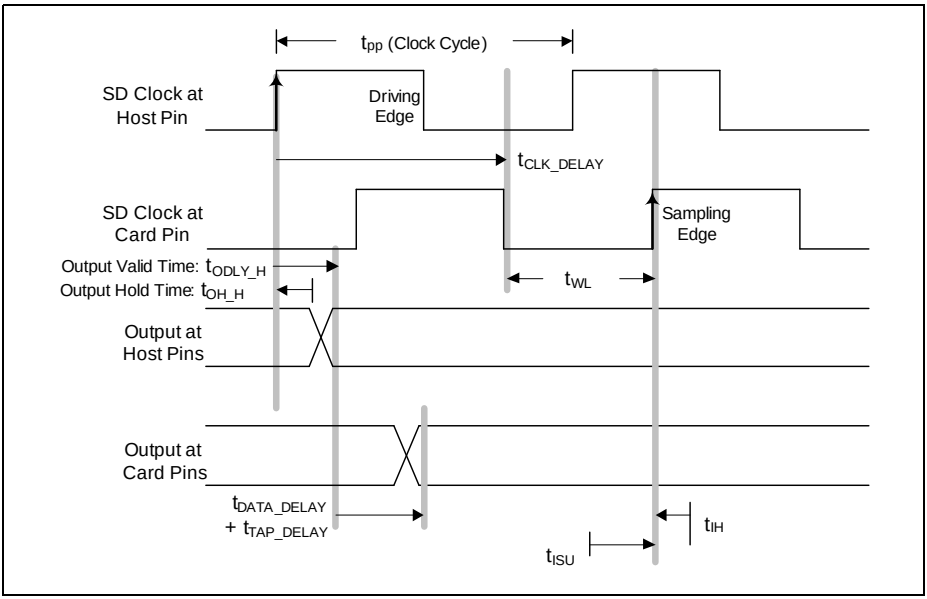

Figure 39 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(7)

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL}$$

With clock delay:

(8)

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(9)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{CLK\_DELAY} < t_{WL} - t_{ISU} - t_{ODLY\_H}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{WL} - t_{ISU} - t_{ODLY\_H} - t_{TAP\_DELAY}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 10 - 6 - 14 - t_{TAP\_DELAY}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < -10 - t_{TAP\_DELAY}$$

The data delay is less than the clock delay by at least 10 ns in the ideal case where t_{WL}= 10 ns.

High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(10)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < t_{WL} + t_{OH\_H} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + 2 + t_{TAP\_DELAY} - 2$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 13.2 ns (external delay line) in ideal case of t_{WL}= 10 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

Demultiplexed Write Timing

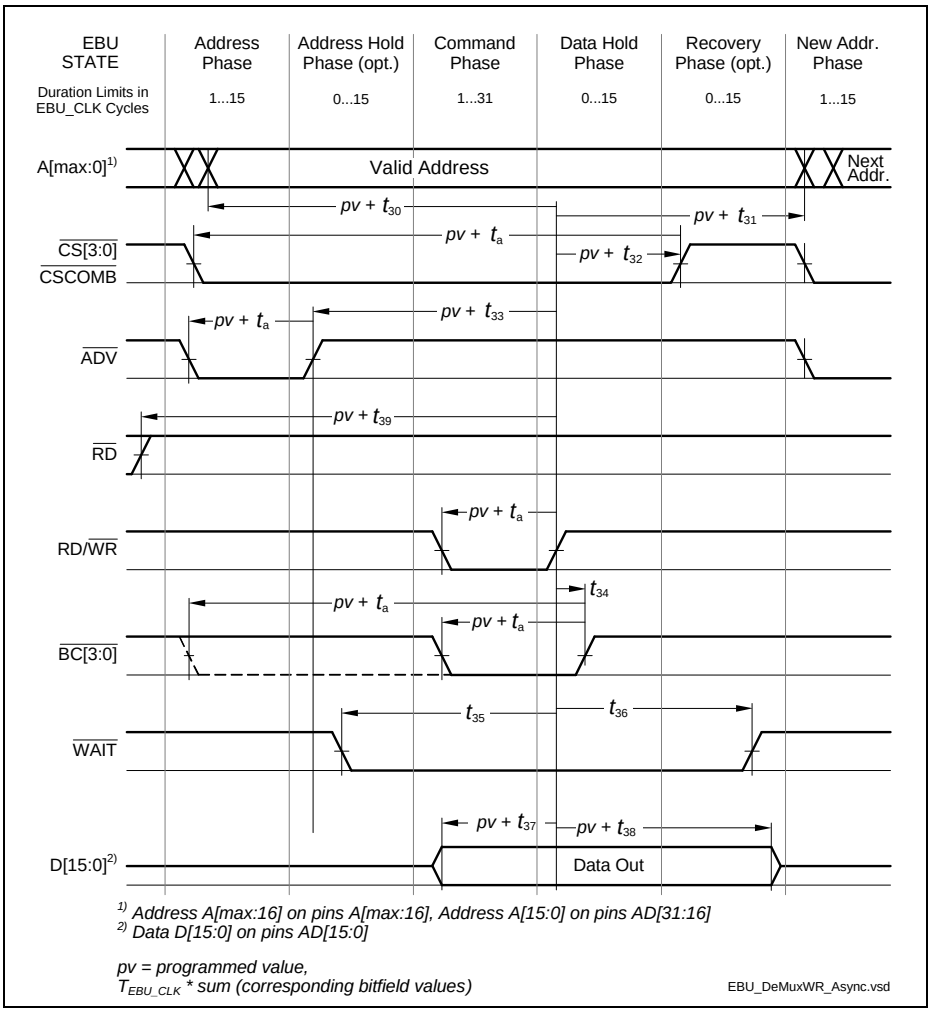

Figure 44 Demultiplexed Write Access

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS}}$(3:0) low		CC	t_8	–	9	
$\overline{\text{CS}}$(3:0) high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC}}$(3:0) low		CC	t_{16}	–	9	
$\overline{\text{BC}}$(3:0) high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1)]		CC	t_{22}	–	7	
CKE output hold[1)]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 64 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

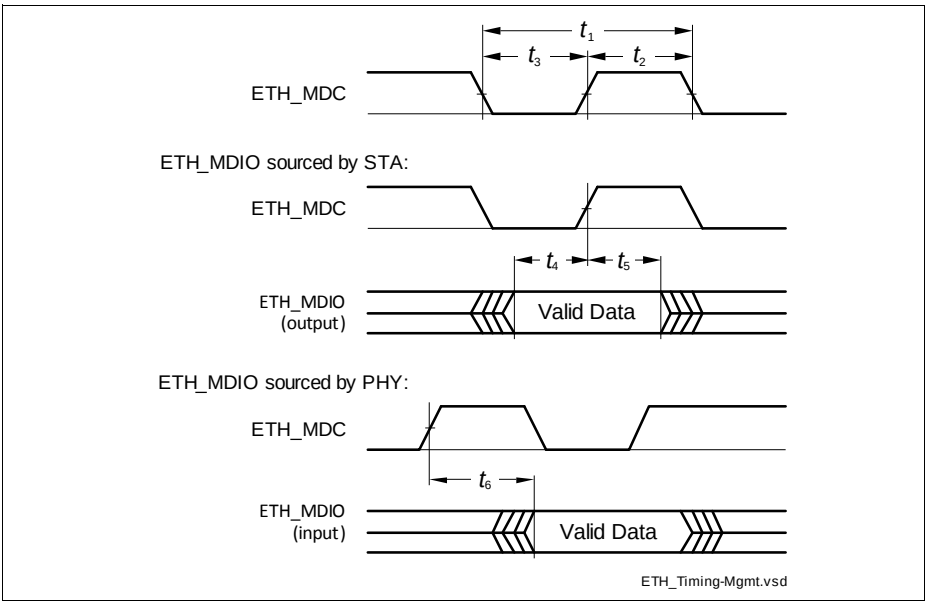

Figure 52 ETH Management Signal Timing

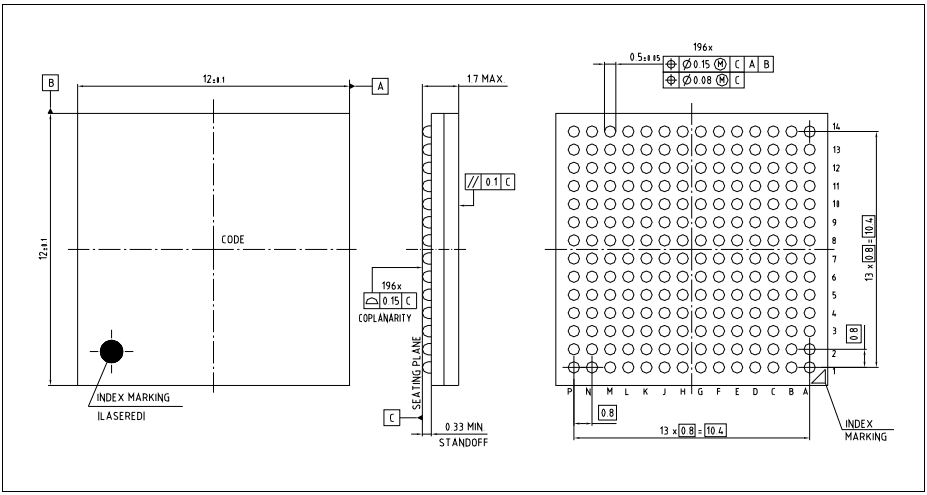

Figure 62 PG-LFBGA-196-2 (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**

5 Quality Declarations

The qualification of the XMC4[78]00 is executed according to the JEDEC standard JESD47I.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 72 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	3 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	1 000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D