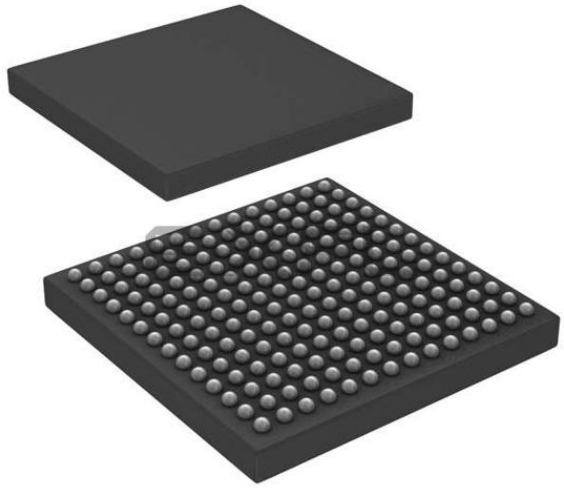
Infineon Technologies - XMC4800E196F1024AAXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	155
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	PG-LFBGA-196-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800e196f1024aaxqma1

XMC4[78]00 Data Sheet

Revision History: V1.0 2016-01

Previous Versions:
V0.7 2015-10 (preliminary)

Page	Subjects
8	Corrected EtherCAT features to 8 Fieldbus Memory Management Units (FMMU) and 8 Sync Manager.
46	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
53	Added HIBIO characteristics.
58	Corrected DAC INL and gain error.
70	Changed frequency dependency of the current consumption.
73	Added peripheral idle current overview.
127ff	Updated package parameters and drawings.
132	Higher HBM and CDM ESD limits.

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Table 2 Features of XMC4[78]00 Device Types (cont'd)

Derivative[1]	LEDTS Intf.	SDMMC Intf.	EBU Intf.[2]	ETH Intf.[3]	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4800-E196x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x2048	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x2048	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1536	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1536	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-E196x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F144x1024	1	1	SDM	MR	2 x MII	1	3 x 2	N[0..5] MO[0..255]
XMC4800-F100x1024	1	1	M16	R	2 x MII	1	3 x 2	N[0..5] MO[0..255]

1) x is a placeholder for the supported temperature range.

2) Memory types supported S=SDRAM, D=DEMUX, M=MUX 16-bit and 32-bit, M16=MUX 16-bit

3) Supported interfaces, M=MII, R=RMII.

Table 3 Features of XMC4[78]00 Device Types

Derivative[1]	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4700-E196x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4700-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4700-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x2048	32	4	2	4 x 4	2 x 4	2

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P5.3	L10	81	-	A2	
P5.4	M10	80	-	A2	
P5.5	L8	79	-	A2	
P5.6	M8	78	-	A2	
P5.7	L7	77	55	A1+	
P5.8	K6	58	-	A2	
P5.9	M6	57	-	A2	
P5.10	K5	56	-	A1+	
P5.11	L5	55	-	A1+	
P6.0	J10	101	-	A2	
P6.1	H9	100	-	A2	
P6.2	K10	99	-	A2	
P6.3	J9	98	-	A1+	
P6.4	H10	97	-	A2	
P6.5	H11	96	-	A2	
P6.6	H12	95	-	A2	
P7.0	L13	-	-	A2	
P7.1	M13	-	-	A2	
P7.2	N13	-	-	A2	
P7.3	M14	-	-	A2	
P7.4	N14	-	-	A1+	
P7.5	L14	-	-	A1+	
P7.6	K14	-	-	A1+	
P7.7	J14	-	-	A1+	
P7.8	H14	-	-	A2	
P7.9	G13	-	-	A1+	
P7.10	G14	-	-	A1+	
P7.11	F14	-	-	A1+	
P8.0	B7	-	-	A2	
P8.1	A7	-	-	A2	
P8.2	B3	-	-	A2	
P8.3	B2	-	-	A2	
P8.4	B6	-	-	A1+	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P14.8					DAC. OUT_0					VADC. G1CH0		VADC. G3CH2	ETH0. RXD0C			
P14.9					DAC. OUT_1					VADC. G1CH1		VADC. G3CH3	ETH0. RXD1C			
P14.12										VADC. G1CH4						ECAT0. P1_RXD1B
P14.13										VADC. G1CH5						ECAT0. P1_RXD2B
P14.14										VADC. G1CH6					G1ORC6	ECAT0. P1_RXD3B
P14.15										VADC. G1CH7					G1ORC7	ECAT0. P1_RX_DVB
P15.2											VADC. G2CH2					ECAT0. P1_RX_ERRB
P15.3											VADC. G2CH3					ECAT0. P1_LINKB
P15.4											VADC. G2CH4					
P15.5											VADC. G2CH5					
P15.6											VADC. G2CH6					
P15.7											VADC. G2CH7					
P15.8												VADC. G3CH0	ETH0. CLK_RMIIC			ETH0. CLKRXC
P15.9												VADC. G3CH1	ETH0. CRS_DVC			ETH0. RXDVC
P15.12												VADC. G3CH4				
P15.13												VADC. G3CH5				
P15.14												VADC. G3CH6				
P15.15												VADC. G3CH7				
HIB_IO_0	HIBOUT	WWDT. SERVICE_OUT							WAKEUPA							
HIB_IO_1	HIBOUT	WWDT. SERVICE_OUT							WAKEUPB							
USB_DP																
USB_DM																
TCK							DB.TCK/ SWCLK									
TMS					DB.TMS/ SWDIO											
$\overline{\text{PORST}}$																

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 13 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in **Table 17**.

Figure 10 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

Table 14 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1)]	I_{OVG} SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 17**.

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

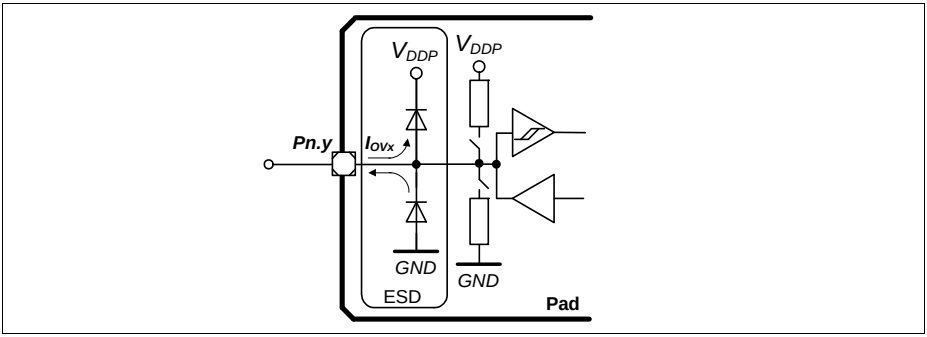

Figure 11 Input Overload Current via ESD structures

Table 15 and **Table 16** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 15 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V
A2	$V_{IN} = V_{DDP}$ + 0.7 V	$V_{IN} = V_{DDP}$ + 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ + 1.0 V	$V_{IN} = V_{DDP}$ + 0.75 V

Table 16 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA, T_J = -40 °C	I_{OV} = 5 mA, T_J = 150 °C
A1 / A1+	$V_{IN} = V_{SS}$ - 1.0 V	$V_{IN} = V_{SS}$ - 0.75 V
A2	$V_{IN} = V_{SS}$ - 0.7 V	$V_{IN} = V_{SS}$ - 0.6 V
AN/DIG_IN	$V_{IN} = V_{DDP}$ - 1.0 V	$V_{IN} = V_{DDP}$ - 0.75 V

Table 17 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[15:0], P3.[15:0], P8.[11:0]
2	P14.[15:0], P15.[15:0]
3	P2.[15:0], P5.[11:0], P7[11:0]
4	P1.[15:0], P4.[7:0], P6.[6:0], P9.[11:0]

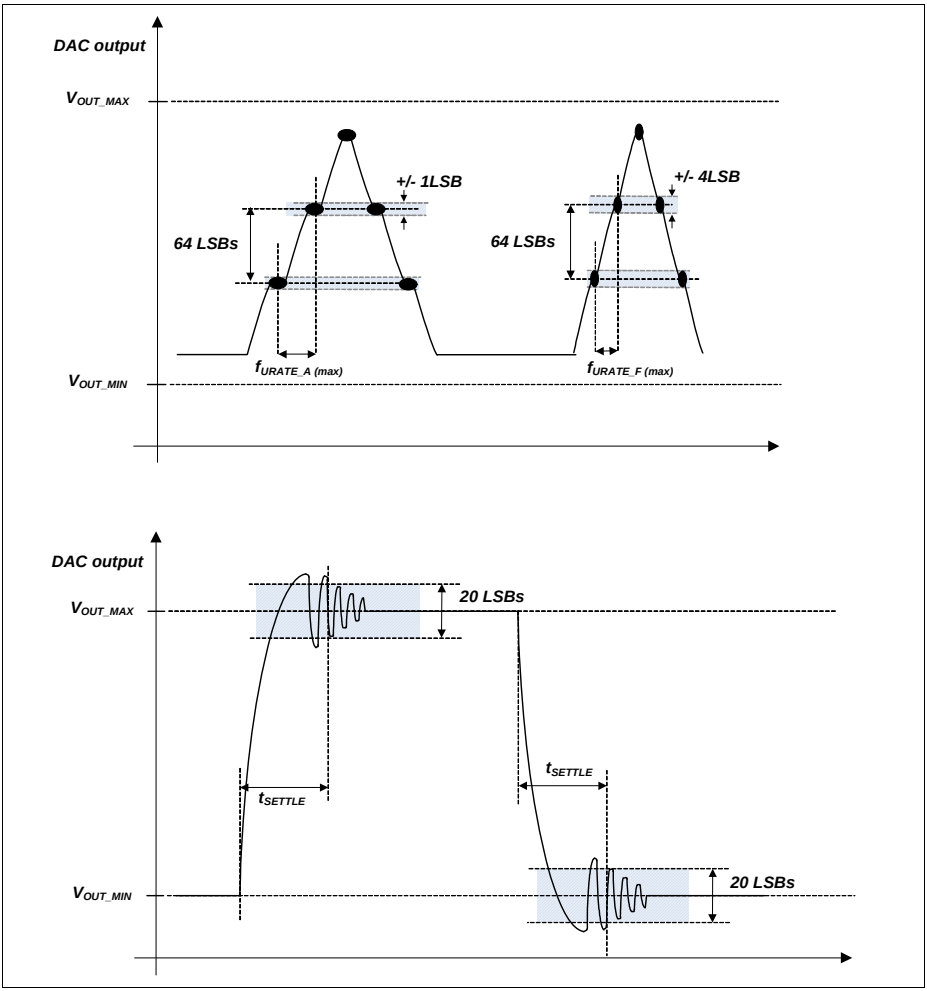

Figure 17 DAC Conversion Examples

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE}	CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1]
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	10	µs	

1) At V_{DDP_max} = 3.63 V the typical offset error increases by an additional ΔT_{OE} = ±1 °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

Temperature T_{DTS} = (RESULT - 605) / 2.05 [°C]

This formula and the values defined in **Table 29** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 30 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0\ V \le V_{IN} \le 5.25\ V$: T_{AVG} = 1 ms

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

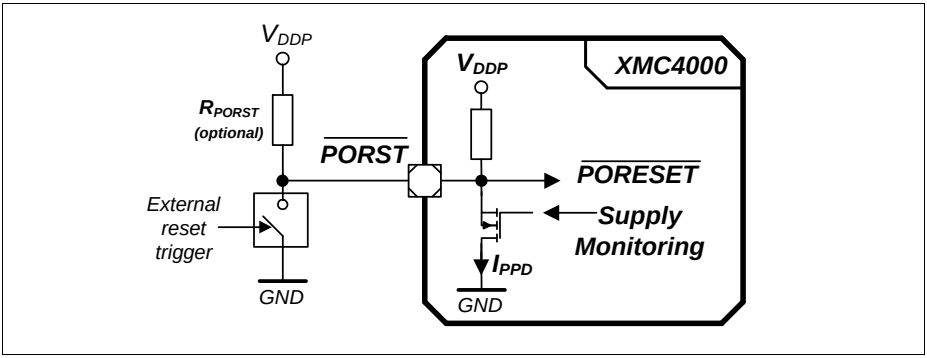

Figure 25 $\overline{\text{PORST}}$ Circuit

Table 37 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	[4]
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

Table 49 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

Full-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(6)

$$t_{CLK\_DELAY} + t_{OH} + t_{DATA\_DELAY} + t_{TAP\_DELAY} > t_{IH\_F}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > t_{IH\_F} - t_{OH} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} > 2 - t_{TAP\_DELAY}$$

The data + clock delay must be greater than 2 ns if t_{TAP_DELAY} is not used.

If the t_{TAP_DELAY} is programmed to at least 2 ns, the data + clock delay must be greater than 0 ns (or less). This is always fulfilled.

AC Timing Specifications (High-Speed Mode)

Table 54 SDMMC Timing for High-Speed Mode

Parameter	Symbol		Values		Unit	Note/ Test Condition
			Min.	Max.		
Clock frequency in high speed transfer mode ($1/t_{pp}$)	f_{pp}	CC	0	48	MHz	
Clock cycle in high speed transfer mode	t_{pp}	CC	20	–	ns	
Clock low time	t_{WL}	CC	7	–	ns	
Clock high time	t_{WH}	CC	7	–	ns	
Clock rise time	t_{TLH}	CC	–	3	ns	
Clock fall time	t_{THL}	CC	–	3	ns	
Inputs setup to clock rising edge	t_{ISU_H}	SR	2	–	ns	
Inputs hold after clock rising edge	t_{IH_H}	SR	2	–	ns	
Outputs valid time in high speed mode	t_{ODLY_H}	CC	–	14	ns	
Outputs hold time in high speed mode	t_{OH_H}	CC	2	–	ns	

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 60 EBU Arbitration Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1	CC	–	–	16	ns	C_L = 50 pF
Data setup to BFCLKO falling edge	t_2	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3	SR	2	–	–	ns	–

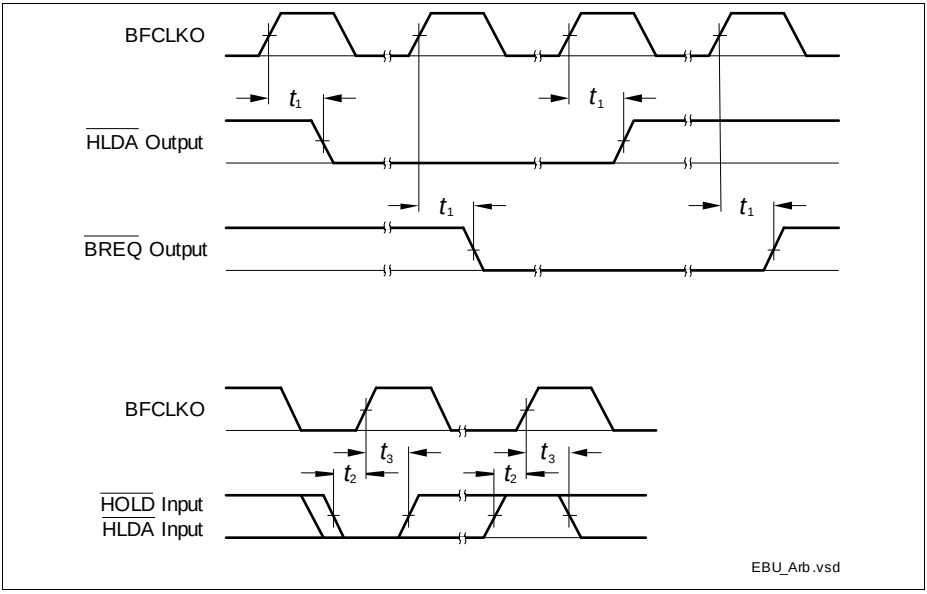

Figure 46 EBU Arbitration Signal Timing

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 64 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

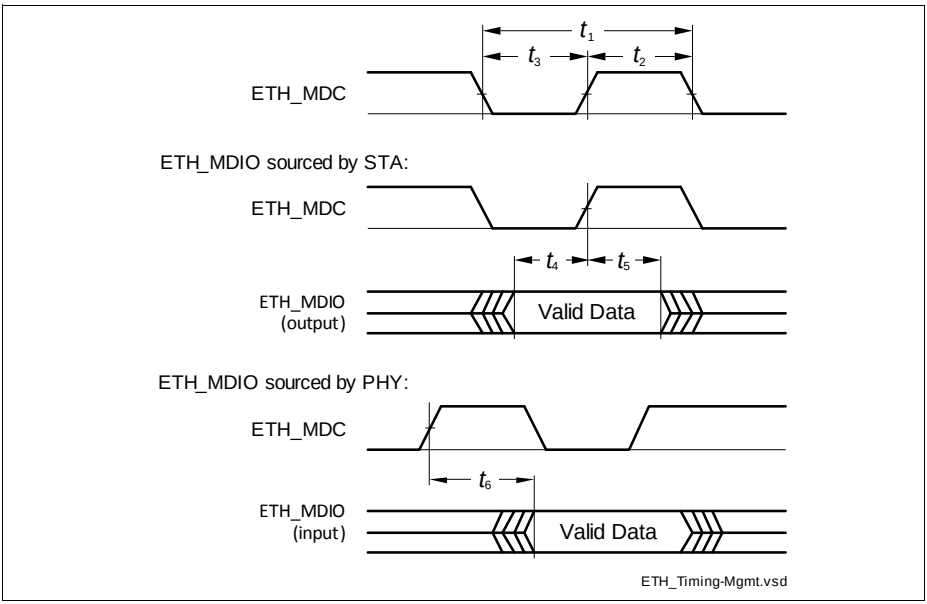

Figure 52 ETH Management Signal Timing

3.3.12.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 66 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	4	–	15	ns	

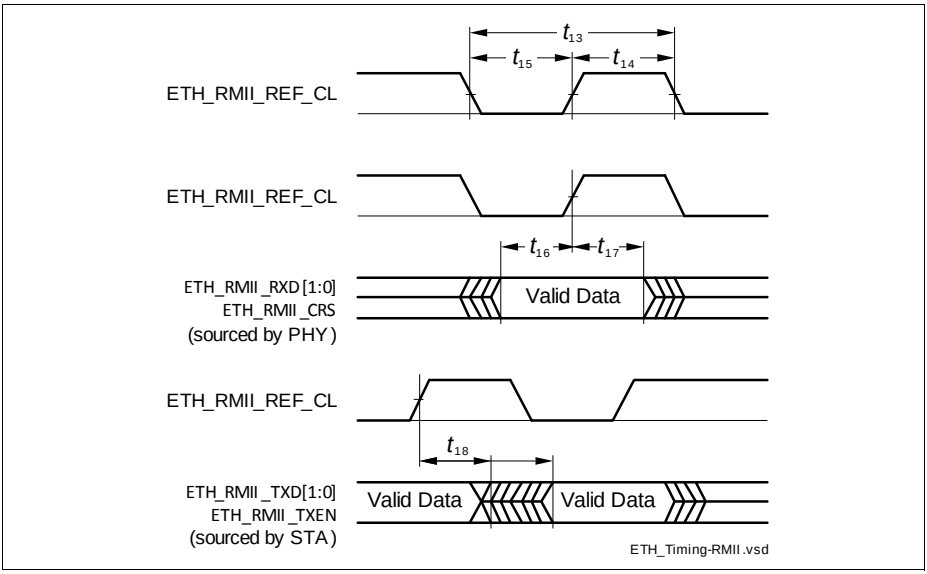

Figure 54 ETH RMII Signal Timing

3.3.13.5 Sync/Latch Timings

Table 70 Sync/Latch Timings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SYNC0/1	$t_{DC\_SYNC\_Jitter}$ SR	–	–	11 + m[1)]	ns	
LATCH0/1	t_{DC_LATCH} SR	12 + n[2)]	–	–	ns	

1) additional delay form logic and pad, number is added after characterization

2) additional shaping delay, number is added after characterization

Note: SYNC0/1 pulse length are initially loaded by EEPROM content ADR 0x0002. The actual used value can be read back from Register DC_PULSE_LEN.

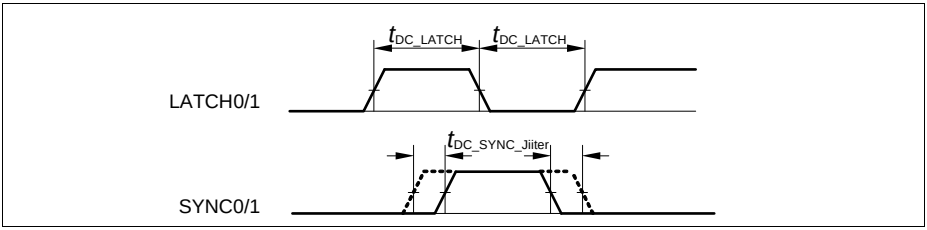

Figure 59 Sync/Latch Timings

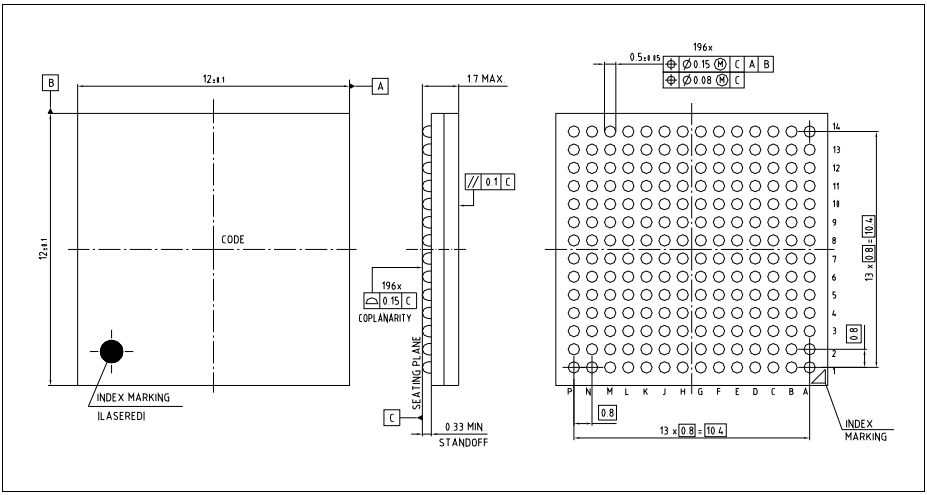

Figure 62 PG-LFBGA-196-2 (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

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