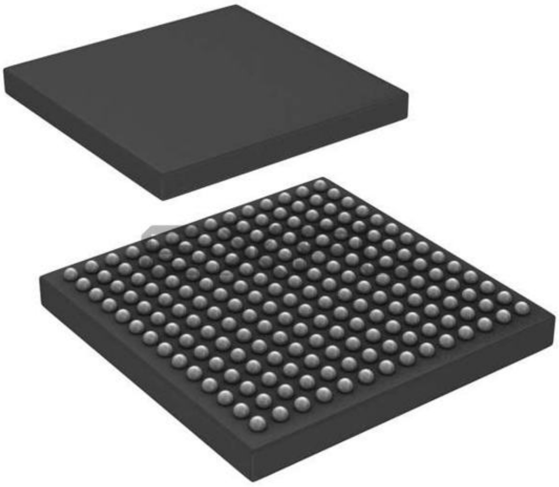

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	155
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	PG-LFBGA-196-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800e196f1536aaxqma1

XMC4700 / XMC4800

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ARM® Cortex®-M4
32-bit processor core

Data Sheet

V1.0 2016-01

Microcontrollers

XMC4[78]00 Data Sheet

Revision History: V1.0 2016-01

Previous Versions:
V0.7 2015-10 (preliminary)

Page	Subjects
8	Corrected EtherCAT features to 8 Fieldbus Memory Management Units (FMMU) and 8 Sync Manager.
46	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
53	Added HIBIO characteristics.
58	Corrected DAC INL and gain error.
70	Changed frequency dependency of the current consumption.
73	Added peripheral idle current overview.
127ff	Updated package parameters and drawings.
132	Higher HBM and CDM ESD limits.

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Table 3 Features of XMC4[78]00 Device Types (cont'd)

Derivative[1)]	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4800-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1024	24	4	2	4 x 4	2 x 4	2

1) x is a placeholder for the supported temperature range.

1.4 Definition of Feature Variants

The XMC4[78]00 types are offered with several memory sizes and number of available VADC channels. **Table 4** describes the location of the available Flash memory, **Table 5** describes the location of the available SRAMs, **Table 6** the available VADC channels.

Table 4 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
1,024 Kbytes	$0800\ 0000_H$ – $080F\ FFFF_H$	$0C00\ 0000_H$ – $0C0F\ FFFF_H$
1,536 Kbytes	$0800\ 0000_H$ – $0817\ FFFF_H$	$0C00\ 0000_H$ – $0C17\ FFFF_H$
2,048 Kbytes	$0800\ 0000_H$ – $081F\ FFFF_H$	$0C00\ 0000_H$ – $0C1F\ FFFF_H$

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

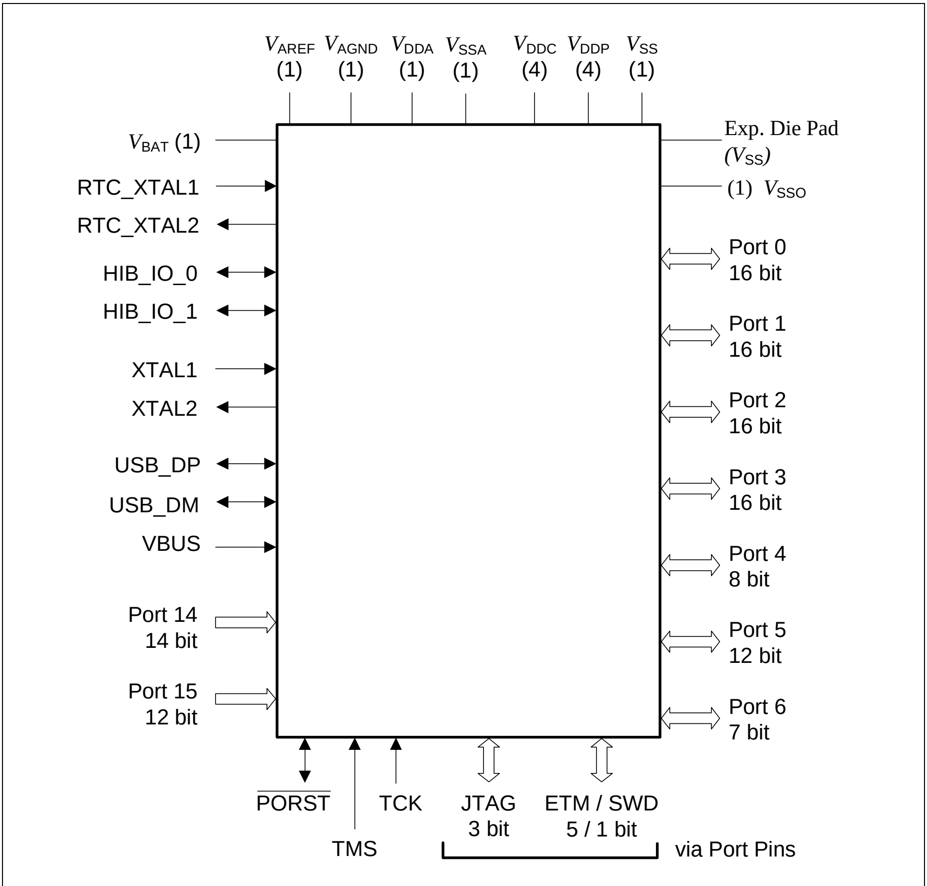

Figure 2 XMC4[78]00 Logic Symbol PG-LQFP-144

2.2.1 Package Pin Summary

The following general scheme is used to describe each pin:

Table 9 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type	Notes
Name	N	Ax	...	A2	

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the dedicated pins (i.e. PORST) and supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type (A1, A1+, A2, special=special pad, In=input pad, AN/DIG_IN=analog and digital input, Power=power supply). Details about the pad properties are defined in the Electrical Parameters.

In the “Notes”, special information to the respective pin/function is given, i.e. deviations from the default configuration after reset. Per default the regular Port pins are configured as direct input with no internal pull device active.

Table 10 Package Pin Mapping

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.0	E4	2	2	A1+	
P0.1	E3	1	1	A1+	
P0.2	C3	144	100	A2	
P0.3	C4	143	99	A2	
P0.4	D5	142	98	A2	
P0.5	C5	141	97	A2	
P0.6	C6	140	96	A2	
P0.7	D7	128	89	A2	After a system reset, via HWSEL this pin selects the DB.TDI function.
P0.8	C8	127	88	A2	After a system reset, via HWSEL this pin selects the DB.TRST function, with a weak pull-down active.
P0.9	F4	4	4	A2	
P0.10	D4	3	3	A1+	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P8.9			CCU81. OUT33						ECAT0. P1_RX_ERRC							
P8.10			CCU81. OUT21						ECAT0. P1_RX_CLKC							
P8.11			CCU81. OUT11						ECAT0. P1_RX_DVC							
P9.0		U2C0. SELO0		ECAT0. SYNC0					ECAT0. LATCH0B	U2C0. DX2C	ECAT0. P1_TX_CLKC					
P9.1		U2C0. SCLKOUT		ECAT0. SYNC1					ECAT0. LATCH1B	U2C0. DX1C	ECAT0. P0_TX_CLKC					
P9.2		U2C0. SELO1		ECAT0. PHY_RST					ETH0. COLC							
P9.3		U2C0. DOUT0		ECAT0. PHY_CLK25					ETH0. CRSC							
P9.4	ECAT0. LED_STATE_RU N			ECAT0. LED_RUN						U2C0. DX0E						
P9.5		U2C0. SELO2		ECAT0. LED_ERR					ETH0. RXD2C							
P9.6		U2C0. SELO3		ECAT0. MCLK					ETH0. RXD3C							
P9.7		U2C0. SELO4			ECAT0. MDO		ECAT0. MDIC		ETH0. RXERC							
P9.8				ECAT0. P0_LINK_ACT						U2C1. DX2C						
P9.9				ECAT0. P1_LINK_ACT						U2C1. DX1C						
P9.10		U2C1. DOUT0							ECAT0. P0_LINKC							
P9.11		U2C1. SELO3							ECAT0. P1_LINKC							
P14.0									VADC. G0CH0							
P14.1									VADC. G0CH1							
P14.2									VADC. G0CH2	VADC. G1CH2						
P14.3									VADC. G0CH3	VADC. G1CH3			CAN. N0_RXDB			
P14.4									VADC. G0CH4		VADC. G2CH0				CAN. N4_RXDB	ECAT0. LATCH1A
P14.5									VADC. G0CH5		VADC. G2CH1		POSIF0. IN2B			ECAT0. LATCH0A
P14.6									VADC. G0CH6				POSIF0. IN1B		G0ORC6	ECAT0. P1_RX_CLKB
P14.7									VADC. G0CH7				POSIF0. IN0B		G0ORC7	ECAT0. P1_RXD0B

Table 14 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV} SR	-5	–	5	mA	
Absolute sum of all input circuit currents for one port group during overload condition[1]	I_{OVG} SR	–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} < 0$ mA
		–	–	20	mA	$\Sigma\|I_{OVx}\|$, for all $I_{OVx} > 0$ mA
Absolute sum of all input circuit currents during overload condition	I_{OVS} SR	–	–	80	mA	ΣI_{OVG}

1) The port groups are defined in **Table 17**.

Figure 11 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

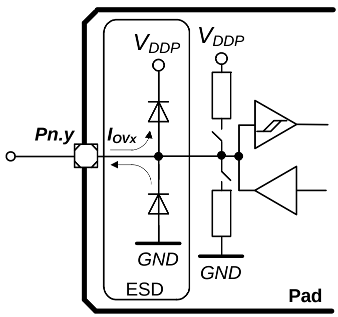

Figure 11 Input Overload Current via ESD structures

Table 15 and **Table 16** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZHIB} CC	-500	500	nA	$0 V \leq V_{IN} \leq V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$	$V_{BAT} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3	$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$	–	V	$V_{BAT} \geq 3.13$ V
		$0.06 \times V_{BAT}$	–	V	$V_{BAT} < 3.13$ V
Output high voltage, POD[1] = medium	V_{OHHIB} CC	$V_{BAT} - 0.4$	–	V	$I_{OH} \geq -1.4$ mA
Output low voltage	V_{OLHIB} CC	–	0.4	V	$I_{OL} \leq 2$ mA
Fall time	t_{FHIB} CC	–	50	ns	$V_{BAT} \geq 3.13$ V $C_L = 50$ pF
		–	100	ns	$V_{BAT} < 3.13$ V $C_L = 50$ pF
Rise time	t_{RHIB} CC	–	50	ns	$V_{BAT} \geq 3.13$ V $C_L = 50$ pF
		–	100	ns	$V_{BAT} < 3.13$ V $C_L = 50$ pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.3 AC Parameters

3.3.1 Testing Waveforms

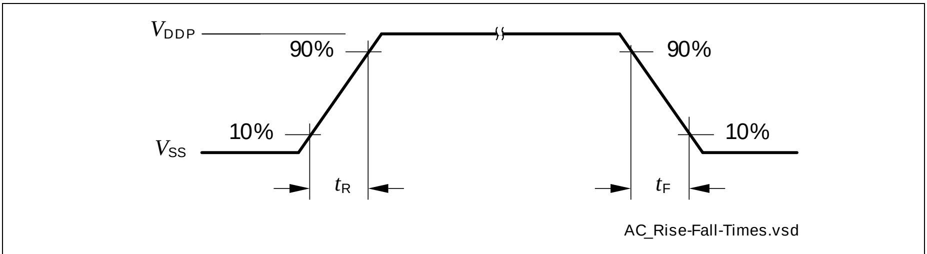

Figure 22 Rise/Fall Time Parameters

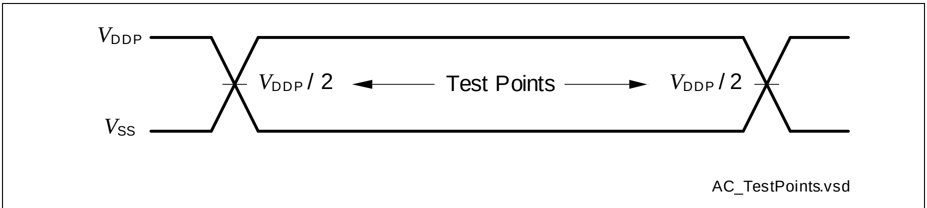

Figure 23 Testing Waveform, Output Delay

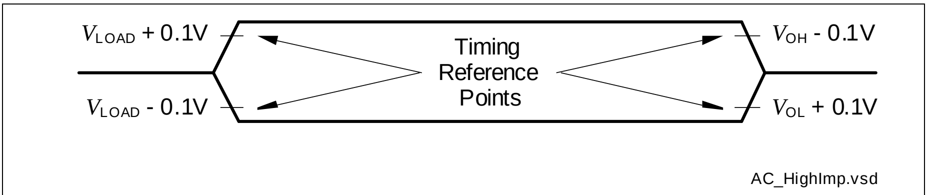

Figure 24 Testing Waveform, Output High Impedance

2) Maximum threshold for reset deassertion.
3) The V_{DDP} monitoring has a typical hysteresis of V_{PORHYS} = 180 mV.
4) If t_{PR} is not met, low spikes on $\overline{\text{PORST}}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping V_{DDP}).

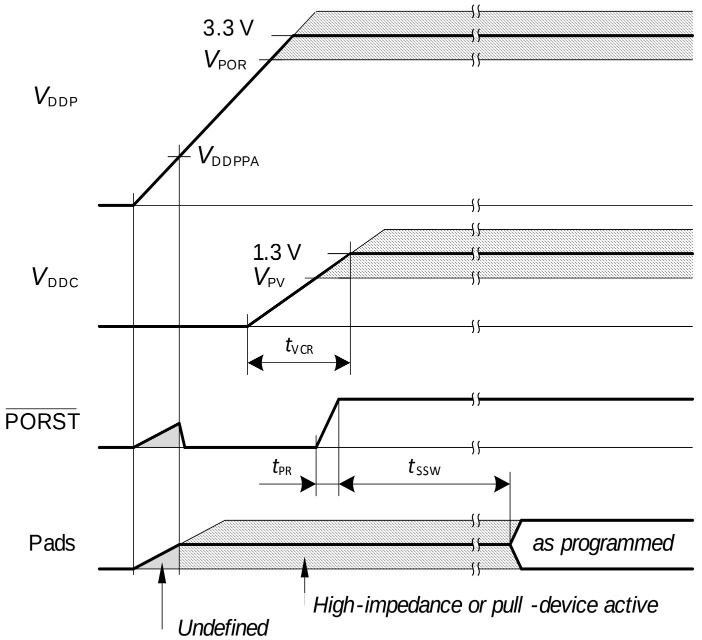

Figure 26 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU}. Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 48 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 53 SD Card Bus Timing for Full-Speed Mode[1] (cont'd)

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	0	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

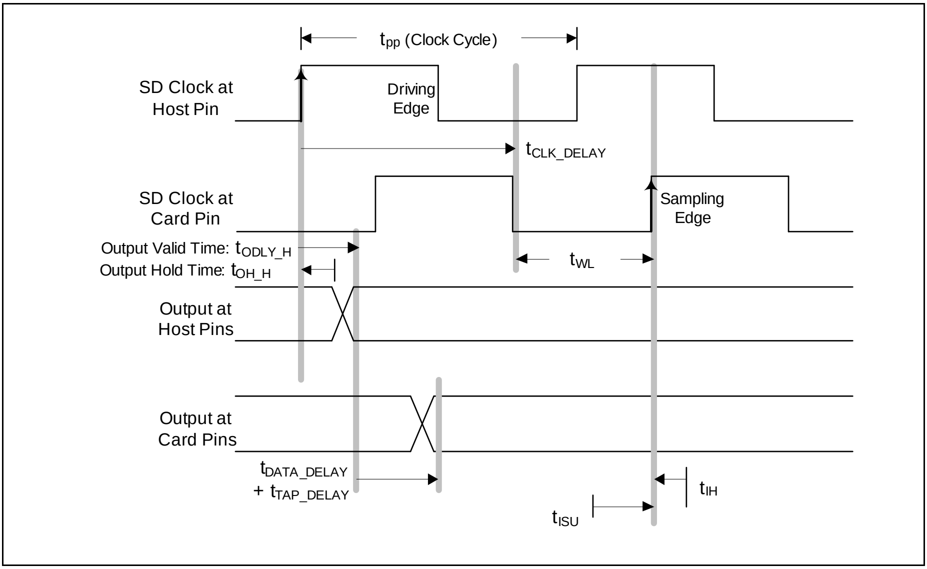

Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} \quad (1)$$

Demultiplexed Read Timing

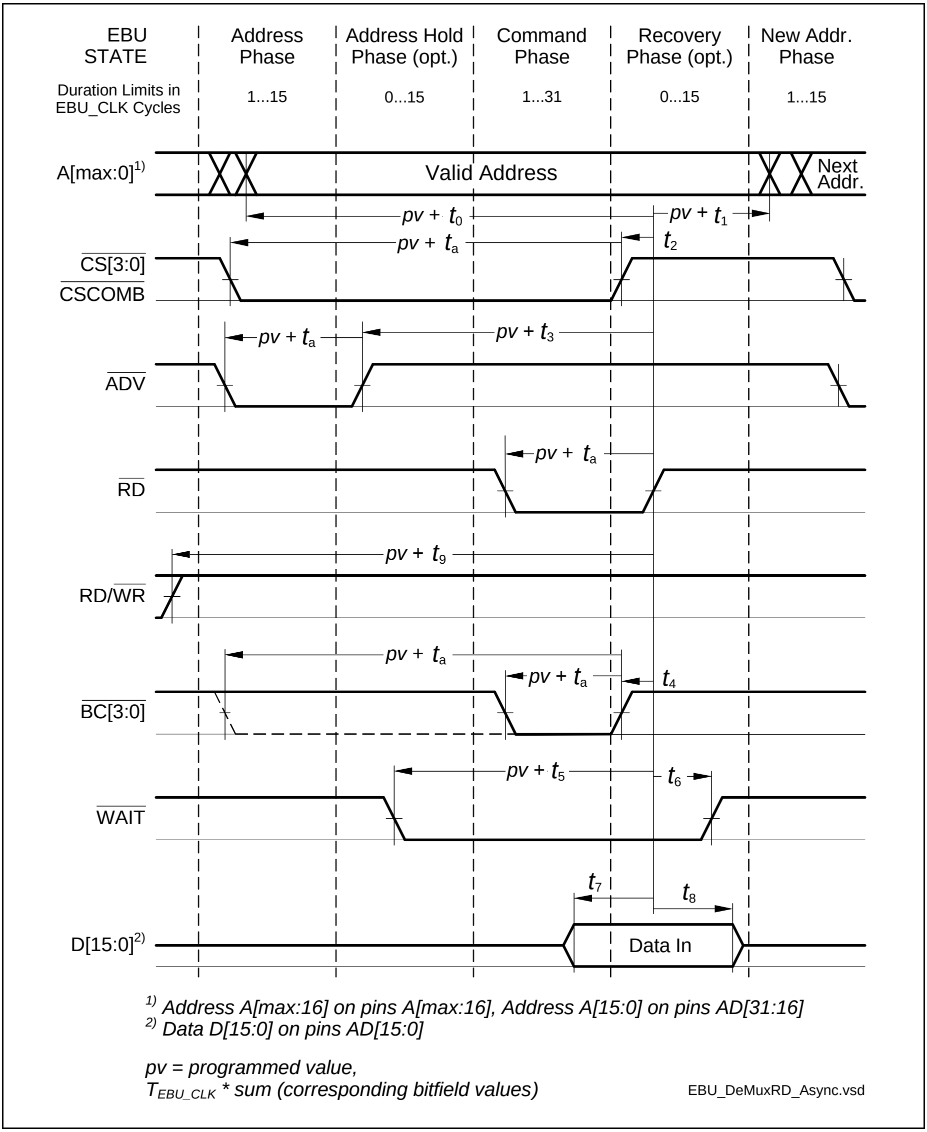

Figure 42 Demultiplexed Read Access

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS}}$(3:0) low		CC	t_8	–	9	
$\overline{\text{CS}}$(3:0) high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC}}$(3:0) low		CC	t_{16}	–	9	
$\overline{\text{BC}}$(3:0) high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1)]		CC	t_{22}	–	7	
CKE output hold[1)]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

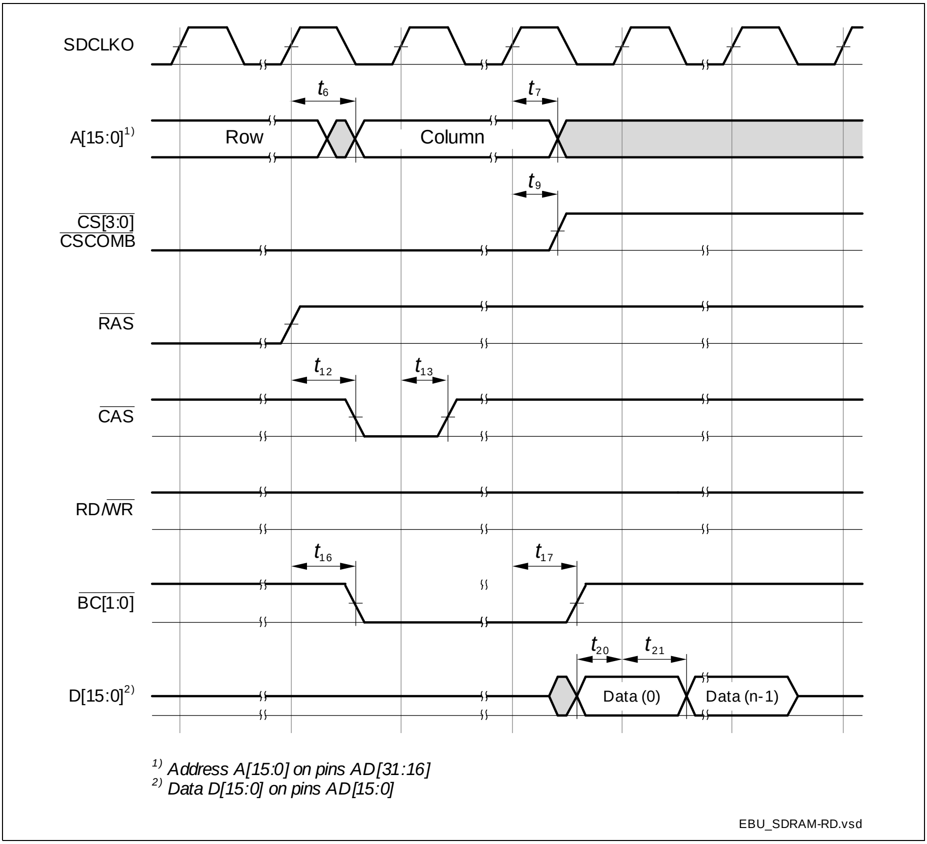

Figure 48 EBU SDRAM Read Access Timing

3.3.11 USB Interface Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 63 USB Timing Parameters (operating conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Rise time	t_R	CC	4	–	20	ns	C_L = 50 pF
Fall time	t_F	CC	4	–	20	ns	C_L = 50 pF
Rise/Fall time matching	t_R/t_F	CC	90	–	111.11	%	C_L = 50 pF
Crossover voltage	V_{CRS}	CC	1.3	–	2.0	V	C_L = 50 pF

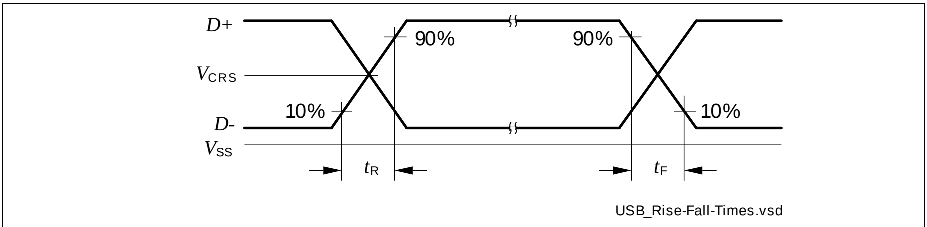

Figure 50 USB Signal Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

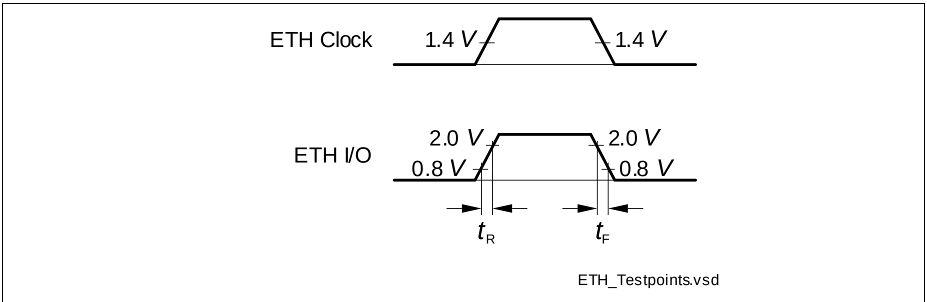

Figure 51 ETH Measurement Reference Points

4 Package and Reliability

The XMC4[78]00 is a member of the XMC4000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the Exposed Die Pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 71 provides the thermal characteristics of the packages used in XMC4[78]00.

Table 71 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad dimensions including U-Groove	Ex × Ey CC	-	7.0 × 7.0	mm	PG-LQFP-144-24
		-	7.0 × 7.0	mm	PG-LQFP-100-25
Exposed Die Pad dimensions excluding U-Groove	Ax × Ay CC	-	6.2 × 6.2	mm	PG-LQFP-144-24
		-	6.2 × 6.2	mm	PG-LQFP-100-25
Thermal resistance Junction-Ambient $T_J \leq 150$ °C	$R_{\Theta JA}$ CC	-	27.0	K/W	PG-LFBGA-196-2
		-	19.5	K/W	PG-LQFP-144-24[1)]
		-	22.5	K/W	PG-LQFP-100-25[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-7) with thermal vias; exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SS}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC4[78]00 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The "Thermal resistance $R_{\Theta JA}$" quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 150 °C.

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**.

The exposed die pad dimensions are listed in **Table 71**.