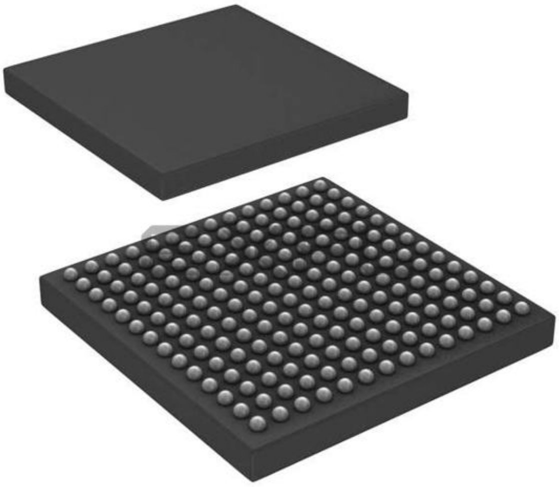


Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	155
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	196-LFBGA
Supplier Device Package	PG-LFBGA-196-2
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800e196k1536aaxqma1

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

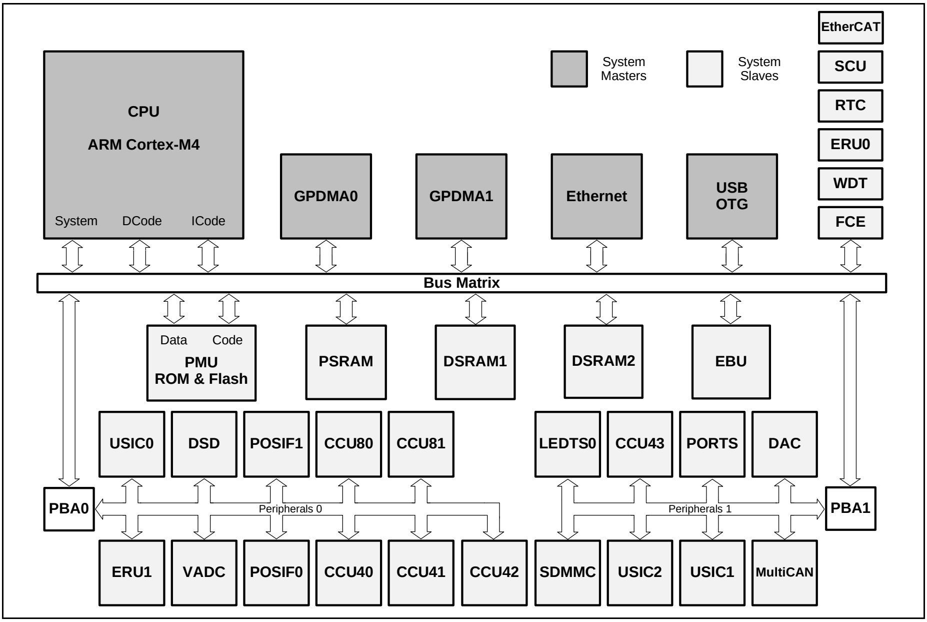


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

- Tri-stated in input mode
- Push/pull or open drain output mode
- Boundary scan test support over JTAG interface

On-Chip Debug Support

- Full support for debug features: 8 breakpoints, CoreSight, trace
- Various interfaces: ARM-JTAG, SWD, single wire trace

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC4<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - E: LFBGA
  - F: LQFP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - K: -40°C to 125°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC4[78]00 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC4[78]00 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC4[78]00** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC4[78]00 Device Types

Derivative[1]	Package	Flash Kbytes	SRAM Kbytes
XMC4700-E196x2048	PG-LFBGA-196	2048	352
XMC4700-F144x2048	PG-LQFP-144	2048	352
XMC4700-F100x2048	PG-LQFP-100	2048	352
XMC4700-E196x1536	PG-LFBGA-196	1536	276

Table 5 SRAM Memory Ranges

Total SRAM Size	Program SRAM	System Data SRAM	Communication Data SRAM
200 Kbytes	1FFE $E000_H$ – 1FFF $FFFF_H$	2000 0000_H – 2001 $FFFF_H$	–
276 Kbytes	1FFE 8000_H – 1FFF $FFFF_H$	2000 0000_H – 2001 $FFFF_H$	2002 0000_H – 2002 $CFFF_H$
352 Kbytes	1FFE 8000_H – 1FFF $FFFF_H$	2000 0000_H – 2001 $FFFF_H$	2002 0000_H – 2003 $FFFF_H$

Table 6 ADC Channels[1)]

Package	VADC G0	VADC G1	VADC G2	VADC G3
PG-LQFP-144 PG-LFBGA-196	CH0..CH7	CH0..CH7	CH0..CH7	CH0..CH7
PG-LQFP-100	CH0..CH7	CH0..CH7	CH0..CH3	CH0..CH3

[1)] Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.5 Identification Registers

The identification registers allow software to identify the marking.

Table 7 XMC4700 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 7001_H	EES-AA, ES-AA, AA
JTAG IDCODE	101D $F083_H$	EES-AA, ES-AA, AA

Table 8 XMC4800 Identification Registers

Register Name	Value	Marking
SCU_IDCHIP	0004 8001_H	EES-AA, ES-AA, AA
JTAG IDCODE	101D $F083_H$	EES-AA, ES-AA, AA

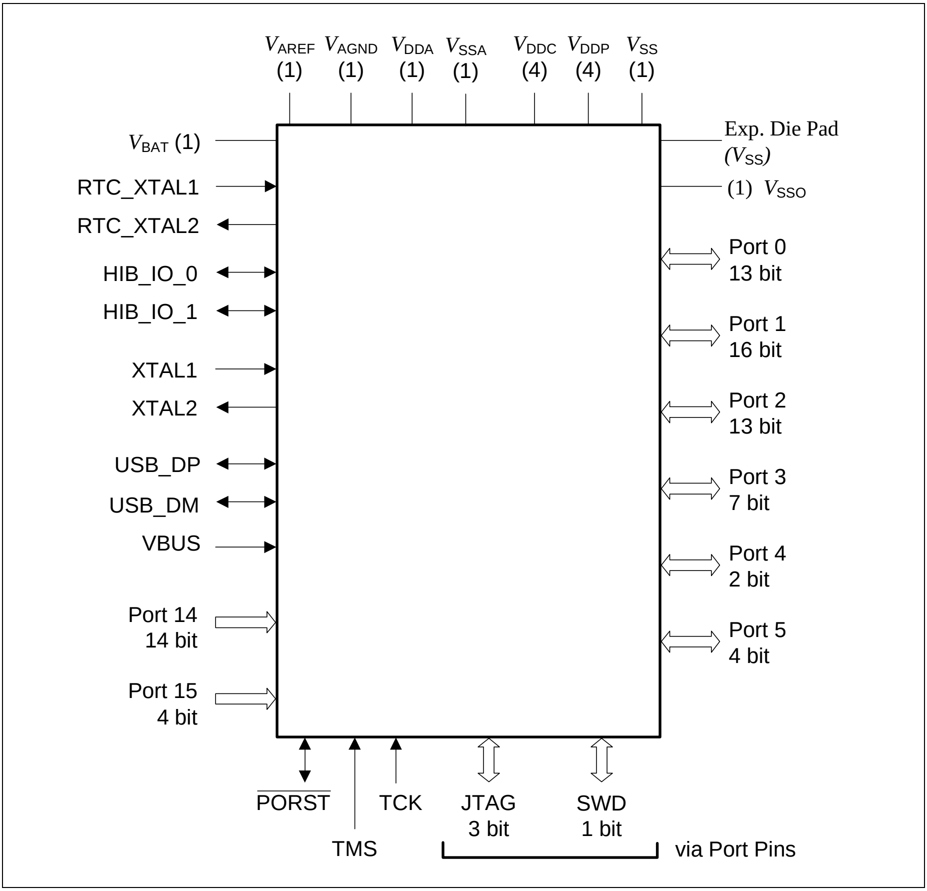


Figure 4 XMC4[78]00 Logic Symbol PG-LQFP-100

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

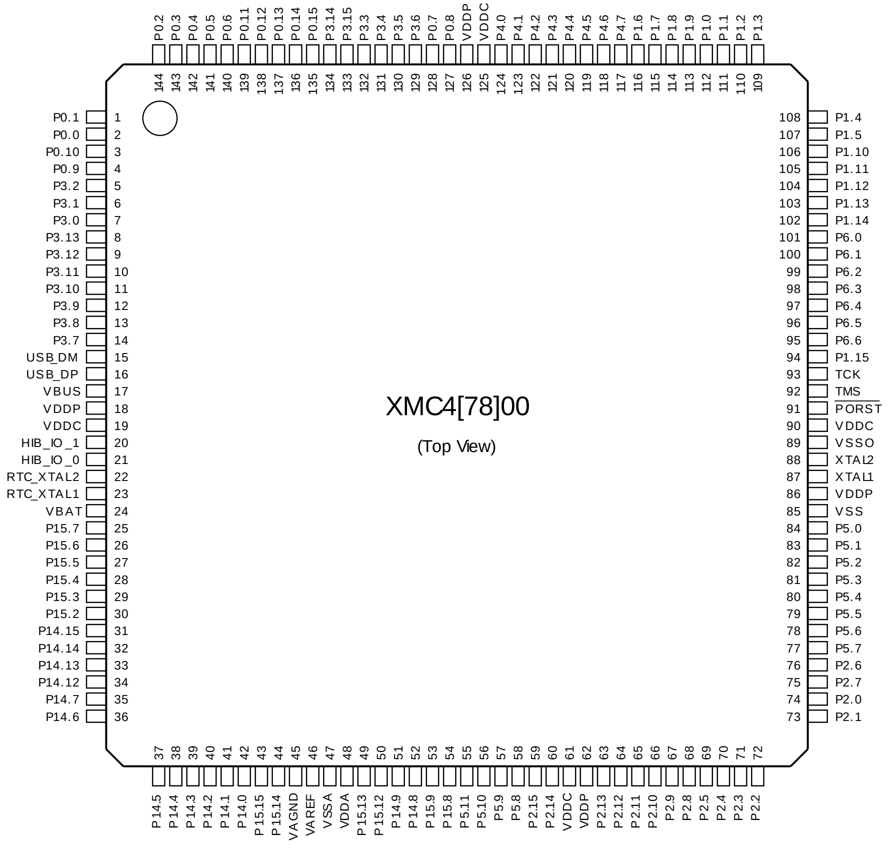


Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)

2.2.2 Port I/O Functions

The following general scheme is used to describe each Port pin:

Table 11 Port I/O Function Description

Function	Outputs			Inputs		
	ALT1	**ALTn**	**HWO0**	**HWI0**	**Input**	**Input**
P0.0		MODA.OUT	MODB.OUT	MODB.INA	MODC.INA	
Pn.y	MODA.OUT				MODA.INA	MODC.INB

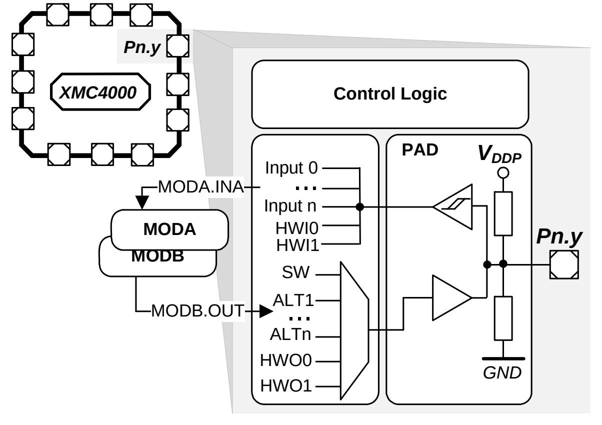


Figure 8 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to four alternate output functions (ALT1/2/3/4) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.
The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

By Pn_HWSEL it is possible to select between different hardware “masters” (HWO0/HWI0). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers.

Table 12 Port I/O Functions (cont’d)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P14.8					DAC.OUT_0					VADC.G1CH0		VADC.G3CH2	ETH0.RXD0C			
P14.9					DAC.OUT_1					VADC.G1CH1		VADC.G3CH3	ETH0.RXD1C			
P14.12										VADC.G1CH4						ECAT0.P1_RXD1B
P14.13										VADC.G1CH5						ECAT0.P1_RXD2B
P14.14										VADC.G1CH6					G1ORC6	ECAT0.P1_RXD3B
P14.15										VADC.G1CH7					G1ORC7	ECAT0.P1_RX_DVB
P15.2											VADC.G2CH2					ECAT0.P1_RX_ERRB
P15.3											VADC.G2CH3					ECAT0.P1_LINKB
P15.4											VADC.G2CH4					
P15.5											VADC.G2CH5					
P15.6											VADC.G2CH6					
P15.7											VADC.G2CH7					
P15.8												VADC.G3CH0	ETH0.CLK_RMIIC			ETH0.CLKRXC
P15.9												VADC.G3CH1	ETH0.CRS_DVC			ETH0.RXDVC
P15.12												VADC.G3CH4				
P15.13												VADC.G3CH5				
P15.14												VADC.G3CH6				
P15.15												VADC.G3CH7				
HIB_IO_0	HIBOUT	WWDT.SERVICE_OUT							WAKEUPA							
HIB_IO_1	HIBOUT	WWDT.SERVICE_OUT							WAKEUPB							
USB_DP																
USB_DM																
TCK							DB.TCK/SWCLK									
TMS					DB.TMS/SWDIO											
$\overline{\text{PORST}}$																

Table 12 **Port I/O Functions** (cont'd)

Function	Outputs						Inputs											
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F		
XTAL2																
RTC_XTAL1											ERU0. 1B1					
RTC_XTAL2																

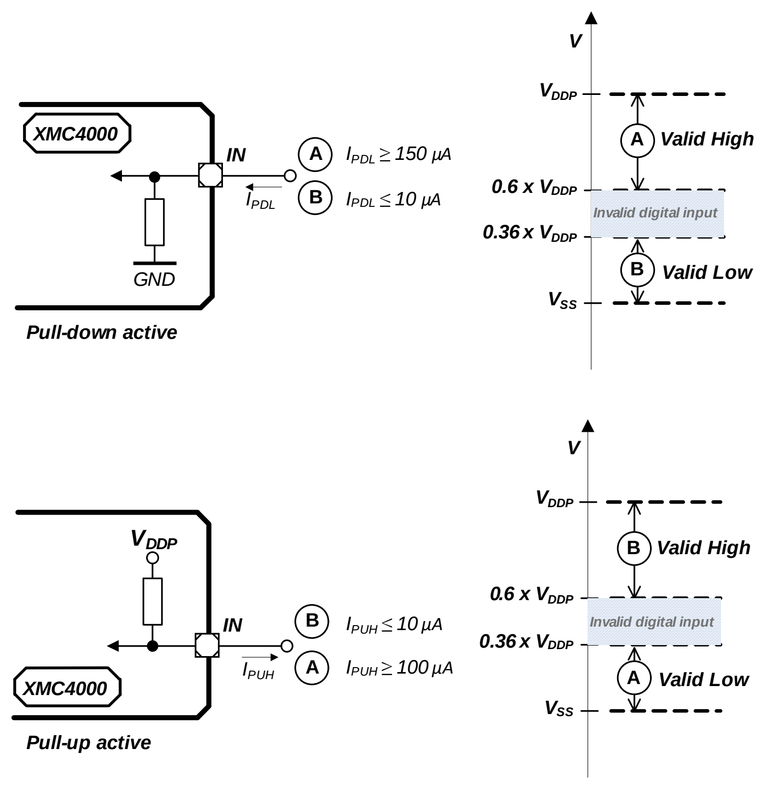


Figure 13 Pull Device Input Characteristics

Figure 13 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		**Max.**		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0\text{ V} \leq V_{\text{IN}} \leq V_{\text{BAT}}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{\text{BAT}}$		$V_{\text{BAT}} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{\text{BAT}}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{\text{BAT}}$		–	V	$V_{\text{BAT}} \geq 3.13\text{ V}$
		$0.06 \times V_{\text{BAT}}$		–	V	$V_{\text{BAT}} < 3.13\text{ V}$
Output high voltage, POD[1] = medium	V_{OHHIB} CC	$V_{\text{BAT}} - 0.4$		–	V	$I_{\text{OH}} \geq -1.4\text{ mA}$
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{\text{OL}} \leq 2\text{ mA}$
Fall time	t_{FHIB} CC	–		50	ns	$V_{\text{BAT}} \geq 3.13\text{ V}$ $C_{\text{L}} = 50\text{ pF}$
		–		100	ns	$V_{\text{BAT}} < 3.13\text{ V}$ $C_{\text{L}} = 50\text{ pF}$
Rise time	t_{RHIB} CC	–		50	ns	$V_{\text{BAT}} \geq 3.13\text{ V}$ $C_{\text{L}} = 50\text{ pF}$
		–		100	ns	$V_{\text{BAT}} < 3.13\text{ V}$ $C_{\text{L}} = 50\text{ pF}$

---

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 27 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error	ED_{OFF} CC		±20		mV	
Gain error	ED_{G_IN} CC	-6.5	-1.5	3	%	
Startup time	$t_{STARTUP}$ CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1} CC	2.5	5	–	MHz	verified by design
Output sourcing current	I_{OUT_SOURCE} CC	–	-30	–	mA	
Output sinking current	I_{OUT_SINK} CC	–	0.6	–	mA	
Output resistance	R_{OUT} CC	–	50	–	Ohm	
Load resistance	R_L SR	5	–	–	kOhm	
Load capacitance	C_L SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR* CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD* CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR* CC	–	56	–	dB	to V_{DDA} verified by design

Conversion Calculation

Unsigned:
DACxDATA = $4095 \times (V_{OUT} - V_{OUT\_MIN}) / (V_{OUT\_MAX} - V_{OUT\_MIN})$

Signed:
DACxDATA = $4095 \times (V_{OUT} - V_{OUT\_MIN}) / (V_{OUT\_MAX} - V_{OUT\_MIN}) - 2048$

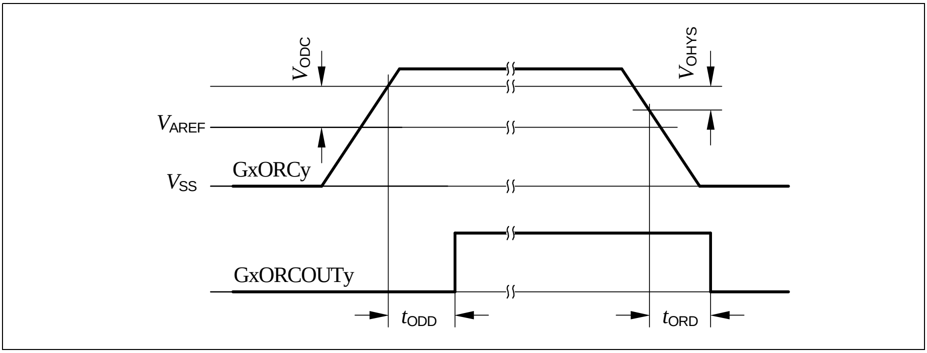


Figure 18 GxORCOUTy Trigger Generation

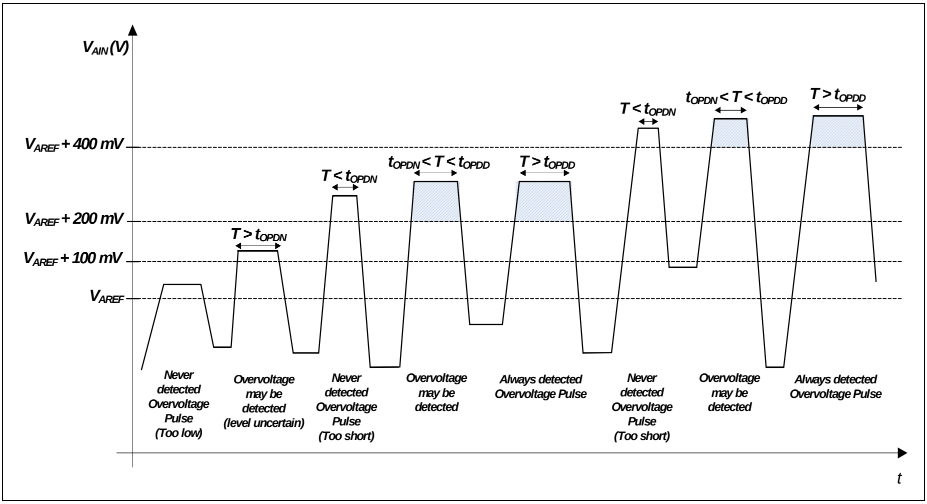


Figure 19 ORC Detection Ranges

Table 31 **USB OTG Data Line (USB_DP, USB_DM) Parameters** (Operating Conditions apply)

Parameter	**Symbol**		**Values**			**Unit**	**Note / Test Condition**
			Min.	**Typ.**	**Max.**		
Input low voltage	V_{IL}	SR	–	–	0.8	V	
Input high voltage (driven)	V_{IH}	SR	2.0	–	–	V	
Input high voltage (floating) [1]	V_{IHZ}	SR	2.7	–	3.6	V	
Differential input sensitivity	V_{DIS}	CC	0.2	–	–	V	
Differential common mode range	V_{CM}	CC	0.8	–	2.5	V	
Output low voltage	V_{OL}	CC	0.0	–	0.3	V	1.5 kOhm pull-up to 3.6 V
Output high voltage	V_{OH}	CC	2.8	–	3.6	V	15 kOhm pull-down to 0 V
DP pull-up resistor (idle bus)	R_{PUI}	CC	900	–	1 575	Ohm	
DP pull-up resistor (upstream port receiving)	R_{PUA}	CC	1 425	–	3 090	Ohm	
DP, DM pull-down resistor	R_{PD}	CC	14.25	–	24.8	kOhm	
Input impedance DP, DM	Z_{INP}	CC	300	–	–	kOhm	$0\ V \leq V_{IN} \leq V_{DDP}$
Driver output resistance DP, DM	Z_{DRV}	CC	28	–	44	Ohm	

1) Measured at A-connector with 1.5 kOhm ± 5% to 3.3 V ± 0.3 V connected to USB_DP or USB_DM and at B-connector with 15 kOhm ± 5% to ground connected to USB_DP and USB_DM.

1) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes an additional time of 5.5 ms.
2) The following formula applies to the wait state configuration: FCON.WSPFLASH × (1 / f_{CPU}) ≥ t_a.
3) Storage and inactive time included.
4) Values given are valid for an average weighted junction temperature of T_J = 110°C.
5) Only valid with robust EEPROM emulation algorithm, equally cycling the logical sectors. For more details see the Reference Manual.

Table 38 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition $C = 100$ nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 144 MHz, main PLL f_{VCO} = 288 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 72 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 4 - 3 - 2)
24 MHz - 48 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 3 - 2)
24 MHz - 72 MHz - 144 MHz (K2 steps 12 - 4 - 2)

3.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 42 JTAG Interface Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	
TCK high time	t_2 SR	10	–	–	ns	
TCK low time	t_3 SR	10	–	–	ns	
TCK clock rise time	t_4 SR	–	–	4	ns	
TCK clock fall time	t_5 SR	–	–	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
		3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1][2]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4[78]00 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ *pF.*

Table 44 ETM Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TRACECLK period	t_1	CC	13.8	–	–	ns	–
TRACECLK high time	t_2	CC	2	–	–	ns	–
TRACECLK low time	t_3	CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4	CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5	CC	–	–	3	ns	–
TRACEDATA output valid time	t_6	CC	-2	–	3	ns	–

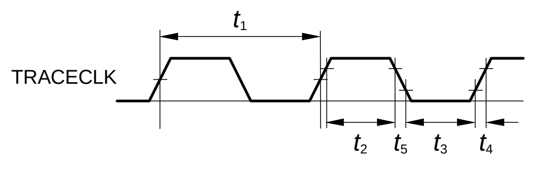


Figure 30 ETM Clock Timing

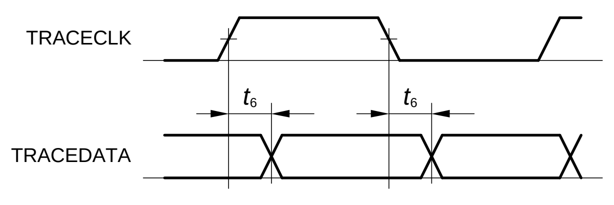


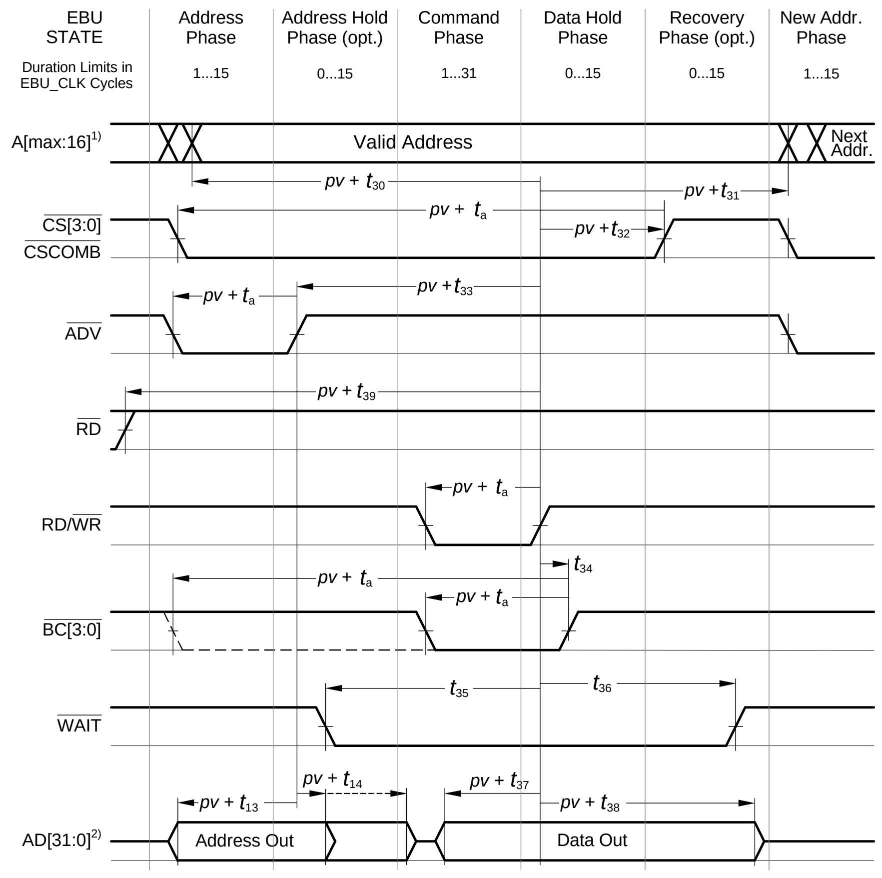
Figure 31 ETM Data Timing

Table 47 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10}	SR	3	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1]	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1]	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1]	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

Multiplexed Write Timing



[1] For 16-bit MUX and Twin 16-bit MUX only

[2] * 16-bit MUX: - Address A[15:0], Data D[15:0] on pins AD[15:0] only
* Twin 16-Bit MUX: - Address A[15:0] on pins AD[15:0] and AD[31:16] in parallel
- Data D[31:0] on pins AD[31:0]
* 32-bit MUX: - Address A[24:0] on pins AD[24:0]
- Data D[31:0] on pins AD[31:0]

pv = programmed value,
*T_{EBU_CLK} * sum (corresponding bitfield values)*

EBU_MuxWR_Async.vsd

Figure 43 Multiplexed Write Access

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS(3:0)}}$ low		CC	t_8	–	9	
$\overline{\text{CS(3:0)}}$ high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC(3:0)}}$ low		CC	t_{16}	–	9	
$\overline{\text{BC(3:0)}}$ high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1]		CC	t_{22}	–	7	
CKE output hold[1]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

[1] Not depicted in the read and write access timing figures below.