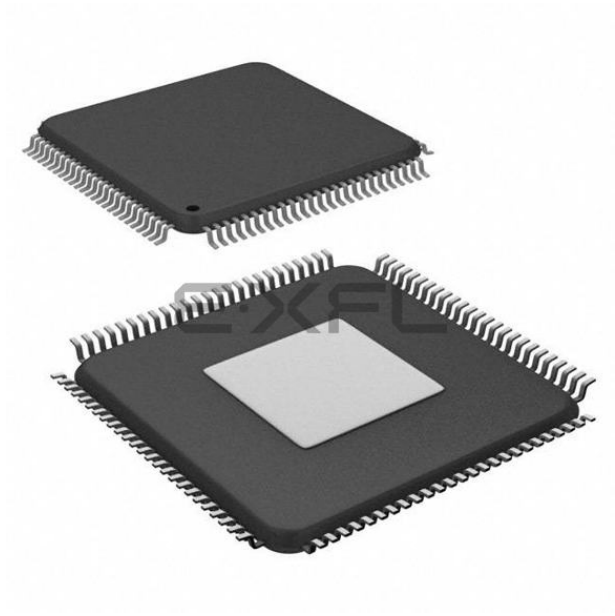
Infineon Technologies - XMC4800F100F1536AAXQMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	75
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-25
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800f100f1536aaxqma1

XMC4700 / XMC4800

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM® Cortex®-M4
32-bit processor core

Data Sheet

V1.0 2016-01

Microcontrollers

XMC4[78]00 Data Sheet

Revision History: V1.0 2016-01

Previous Versions:
V0.7 2015-10 (preliminary)

Page	Subjects
8	Corrected EtherCAT features to 8 Fieldbus Memory Management Units (FMMU) and 8 Sync Manager.
46	Added footnote explaining minimum V_{BAT} requirements to start the hibernate domain and/or oscillation of a crystal on RTC_XTAL.
53	Added HIBIO characteristics.
58	Corrected DAC INL and gain error.
70	Changed frequency dependency of the current consumption.
73	Added peripheral idle current overview.
127ff	Updated package parameters and drawings.
132	Higher HBM and CDM ESD limits.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

On-Chip Memories

- 16 KB on-chip boot ROM
- 96 KB on-chip high-speed program memory
- 128 KB on-chip high speed data memory
- 128 KB on-chip high-speed communication memory
- 2,048 KB on-chip Flash Memory with 8 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- EtherCATSlave interface (ECAT) capable of 100 Mbit/s transfer rates with 2 MII ports, 8 Fieldbus Memory Management Units (FMMU), 8 Sync Manager, 64 bit distributed clocks
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 6 nodes, 256 message objects (MO), data rate up to 1 MBaud
- Six Universal Serial Interface Channels (USIC),providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability

Table 1 Synopsis of XMC4[78]00 Device Types (cont'd)

Derivative[1)]	Package	Flash Kbytes	SRAM Kbytes
XMC4700-F144x1536	PG-LQFP-144	1536	276
XMC4700-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x2048	PG-LFBGA-196	2048	352
XMC4800-F144x2048	PG-LQFP-144	2048	352
XMC4800-F100x2048	PG-LQFP-100	2048	352
XMC4800-E196x1536	PG-LFBGA-196	1536	276
XMC4800-F144x1536	PG-LQFP-144	1536	276
XMC4800-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x1024	PG-LFBGA-196	1024	200
XMC4800-F144x1024	PG-LQFP-144	1024	200
XMC4800-F100x1024	PG-LQFP-100	1024	200

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4[78]00 Device Types

Derivative[1)]	LEDTS Intf.	SDMMC Intf.	EBU Intf.[2)]	ETH Intf.[3)]	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4700-E196x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x2048	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-E196x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x1536	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]

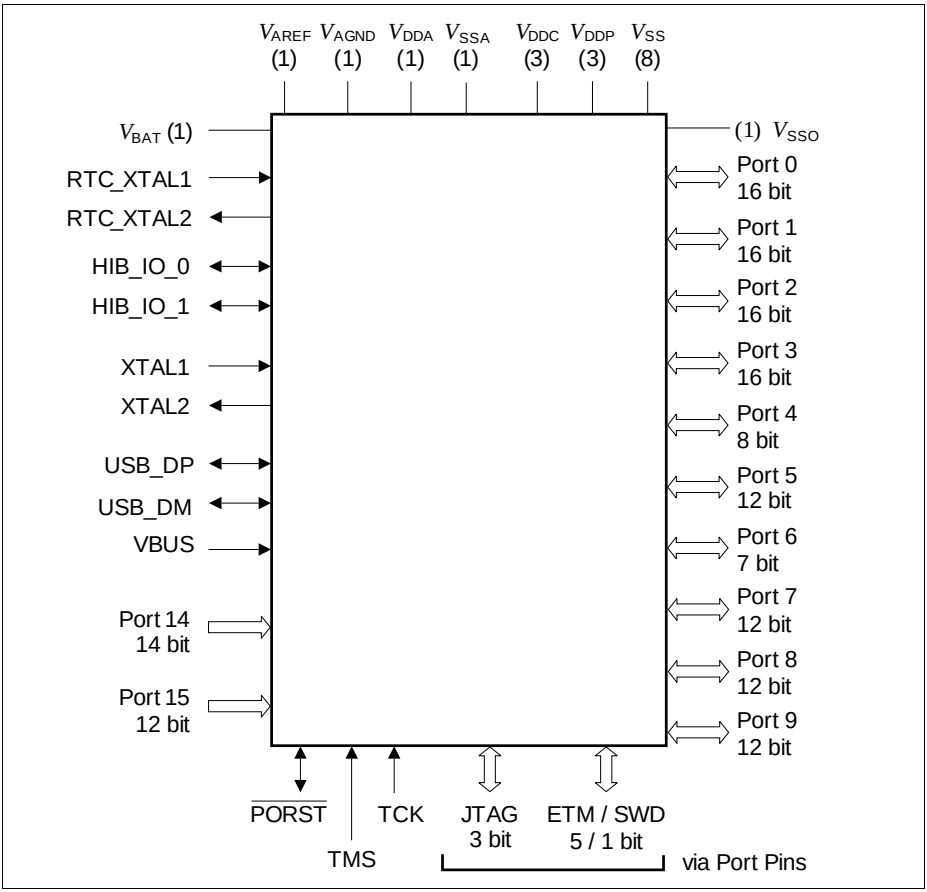

Figure 3 XMC4[78]00 Logic Symbol PG-LFBGA-196

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P8.5	B5	-	-	A1+	
P8.6	A2	-	-	A1+	
P8.7	B4	-	-	A1+	
P8.8	A3	-	-	A2	
P8.9	A5	-	-	A1+	
P8.10	A4	-	-	A1+	
P8.11	A6	-	-	A1+	
P9.0	F13	-	-	A2	
P9.1	E14	-	-	A2	
P9.2	D14	-	-	A1+	
P9.3	D13	-	-	A2	
P9.4	A12	-	-	A1+	
P9.5	A11	-	-	A1+	
P9.6	B11	-	-	A1+	
P9.7	A9	-	-	A1+	
P9.8	A8	-	-	A1+	
P9.9	A10	-	-	A1+	
P9.10	B8	-	-	A1+	
P9.11	B9	-	-	A1+	
P14.0	N3	42	31	AN/DIG_IN	
P14.1	N2	41	30	AN/DIG_IN	
P14.2	M3	40	29	AN/DIG_IN	
P14.3	L4	39	28	AN/DIG_IN	
P14.4	M1	38	27	AN/DIG_IN	
P14.5	M2	37	26	AN/DIG_IN	
P14.6	L3	36	25	AN/DIG_IN	
P14.7	L2	35	24	AN/DIG_IN	
P14.8	P5	52	37	AN/DAC/DIG_IN	
P14.9	N5	51	36	AN/DAC/DIG_IN	
P14.12	L1	34	23	AN/DIG_IN	
P14.13	K4	33	22	AN/DIG_IN	

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 13 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1)]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

1) The port groups are defined in **Table 17**.

Figure 10 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

3.2.9 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 36 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per 256 Kbyte Sector	t_{ERP} CC	–	5	5.5	s	
Erase Time per 64 Kbyte Sector	t_{ERP} CC	–	1.2	1.4	s	
Erase Time per 16 Kbyte Logical Sector	t_{ERP} CC	–	0.3	0.4	s	
Program time per page[1]	t_{PRP} CC	–	5.5	11	ms	
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Wake-up time	t_{WU} CC	–	–	270	µs	
Read access time	t_a CC	22	–	–	ns	For operation with 1 / f_{CPU} < t_a wait states must be configured[2]
Data Retention Time, Physical Sector[3][4]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Data Retention Time, Logical Sector[3][4]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
Data Retention Time, User Configuration Block (UCB)[3][4]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Endurance on 64 Kbyte Physical Sector PS4	N_{EPS4} CC	10000	–	–	cycles	Cycling distributed over life time[5]

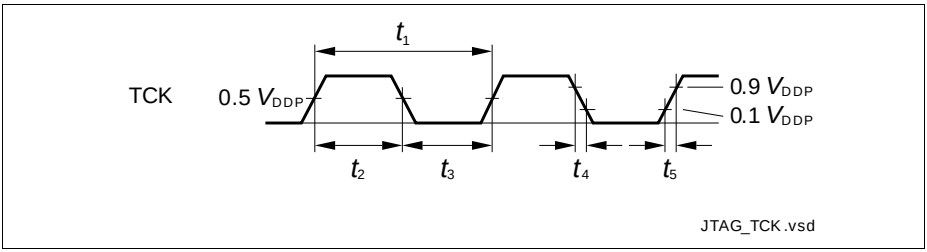

Figure 27 Test Clock Timing (TCK)

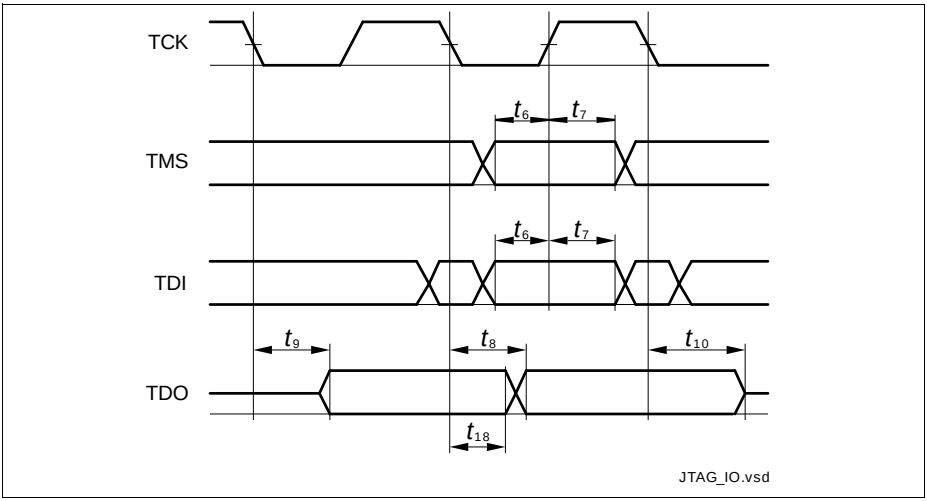

Figure 28 JTAG Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4[78]00 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 44 ETM Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TRACECLK period	t_1	CC	13.8	–	–	ns	–
TRACECLK high time	t_2	CC	2	–	–	ns	–
TRACECLK low time	t_3	CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4	CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5	CC	–	–	3	ns	–
TRACEDATA output valid time	t_6	CC	-2	–	3	ns	–

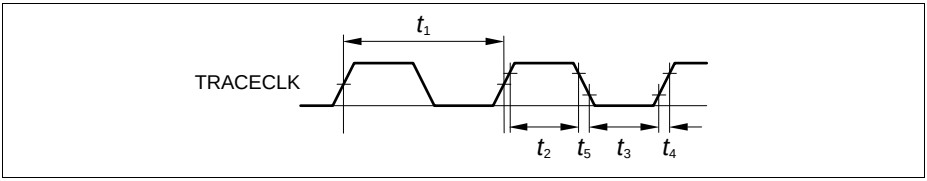

Figure 30 ETM Clock Timing

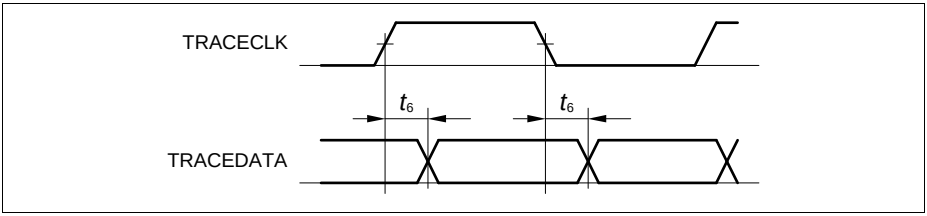

Figure 31 ETM Data Timing

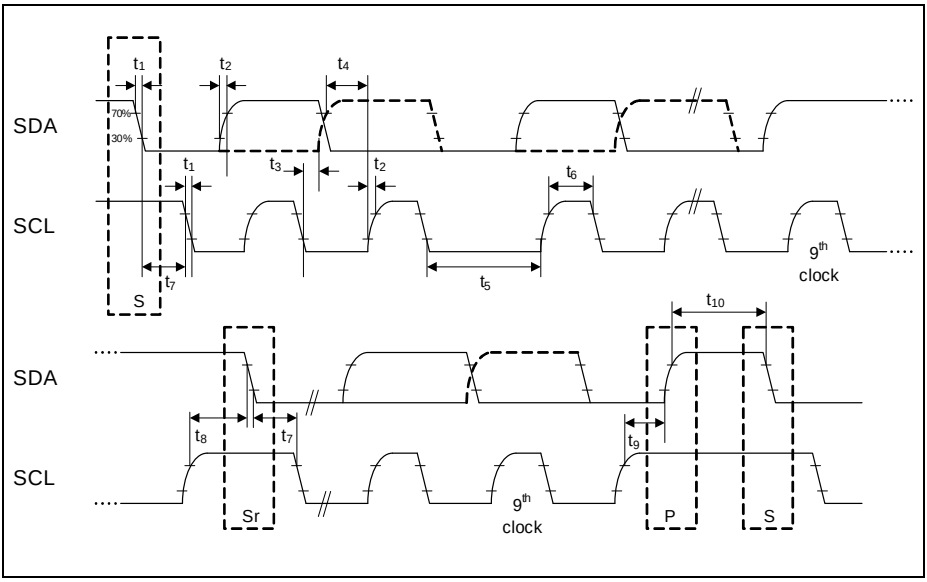

Figure 34 USIC IIC Stand and Fast Mode Timing

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 50 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock high time	t_2 CC	0.35 x t_{1min}	–	–	ns	
Clock low time	t_3 CC	0.35 x t_{1min}	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x t_{1min}	ns	

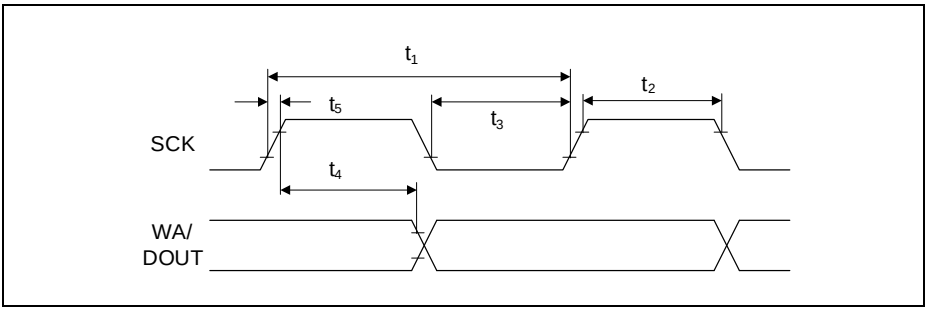

Figure 35 USIC IIS Master Transmitter Timing

Table 51 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x t_{6min}	–	–	ns	
Clock low time	t_8 SR	0.35 x t_{6min}	–	–	ns	
Set-up time	t_9 SR	0.2 x t_{6min}	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

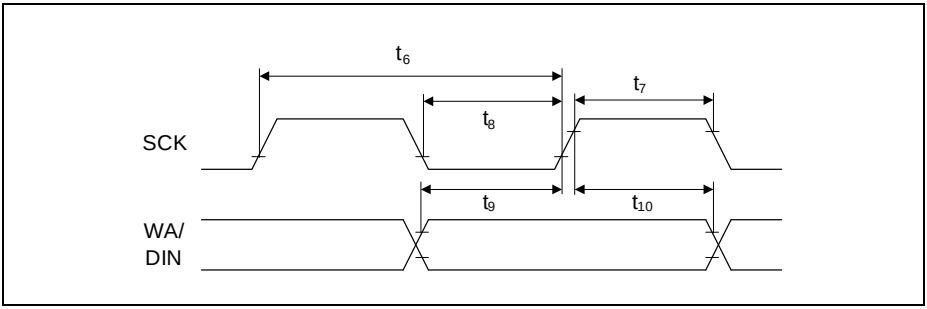

Figure 36 USIC IIS Slave Receiver Timing

Table 53 SD Card Bus Timing for Full-Speed Mode[1)] (cont'd)

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	0	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

Full-Speed Output Path (Write)

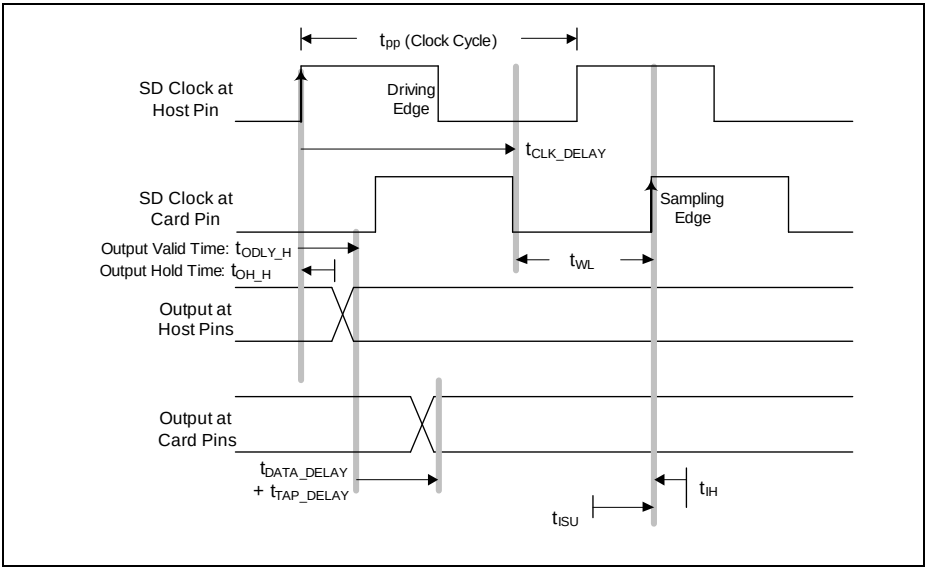

Figure 37 Full-Speed Output Path

Full-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

No clock delay:

(1)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL}$$

Table 62 EBU SDRAM Access Signal Timing Parameters

Parameter			Symbol	Limit Values		Unit
				Min.	Max.	
A(15:0) output valid	from SDCLKO low-to-high transition	CC	t_6	–	9	ns
A(15:0) output hold		CC	t_7	3	–	
$\overline{\text{CS}}$(3:0) low		CC	t_8	–	9	
$\overline{\text{CS}}$(3:0) high		CC	t_9	3	–	
$\overline{\text{RAS}}$ low		CC	t_{10}	–	9	
$\overline{\text{RAS}}$ high		SR	t_{11}	3	–	
$\overline{\text{CAS}}$ low		SR	t_{12}	–	9	
$\overline{\text{CAS}}$ high		CC	t_{13}	3	–	
RD/$\overline{\text{WR}}$ low		CC	t_{14}	–	9	
RD/$\overline{\text{WR}}$ high		CC	t_{15}	3	–	
$\overline{\text{BC}}$(3:0) low		CC	t_{16}	–	9	
$\overline{\text{BC}}$(3:0) high		CC	t_{17}	3	–	
D(15:0) output valid		CC	t_{18}	–	9	
D(15:0) output hold		CC	t_{19}	3	–	
CKE output valid[1)]		CC	t_{22}	–	7	
CKE output hold[1)]		CC	t_{23}	2	–	
D(15:0) input hold		SR	t_{21}	3	–	
D(15:0) input setup to SDCLKO low-to-high transition		SR	t_{20}	4	–	

1) Not depicted in the read and write access timing figures below.

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

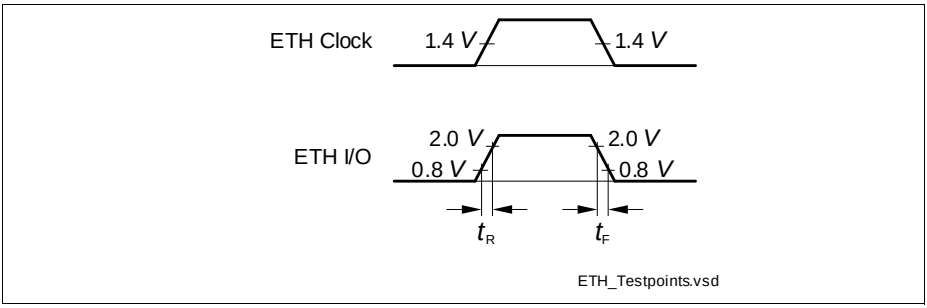

Figure 51 ETH Measurement Reference Points

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 64 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	–	–	ns	C_L = 25 pF
ETH_MDC high time	t_2	CC	160	–	–	ns	
ETH_MDC low time	t_3	CC	160	–	–	ns	
ETH_MDIO setup time (output)	t_4	CC	10	–	–	ns	
ETH_MDIO hold time (output)	t_5	CC	10	–	–	ns	
ETH_MDIO data valid (input)	t_6	SR	0	–	300	ns	

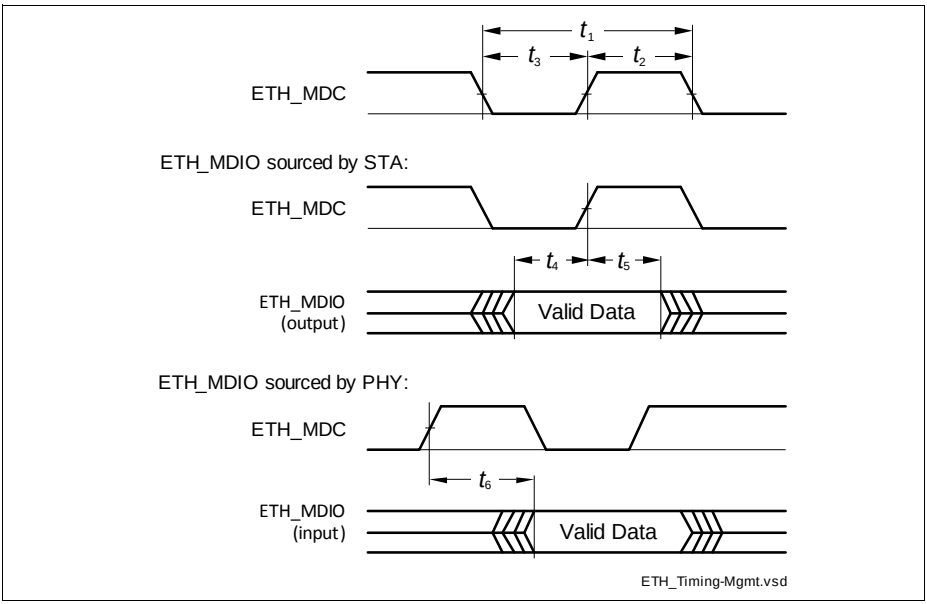

Figure 52 ETH Management Signal Timing

3.3.12.3 ETH MII Parameters

In the following, the parameters of the MII (Media Independent Interface) are described.

Table 65 ETH MII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Clock period, 10 Mbps	t_7	SR	400	–	–	ns	C_L = 25 pF
Clock high time, 10 Mbps	t_8	SR	140	–	260	ns	
Clock low time, 10 Mbps	t_9	SR	140	–	260	ns	
Clock period, 100 Mbps	t_7	SR	40	–	–	ns	
Clock high time, 100 Mbps	t_8	SR	14	–	26	ns	
Clock low time, 100 Mbps	t_9	SR	14	–	26	ns	
Input setup time	t_{10}	SR	10	–	–	ns	
Input hold time	t_{11}	SR	10	–	–	ns	
Output valid time	t_{12}	CC	0	–	25	ns	

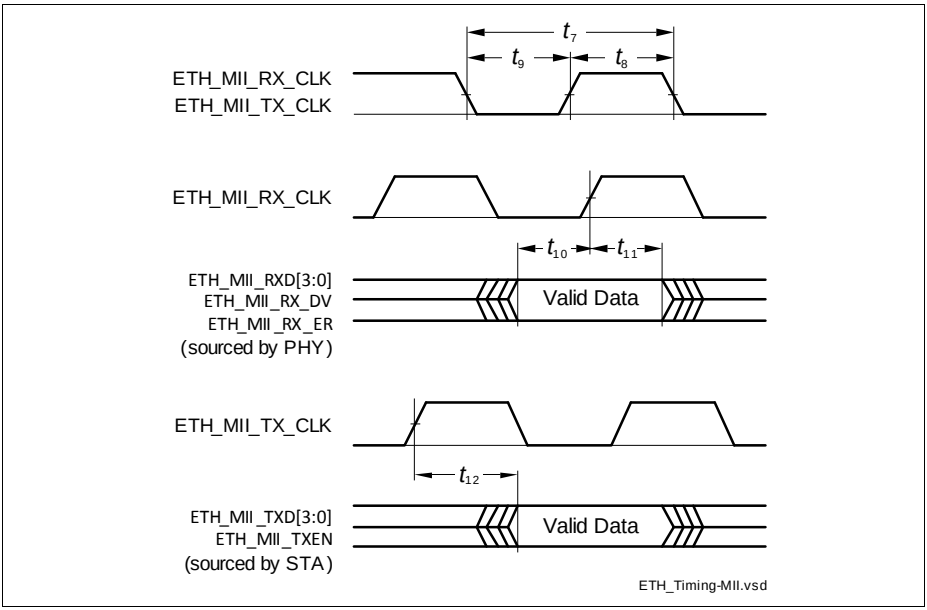

Figure 53 ETH MII Signal Timing

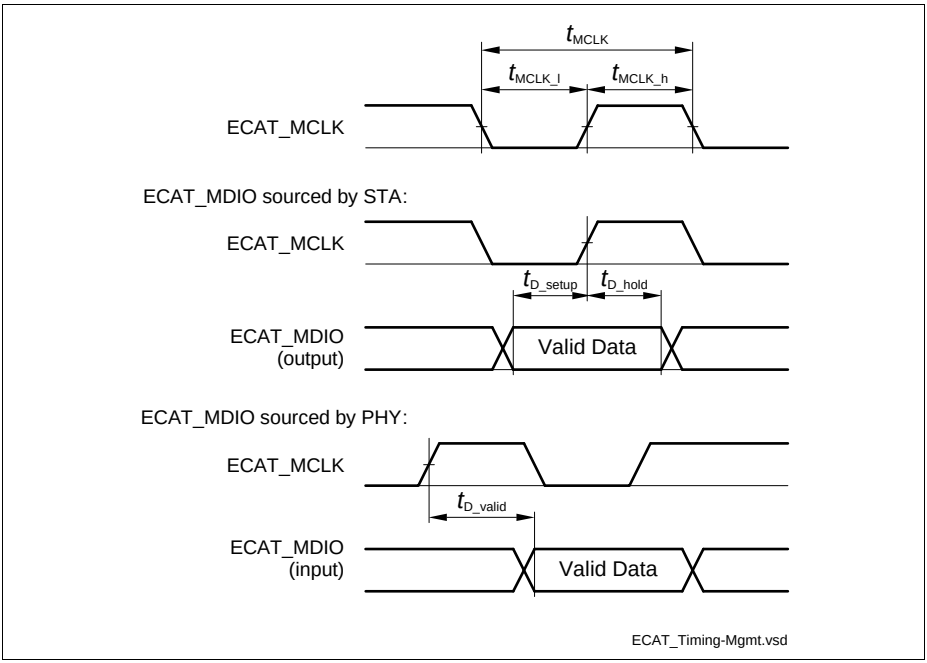

Figure 56 ECAT Management Signal Timing

3.3.13.3 MII Timing TX Characteristics

Table 68 ETH MII TX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PHY_CLK25, TX_CLK period	t_{TX_CLK} SR	–	40	–	ns	
Delay between PHY clock source PHY_CLK25 and TX_CLK output of the PHY	t_{PHY_delay} SR	–	–	–	ns	PHY dependent

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