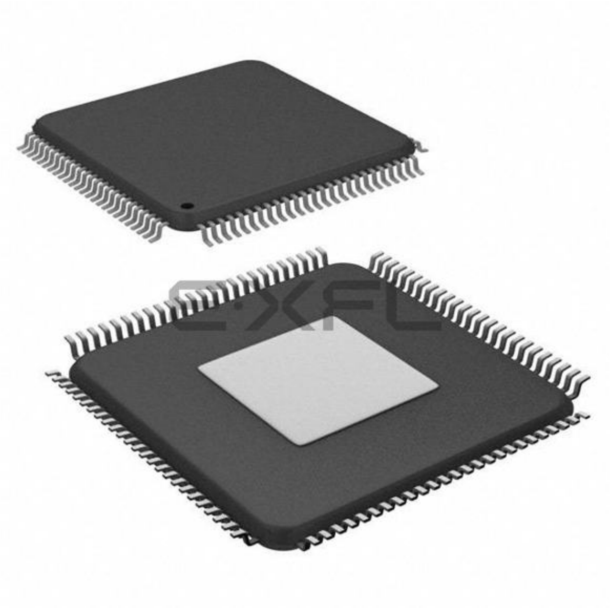

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Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	75
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	352K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-25
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800f100f2048aaxqma1

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Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.11	G5	139	95	A1+	
P0.12	F5	138	94	A1+	
P0.13	E5	137	-	A1+	
P0.14	G6	136	-	A1+	
P0.15	E6	135	-	A1+	
P1.0	F9	112	79	A1+	
P1.1	G9	111	78	A1+	
P1.2	E11	110	77	A2	
P1.3	E12	109	76	A2	
P1.4	E10	108	75	A1+	
P1.5	F10	107	74	A1+	
P1.6	D9	116	83	A2	
P1.7	D10	115	82	A2	
P1.8	C10	114	81	A2	
P1.9	D11	113	80	A2	
P1.10	F12	106	73	A1+	
P1.11	F11	105	72	A1+	
P1.12	G11	104	71	A2	
P1.13	G12	103	70	A2	
P1.14	G10	102	69	A2	
P1.15	J12	94	68	A2	
P2.0	L11	74	52	A2	
P2.1	M12	73	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	M11	72	50	A2	
P2.3	N11	71	49	A2	
P2.4	N10	70	48	A2	
P2.5	P10	69	47	A2	
P2.6	L9	76	54	A1+	
P2.7	M9	75	53	A1+	
P2.8	N9	68	46	A2	
P2.9	P9	67	45	A2	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**HWO0**	**HWO1**	**HWI0**	**HWI1**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P2.12	ETH0.TXD2	ECAT0.P1_TXD1	CCU81.OUT33	ETH0.TXD0	DB.ETM_TRACEDATA1	EBU.AD30		EBU.D30					CCU43.IN3C			
P2.13	ETH0.TXD3	ECAT0.P1_TXD2		ETH0.TXD1	DB.ETM_TRACEDATA0	EBU.AD31		EBU.D31					CCU43.IN2C			
P2.14	VADC.EMUX11	U1C0.DOUT0	CCU80.OUT21	CAN.N4_TXD	DB.ETM_TRACECLK	EBU.$\overline{\text{BC0}}$				U1C0.DX0D			CCU43.IN0B	CCU43.IN1B	CCU43.IN2B	CCU43.IN3B
P2.15	VADC.EMUX12	ECAT0.P1_TXD3	CCU80.OUT11	LEDTS0.LINE6	LEDTS0.EXTENDED6	EBU.$\overline{\text{BC1}}$	LEDTS0.TSIN6A		ETH0.COLA	U1C0.DX0C	CAN.N4_RXDA		CCU42.IN0B	CCU42.IN1B	CCU42.IN2B	CCU42.IN3B
P3.0	U2C1.SELO0	U0C1.SCLKOUT	CCU42.OUT0	ECAT0.P1_TX_ENA		EBU.$\overline{\text{RD}}$			U0C1.DX1B				CCU80.IN2C	CCU81.IN0C		
P3.1		U0C1.SELO0	ECAT0.P1_TXD0			EBU.$\overline{\text{RD\_WR}}$			U0C1.DX2B		ERU0.0B1		CCU80.IN1C			
P3.2	USB.DRIVEVBUS	CAN.N0_TXD	ECAT0.P1_TXD1	LEDTS0.COLA		EBU.$\overline{\text{CS0}}$					ERU0.0A1		CCU80.IN0C			
P3.3		U1C1.SELO1	CCU42.OUT3	ECAT0.MCLK	SDMMC.LED			EBU.$\overline{\text{WAIT}}$		DSD.DIN3B			CCU42.IN3A	CCU80.IN3B		
P3.4	U2C1.MCLKOUT	U1C1.SELO2	CCU42.OUT2	DSD.MCLK3	SDMMC.BUS_POWER			EBU.$\overline{\text{HOLD}}$	U2C1.DX0B	DSD.MCLK3B			CCU42.IN2A	CCU80.IN0B	ECAT0.P1_LINKA	
P3.5	U2C1.DOUT0	U1C1.SELO3	CCU42.OUT1	U0C1.DOUT0	SDMMC.CMD_OUT	EBU.AD4	SDMMC.CMD_IN	EBU.D4	U2C1.DX0A		ERU0.3B1		CCU42.IN1A		ECAT0.P1_RX_ERRA	
P3.6	U2C1.SCLKOUT	U1C1.SELO4	CCU42.OUT0	U0C1.SCLKOUT	SDMMC.CLK_OUT	EBU.AD5	SDMMC.CLK_IN	EBU.D5	U2C1.DX1B		ERU0.3A1		CCU42.IN0A			
P3.7	ECAT0.SYNC0	CAN.N2_TXD	CCU41.OUT3	LEDTS0.LINE0					U2C0.DX0C							
P3.8	U2C0.DOUT0	U0C1.SELO3	CCU41.OUT2	LEDTS0.LINE1					CAN.N2_RXDB				POSIF1.IN2B			
P3.9	U2C0.SCLKOUT	CAN.N1_TXD	CCU41.OUT1	LEDTS0.LINE2									POSIF1.IN1B			
P3.10	U2C0.SELO0	CAN.N0_TXD	CCU41.OUT0	LEDTS0.LINE3	U0C1.DOUT3		U0C1.HWIN3						POSIF1.IN0B			
P3.11	U2C1.DOUT0	U0C1.SELO2	CCU42.OUT3	LEDTS0.LINE4	U0C1.DOUT2		U0C1.HWIN2		CAN.N1_RXDB					CCU81.IN3C		
P3.12	ECAT0.P1_LINK_ACT	U0C1.SELO1	CCU42.OUT2	LEDTS0.LINE5	U0C1.DOUT1		U0C1.HWIN1		CAN.N0_RXDC	U2C1.DX0D				CCU81.IN2C		
P3.13	U2C1.SCLKOUT	U0C1.DOUT0	CCU42.OUT1	LEDTS0.LINE6	U0C1.DOUT0		U0C1.HWIN0		U0C1.DX0D				CCU80.IN3C	CCU81.IN1C		
P3.14		U1C0.SELO3			U1C1.DOUT1		U1C1.HWIN1			U1C1.DX0B			CCU42.IN1C			
P3.15		U1C1.DOUT0			U1C1.DOUT0		U1C1.HWIN0			U1C1.DX0A			CCU42.IN0C			
P4.0	CAN.N3_TXD	ECAT0.PHY_CLK25	DSD.MCLK1	U1C0.SCLKOUT	SDMMC.DATA0_OUT	EBU.AD8	SDMMC.DATA0_IN	EBU.D8	U1C1.DX1C	DSD.MCLK1B	U0C1.DX0E	U2C1.DX0C				ECAT0.P0_RX_ERRA
P4.1	U2C1.SELO0	U1C1.MCLKOUT	DSD.MCLK0	U0C1.SELO0	SDMMC.DATA3_OUT	EBU.AD9	SDMMC.DATA3_IN	EBU.D9	U2C1.DX2B	DSD.MCLK0B		U2C1.DX2A	DSD.MCLK1D			ECAT0.P0_LINKA
P4.2	U2C1.SELO1	U1C1.DOUT0		U2C1.SCLKOUT	ECAT0.MDO		ECAT0.MDIB		U1C1.DX0C			U2C1.DX1A	CCU43.IN1C			

2.3 Power Connection Scheme

Figure 9. shows a reference power connection scheme for the XMC4[78]00.

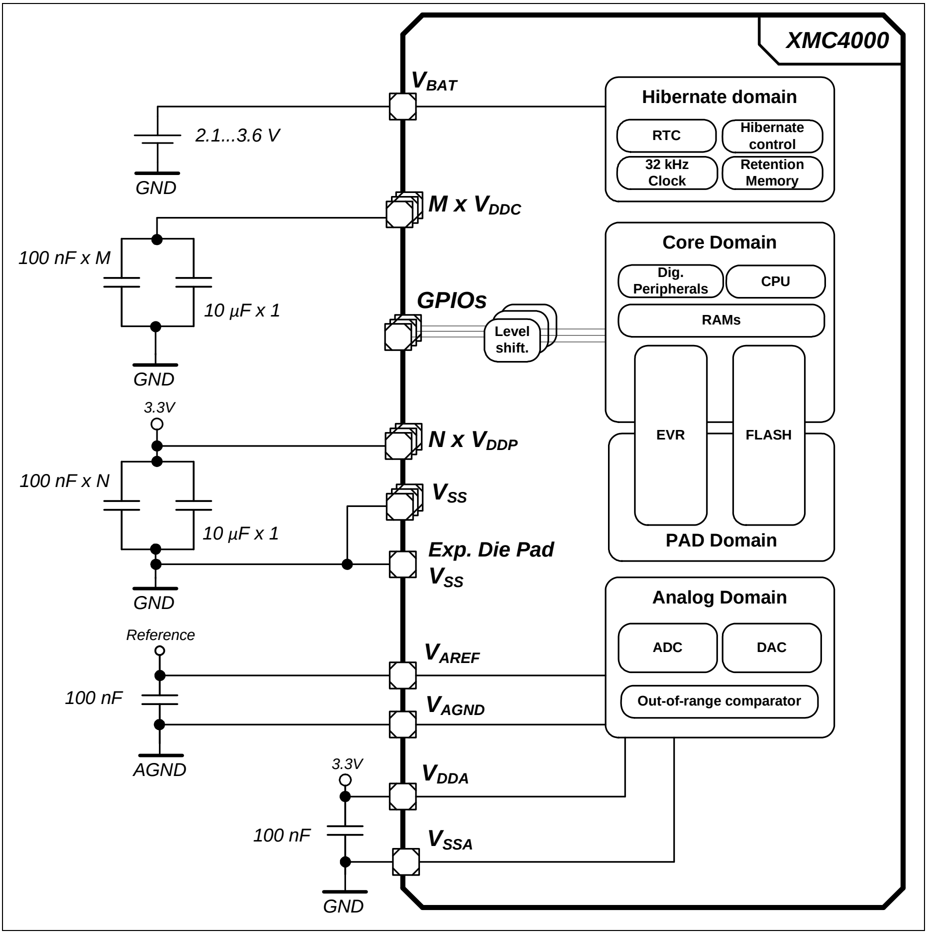

Figure 9 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 10 uF capacitor to the V_{DDC} nets.

The XMC4[78]00 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.
V_{AGND} is the low potential to the analog reference V_{AREF}. Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as "Alternate Reference"; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

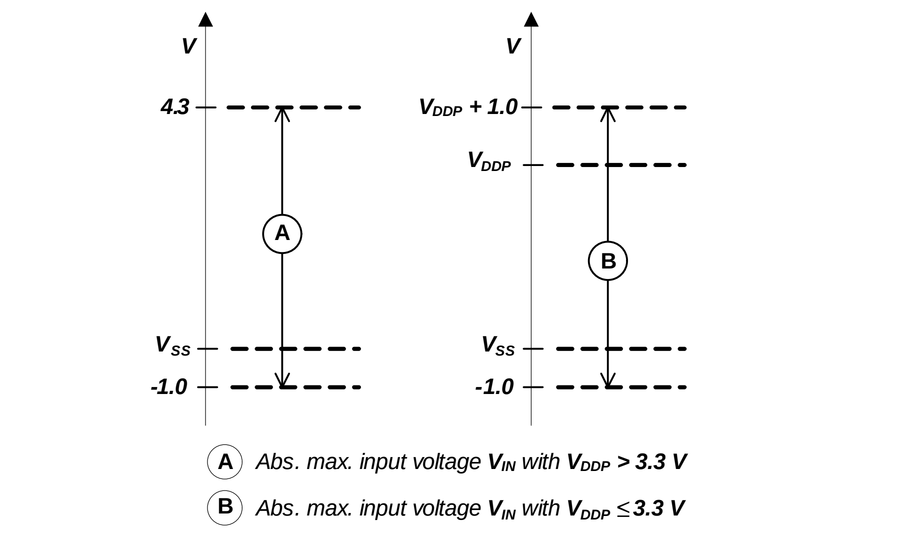

Figure 10 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP} or V_{DDA})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

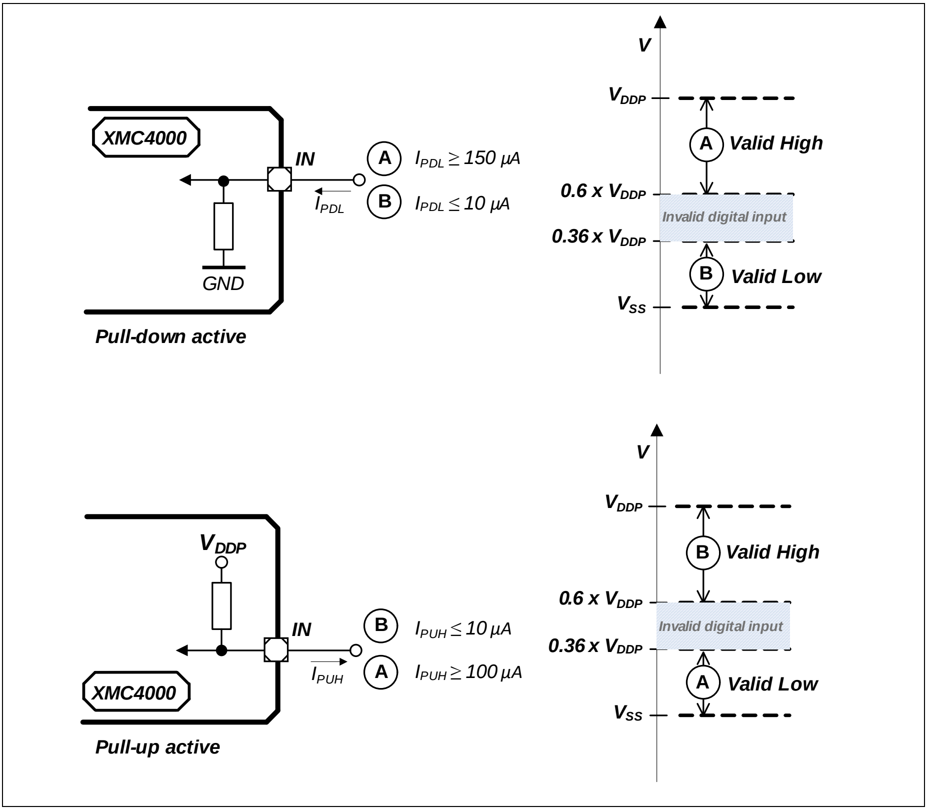

Figure 13 Pull Device Input Characteristics

Figure 13 visualizes the input characteristics with an active internal pull device:

- in the cases “A” the internal pull device is overridden by a strong external driver;
- in the cases “B” the internal pull device defines the input logical state against a weak external load.

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Analog reference voltage[5]	V_{AREF} SR	V_{AGND} + 1	–	V_{DDA} + 0.05[1]	V	
Analog reference ground[5]	V_{AGND} SR	V_{SSM} - 0.05	–	V_{AREF} - 1	V	
Analog reference voltage range[2)5]	V_{AREF} - V_{AGND} SR	1	–	V_{DDA} + 0.1	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{DDA} < V_{AIN} < 0.97 \times V_{DDA}$
		-500	–	100	nA	$0\ V \leq V_{AIN} \leq 0.03 \times V_{DDA}$
		-100	–	500	nA	$0.97 \times V_{DDA} \leq V_{AIN} \leq V_{DDA}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\ V \leq V_{AREF} \leq V_{DDA}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\ V \leq V_{AGND} \leq V_{DDA}$
Internal ADC clock	f_{ADCI} CC	2	–	36	MHz	V_{DDA} = 3.3 V
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[5)6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	$C_{AREFTOT}$ CC	–	20	40	pF	

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 Die Temperature Sensor Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Temperature sensor range	T_{SR}	SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE}	CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE}	CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V[1)]
Measurement time	t_M	CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST}	SR	–	–	10	µs	

1) At V_{DDP_max} = 3.63 V the typical offset error increases by an additional ΔT_{OE} = ±1 °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

$$\text{Temperature } T_{DTS} = (\text{RESULT} - 605) / 2.05 \ [°\text{C}]$$

This formula and the values defined in **Table 29** apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

Table 33 RTC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	–	32.768	–	kHz	
Oscillator start-up time[1)2)3)]	t_{OSCS} CC	–	–	5	s	
Input voltage at RTC_XTAL1	V_{IX} SR	-0.3	–	V_{BAT} + 0.3	V	
Input amplitude (peak-to-peak) at RTC_XTAL1[2)4)]	V_{PPX} SR	0.4	–	–	V	
Input high voltage at RTC_XTAL1[5)]	V_{IHBX} SR	$0.6 \times V_{BAT}$	–	V_{BAT} + 0.3	V	
Input low voltage at RTC_XTAL1[5)]	V_{ILBX} SR	-0.3	–	$0.36 \times V_{BAT}$	V	
Input Hysteresis for RTC_XTAL1[5)6)]	V_{HYSX} CC	$0.1 \times V_{BAT}$		–	V	$3.0\text{ V} \leq V_{BAT} < 3.6\text{ V}$
		$0.03 \times V_{BAT}$		–	V	$V_{BAT} < 3.0\text{ V}$
Input leakage current at RTC_XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0\text{ V} \leq V_{IX} \leq V_{BAT}$

1) t_{OSCS} is defined from the moment the oscillator is enabled by the user with SCU_OSCULCTRL.MODE until the oscillations reach an amplitude at RTC_XTAL1 of 400 mV.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) For a reliable start of the oscillation in crystal mode it is required that $V_{BAT} \geq 3.0$ V. A running oscillation is maintained across the full V_{BAT} voltage range.

4) If the shaper unit is enabled and not bypassed.

5) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

6) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 34 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)11)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	135	–	mA	144 / 144 / 144
			–	125	–		144 / 72 / 72
			–	97	–		72 / 72 / 144
			–	80	–		24 / 24 / 24
			–	68	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA}	CC	–	108	–	mA	144 / 144 / 144
			–	98	–		144 / 72 / 72
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	86	–	mA	144 / 144 / 144
			–	85	–		144 / 72 / 72
			–	70	–		72 / 72 / 144
			–	55	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	127	–	mA	144 / 144 / 144
			–	115	–		144 / 72 / 72
			–	93	–		72 / 72 / 144
			–	57	–		24 / 24 / 24
			–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	48	–		100 / 100 / 100

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

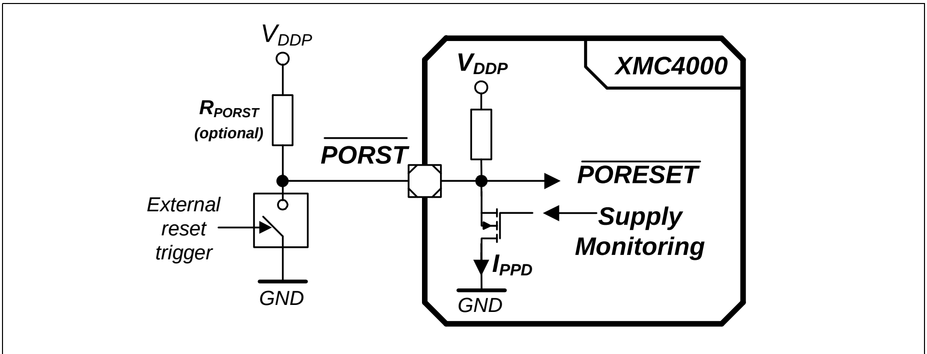

Figure 25 $\overline{\text{PORST}}$ Circuit

Table 37 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	[4]
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

3.3.4 Phase Locked Loop (PLL) Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Main and USB PLL

Table 39 PLL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	–	–	±5	ns	accumulated over 300 cycles f_{SYS} = 144 MHz
Duty Cycle[1)]	D_{DC} CC	46	50	54	%	Low pulse to total period, assuming an ideal input clock source
PLL base frequency	$f_{PLLBASE}$ CC	30	–	140	MHz	
VCO input frequency	f_{REF} CC	4	–	16	MHz	
VCO frequency range	f_{VCO} CC	260	–	520	MHz	
PLL lock-in time	t_L CC	–	–	400	µs	

1) 50% for even K2 divider values, 50±(10/K2) for odd K2 divider values.

3.3.5 Internal Clock Source Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Fast Internal Clock Source

Table 40 Fast Internal Clock Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Nominal frequency	f_{OFINC} CC	–	36.5	–	MHz	not calibrated
		–	24	–	MHz	calibrated
Accuracy	Δf_{OFI} CC	-0.5	–	0.5	%	automatic calibration[1)2)]
		-15	–	15	%	factory calibration, V_{DDP} = 3.3 V
		-25	–	25	%	no calibration, V_{DDP} = 3.3 V
		-7	–	7	%	Variation over voltage range[3)] 3.13 V $\leq V_{DDP} \leq$ 3.63 V
Start-up time	t_{OFIS} CC	–	50	–	µs	

1) Error in addition to the accuracy of the reference clock.

2) Automatic calibration compensates variations of the temperature and in the V_{DDP} supply voltage.

3) Deviations from the nominal V_{DDP} voltage induce an additional error to the uncalibrated and/or factory calibrated oscillator frequency.

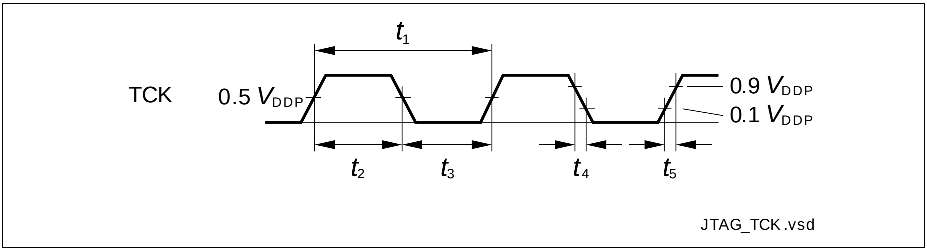

Figure 27 Test Clock Timing (TCK)

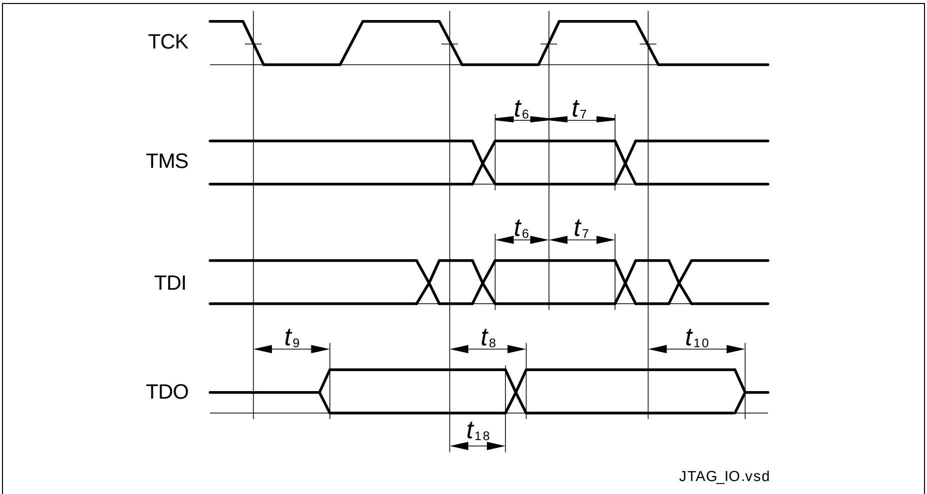

Figure 28 JTAG Timing

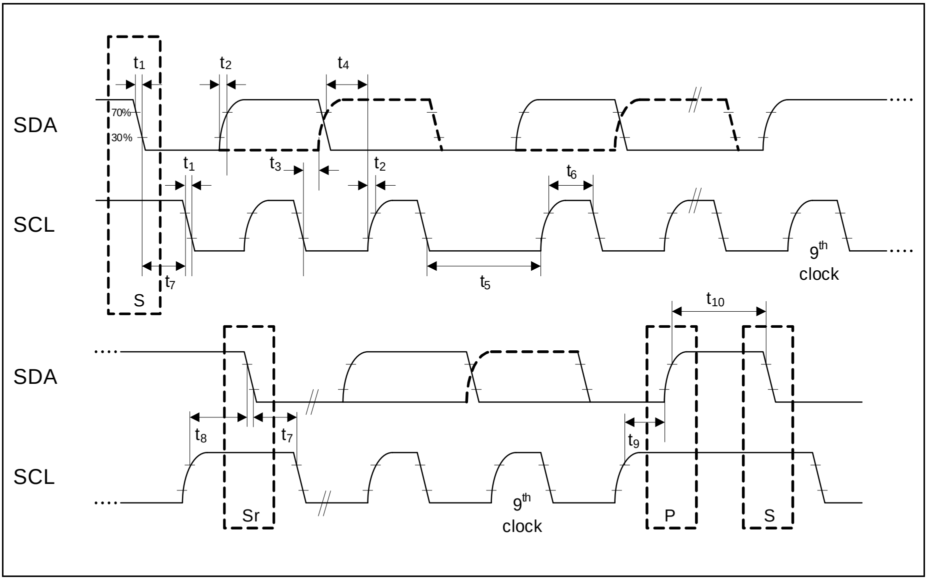

Figure 34 USIC IIC Stand and Fast Mode Timing

3.3.9.4 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 50 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	33.3	–	–	ns	
Clock high time	t_2 CC	0.35 x $t_{1\text{min}}$	–	–	ns	
Clock low time	t_3 CC	0.35 x $t_{1\text{min}}$	–	–	ns	
Hold time	t_4 CC	0	–	–	ns	
Clock rise time	t_5 CC	–	–	0.15 x $t_{1\text{min}}$	ns	

Multiplexed Write Timing

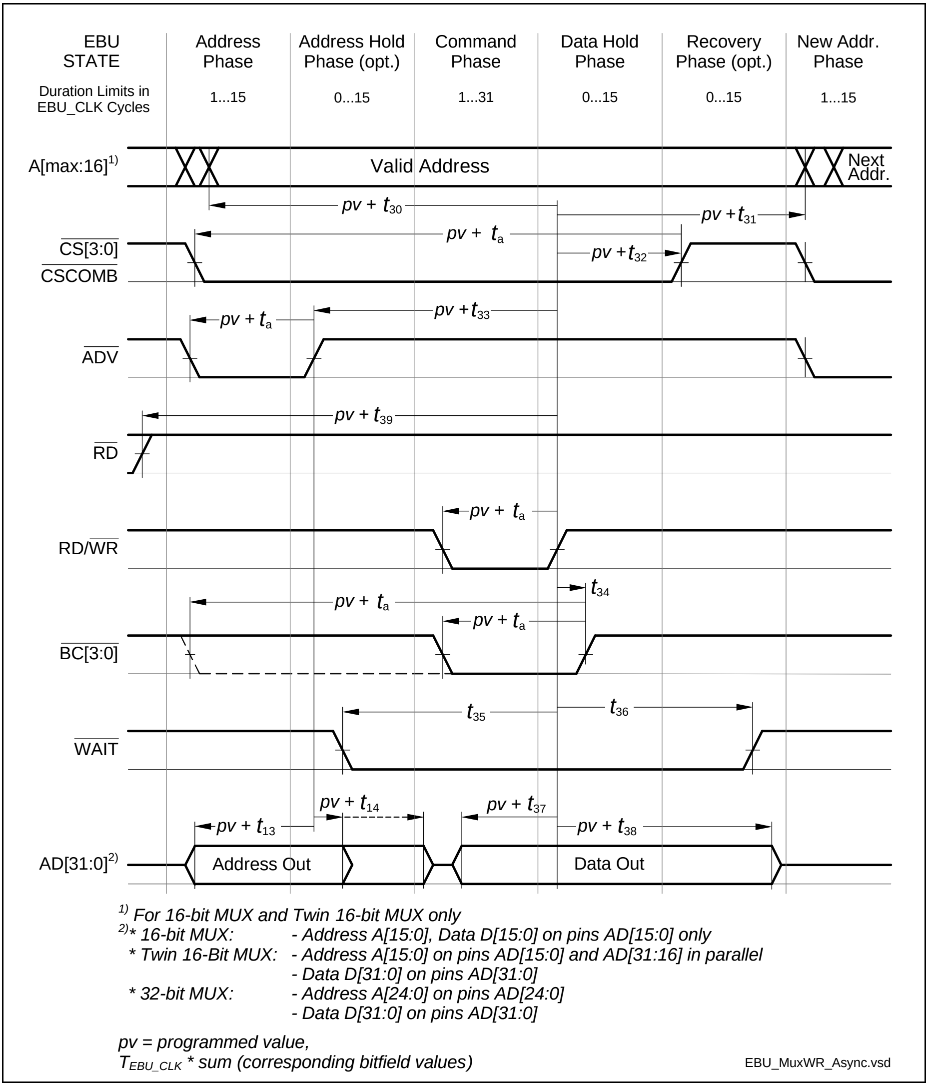

Figure 43 Multiplexed Write Access

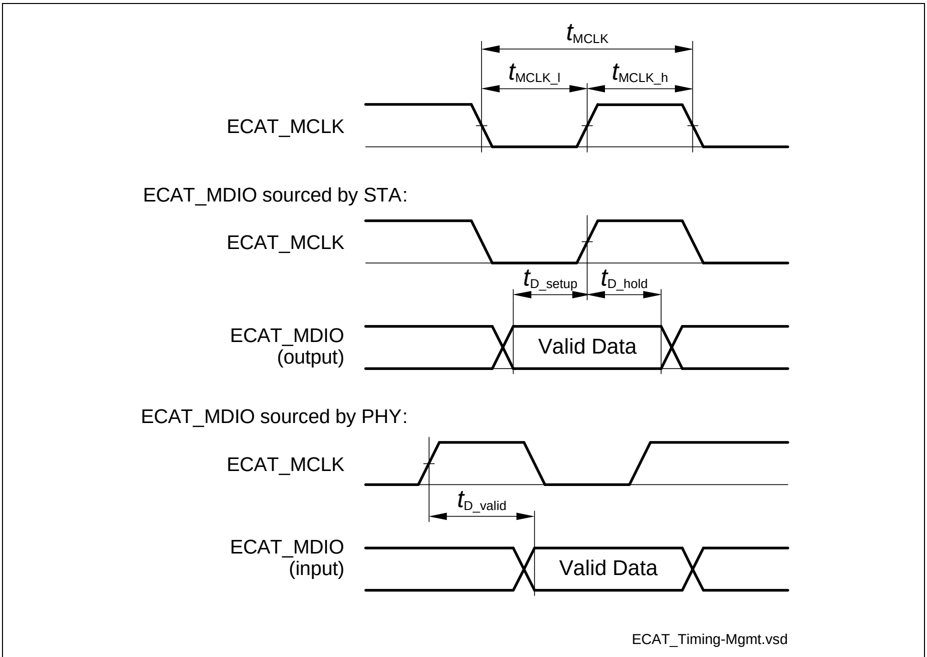

Figure 56 ECAT Management Signal Timing

3.3.13.3 MII Timing TX Characteristics

Table 68 ETH MII TX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PHY_CLK25, TX_CLK period	t_{TX_CLK} SR	–	40	–	ns	
Delay between PHY clock source PHY_CLK25 and TX_CLK output of the PHY	t_{PHY_delay} SR	–	–	–	ns	PHY dependent

The difference between junction temperature and ambient temperature is determined by
$\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

The availability of different packages for different devices types is listed in **Table 1**.

The exposed die pad dimensions are listed in **Table 71**.

5 Quality Declarations

The qualification of the XMC4[78]00 is executed according to the JEDEC standard JESD47I.

Note: For automotive applications refer to the Infineon automotive microcontrollers.

Table 72 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation lifetime	t_{OP} CC	20	–	–	a	$T_J \leq 109°C$, device permanent on
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	–	–	3 000	V	EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	–	–	1 000	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	–	–	3	–	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	–	–	260	°C	Profile according to JEDEC J-STD-020D