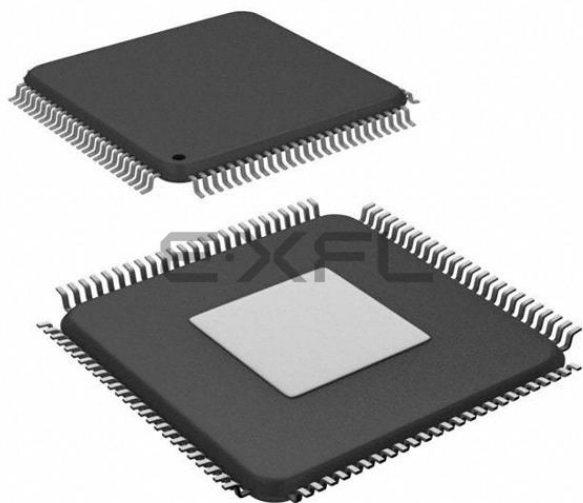




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I ² S, LED, POR, Touch-Sense, WDT
Number of I/O	75
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-25
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800f100k1024aaxqma1

XMC4700 / XMC4800

Microcontroller Series
for Industrial Applications

XMC4000 Family

ARM[®] Cortex[®]-M4
32-bit processor core

Data Sheet
V1.0 2016-01

Microcontrollers

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
 - describes the functionality of the superset of devices.
- **Data Sheets**
 - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
 - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to <http://www.infineon.com/xmc4000> to get access to the latest versions of those documents.

Summary of Features
Table 1 Synopsis of XMC4[78]00 Device Types (cont'd)

Derivative¹⁾	Package	Flash Kbytes	SRAM Kbytes
XMC4700-F144x1536	PG-LQFP-144	1536	276
XMC4700-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x2048	PG-LFBGA-196	2048	352
XMC4800-F144x2048	PG-LQFP-144	2048	352
XMC4800-F100x2048	PG-LQFP-100	2048	352
XMC4800-E196x1536	PG-LFBGA-196	1536	276
XMC4800-F144x1536	PG-LQFP-144	1536	276
XMC4800-F100x1536	PG-LQFP-100	1536	276
XMC4800-E196x1024	PG-LFBGA-196	1024	200
XMC4800-F144x1024	PG-LQFP-144	1024	200
XMC4800-F100x1024	PG-LQFP-100	1024	200

1) x is a placeholder for the supported temperature range.

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC4[78]00 Device Types

Derivative¹⁾	LED TS Intf.	SD MMC Intf.	EBU Intf.²⁾	ETH Intf.³⁾	ECAT Slave Intf.	USB Intf.	USIC Chan.	MultiCAN Nodes, MO
XMC4700-E196x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x2048	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x2048	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-E196x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F144x1536	1	1	SDM	MR	-	1	3 x 2	N[0..5] MO[0..255]
XMC4700-F100x1536	1	1	M16	R	-	1	3 x 2	N[0..5] MO[0..255]

General Device Information
Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P2.10	N8	66	44	A2	
P2.11	P8	65	-	A2	
P2.12	N7	64	-	A2	
P2.13	P7	63	-	A2	
P2.14	M7	60	41	A2	
P2.15	L6	59	40	A2	
P3.0	E1	7	7	A2	
P3.1	D2	6	6	A2	
P3.2	D3	5	5	A2	
P3.3	H7	132	93	A1+	
P3.4	G7	131	92	A1+	
P3.5	D6	130	91	A2	
P3.6	C7	129	90	A2	
P3.7	G4	14	-	A1+	
P3.8	G3	13	-	A1+	
P3.9	H5	12	-	A1+	
P3.10	H6	11	-	A1+	
P3.11	F3	10	-	A1+	
P3.12	F2	9	-	A2	
P3.13	E2	8	-	A2	
P3.14	F6	134	-	A1+	
P3.15	F7	133	-	A1+	
P4.0	D8	124	85	A2	
P4.1	C9	123	84	A2	
P4.2	G8	122	-	A1+	
P4.3	H8	121	-	A1+	
P4.4	E7	120	-	A1+	
P4.5	F8	119	-	A1+	
P4.6	E8	118	-	A1+	
P4.7	E9	117	-	A1+	
P5.0	K9	84	58	A1+	
P5.1	K8	83	57	A1+	
P5.2	K7	82	56	A1+	

General Device Information
Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
PORST	J11	91	65	special	Weak pull-up permanently active, strong pull-down controlled by EVR.
XTAL1	K11	87	61	clock_IN	
XTAL2	K12	88	62	clock_O	
RTC_XTAL1	H1	23	16	clock_IN	
RTC_XTAL2	H2	22	15	clock_O	
VBAT	J1	24	17	Power	When VDDP is supplied VBAT has to be supplied as well.
VBUS	G2	17	10	special	
VAREF	P3	46	33	AN_Ref	
VAGND	P2	45	32	AN_Ref	
VDDA	N1	48	35	AN_Power	
VSSA	P1	47	34	AN_Power	
VDDC	-	19	12	Power	
VDDC	-	61	42	Power	
VDDC	-	90	64	Power	
VDDC	-	125	86	Power	
VDDC	C2	-	-	Power	
VDDC	D12	-	-	Power	
VDDC	P11	-	-	Power	
VDDP	-	18	11	Power	
VDDP	-	62	43	Power	
VDDP	-	86	60	Power	
VDDP	-	126	87	Power	
VDDP	C11	-	-	Power	
VDDP	D1	-	-	Power	
VDDP	N12	-	-	Power	
VSS	-	85	59	Power	
VSS	A1	-	-	Power	
VSS	A14	-	-	Power	
VSS	B13	-	-	Power	
VSS	C1	-	-	Power	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23	CCU81. OUT10	U0C0. DOUT0		U0C0. HWO0		U0C0. DX0A	CAN. N0_RXDA	ERU0. ZA0	ERU1. GA0	CCU41. IN1C	DSD. DIN2B		ECAT0. P0_RXD1A
P1.6	ECAT0. P0_TXD0	U0C0. SCLKOUT			SDMMC. DATA1_OUT	EBU. AD10	SDMMC. DATA1_IN	EBU. D10	DSD. DIN2A							
P1.7	ECAT0. P0_TXD1	U0C0. DOUT0	DSD. MCLK2	U1C1. SEL02	SDMMC. DATA2_OUT	EBU. AD11	SDMMC. DATA2_IN	EBU. D11		DSD. MCLK2A			DSD. MCLK0C			
P1.8	ECAT0. P0_TXD2	U0C0. SEL01	DSD. MCLK1	U1C1. SCLKOUT	SDMMC. DATA4_OUT	EBU. AD12	SDMMC. DATA4_IN	EBU. D12	CAN. N2_RXDA	DSD. MCLK1A			DSD. MCLK0D	DSD. MCLK2D	DSD. MCLK3D	
P1.9	U0C0. SCLKOUT	CAN. N2_TXD	DSD. MCLK0	U1C1. DOUT0	SDMMC. DATA5_OUT	EBU. AD13	SDMMC. DATA5_IN	EBU. D13		DSD. MCLK0A			DSD. MCLK1C	DSD. MCLK2C	DSD. MCLK3C	ECAT0. P0_RX_DVA
P1.10	U0C0. MDC	U0C0. SCLKOUT	CCU81. OUT21	ECAT0. LED_ERR			SDMMC. SDC0						CCU41. IN2C			ECAT0. P0_RXD2A
P1.11	ECAT0. LED_STATE_RU N	U0C0. SEL00	CCU81. OUT11	ECAT0. LED_RUN	ETH0. MDO		ETH0. MDIC						CCU41. IN3C			ECAT0. P0_RXD3A
P1.12	ETH0. TX_EN	CAN. N1_TXD	CCU81. OUT01	ECAT0. P0_LINK_ACT	SDMMC. DATA6_OUT	EBU. AD16	SDMMC. DATA6_IN	EBU. D16								
P1.13	ETH0. TXD0	U0C1. SEL03	CCU81. OUT20	ECAT0. PHY_CLK25	SDMMC. DATA7_OUT	EBU. AD17	SDMMC. DATA7_IN	EBU. D17	CAN. N1_RXDC							
P1.14	ETH0. TXD1	U0C1. SEL02	CCU81. OUT10	ECAT0. SYNC0		EBU. AD18		EBU. D18	U1C0. DX0E							
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81. OUT00	U1C0. DOUT0		EBU. AD19		EBU. D19		DSD. MCLK2B		ERU1. IA0				ECAT0. P0_LINKB
P2.0	CAN. N0_TXD	CCU81. OUT21	DSD. CGPWMN	LEDTS0. COL1	ETH0. MDO	EBU. AD20	ETH0. MDIB	EBU. D20			ERU0. 0B3		CCU40. IN1C			
P2.1	CAN. N5_TXD	CCU81. OUT11	DSD. CGPWMF	LEDTS0. COL0	DB.TD0/ TRACESWO	EBU. AD21		EBU. D21	ETH0. CLK_RMIIA			ERU1. 0B0	CCU40. IN0C			ETH0. CLKRXA
P2.2	VADC. EMUX00	CCU81. OUT01	CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	EBU. AD22	LEDTS0. TSINGA	EBU. D22	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2		CCU41. IN2A			
P2.3	VADC. EMUX01	U0C1. SEL00	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	EBU. AD23	LEDTS0. TSIN1A	EBU. D23	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2	POSIF1. IN2A	CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	EBU. AD24	LEDTS0. TSIN2A	EBU. D24	ETH0. RXRERA	U0C1. DX1A	ERU0. 0B2	POSIF1. IN1A	CCU41. IN1A			
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	EBU. AD25	LEDTS0. TSIN3A	EBU. D25	ETH0. RXDVA	U0C1. DX0B	ERU0. GA2	POSIF1. IN0A	CCU41. IN0A			ETH0. CRS_DVA
P2.6	U0C0. SELO4	ERU1. PDOU73	CCU80. OUT13	LEDTS0. COL3	U0C0. DOUT3		U0C0. HWO3		DSD. DIN1B	CAN. N1_RXDA	ERU0. 1B3	CAN. N5_RXDB	CCU40. IN3C	ECAT0. P0_RX_ERRB		
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2					DSD. DIN0B			ERU1. 1B0	CCU40. IN2C			
P2.8	ETH0. TXD0	ERU1. PDOU71	CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	EBU. AD26	LEDTS0. TSIN4A	EBU. D26	DAC. TRIGGERS				CCU40. IN0B	CCU40. IN2B	CCU40. IN3B	CCU40. IN3B
P2.9	ETH0. TXD1	ERU1. PDOU72	CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	EBU. AD27	LEDTS0. TSIN5A	EBU. D27	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN2B	CCU41. IN3B	CCU41. IN3B
P2.10	VADC. EMUX10	ERU1. PDOU70	ECAT0. PHY_RST	ECAT0. SYNC1	DB. ETM_TRACEDA TA3	EBU. AD28		EBU. D28								
P2.11	ETH0. TXER	ECAT0. P1_TXD0	CCU80. OUT22		DB. ETM_TRACEDA TA2	EBU. AD29		EBU. D29								

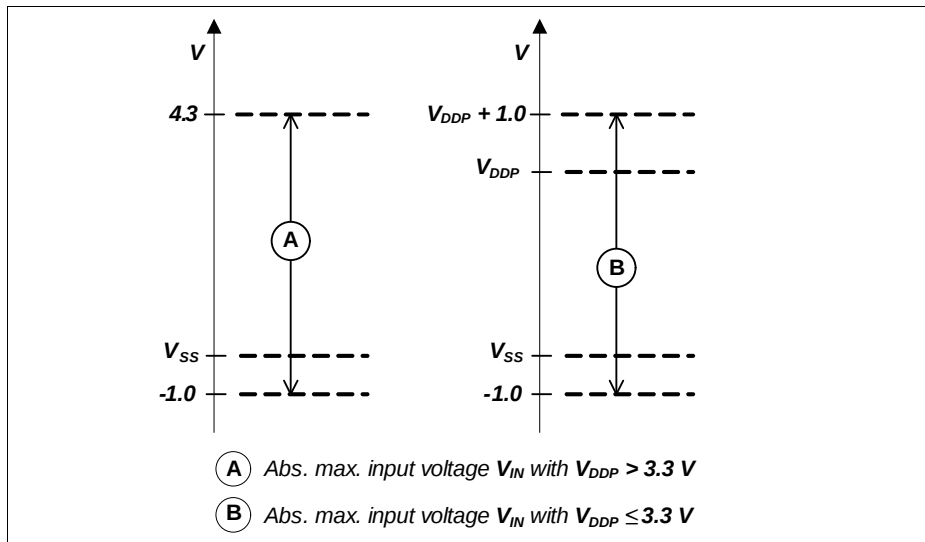


Figure 10 Absolute Maximum Input Voltage Ranges

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 14 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
 - pad supply levels (V_{DDP} or V_{DDA})
 - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.

The Pull-up on the PORST pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	10	pF	
Pull-down current	$ I_{PDL} $ SR	150	–	μA	$^1)V_{IN} \geq 0.6 \times V_{DDP}$
		–	10	μA	$^2)V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$ I_{PUH} $ SR	–	10	μA	$^2)V_{IN} \geq 0.6 \times V_{DDP}$
		100	–	μA	$^1)V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes ³⁾	H_{YSA} CC	$0.1 \times V_{DDP}$	–	V	
PORST spike filter always blocked pulse duration	t_{SF1} CC	–	10	ns	
PORST spike filter pass-through pulse duration	t_{SF2} CC	100	–	ns	
PORST pull-down current	$ I_{PPD} $ CC	13	–	mA	$V_{IN} = 1.0 V$

1) Current required to override the pull device with the opposite logic level ("force current").

With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level ("keep current").

With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 21 Standard Pads Class_A1

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1} CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3	$0.36 \times V_{DDP}$	V	
Output high voltage, POD ¹⁾ = weak	V_{OHA1} CC	$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{OH} \geq -500\text{ }\mu\text{A}$
Output high voltage, POD ¹⁾ = medium		$V_{DDP} - 0.4$	–	V	$I_{OH} \geq -1.4\text{ mA}$
		2.4	–	V	$I_{OH} \geq -2\text{ mA}$
Output low voltage	V_{OLA1} CC	–	0.4	V	$I_{OL} \leq 500\text{ }\mu\text{A}$; POD ¹⁾ = weak
		–	0.4	V	$I_{OL} \leq 2\text{ mA}$; POD ¹⁾ = medium
Fall time	t_{FA1} CC	–	150	ns	$C_L = 20\text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50\text{ pF}$; POD ¹⁾ = medium
Rise time	t_{RA1} CC	–	150	ns	$C_L = 20\text{ pF}$; POD ¹⁾ = weak
		–	50	ns	$C_L = 50\text{ pF}$; POD ¹⁾ = medium

1) POD = Pin Out Driver

Table 22 Standard Pads Class_A1+

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZA1+} CC	-1	1	μA	$0\text{ V} \leq V_{IN} \leq V_{DDP}$
Input high voltage	V_{IHA1+} SR	$0.6 \times V_{DDP}$	$V_{DDP} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1+} SR	-0.3	$0.36 \times V_{DDP}$	V	

Table 32 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		4	–	25	MHz	External Crystal Mode selected
Oscillator start-up time ¹⁾²⁾	t_{OSCS} CC	–	–	10	ms	
Input voltage at XTAL1	V_{IX} SR	-0.5	–	$V_{\text{DDP}} + 0.5$	V	
Input amplitude (peak-to-peak) at XTAL1 ²⁾³⁾	V_{PPX} SR	$0.4 \times V_{\text{DDP}}$	–	$V_{\text{DDP}} + 1.0$	V	
Input high voltage at XTAL1 ⁴⁾	V_{IHBX} SR	1.0	–	$V_{\text{DDP}} + 0.5$	V	
Input low voltage at XTAL1 ⁴⁾	V_{ILBX} SR	-0.5	–	0.4	V	
Input leakage current at XTAL1	I_{ILX1} CC	-100	–	100	nA	Oscillator power down $0 \text{ V} \leq V_{\text{IX}} \leq V_{\text{DDP}}$

1) t_{OSCS} is defined from the moment the oscillator is enabled with SCU_OSCHPCTRL.MODE until the oscillations reach an amplitude at XTAL1 of $0.4 \times V_{\text{DDP}}$.

2) The external oscillator circuitry must be optimized by the customer and checked for negative resistance and amplitude as recommended and specified by crystal suppliers.

3) If the shaper unit is enabled and not bypassed.

4) If the shaper unit is bypassed, dedicated DC-thresholds have to be met.

3.3 AC Parameters

3.3.1 Testing Waveforms

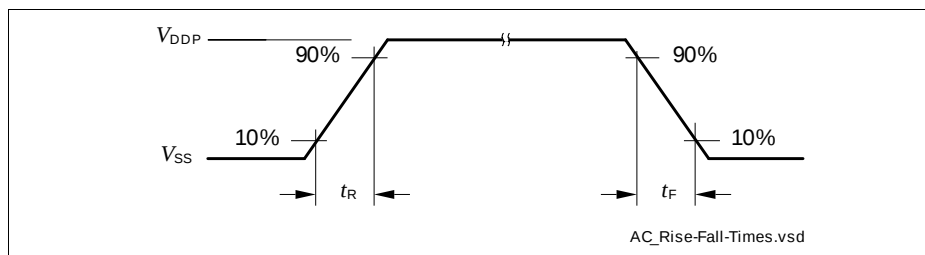


Figure 22 Rise/Fall Time Parameters

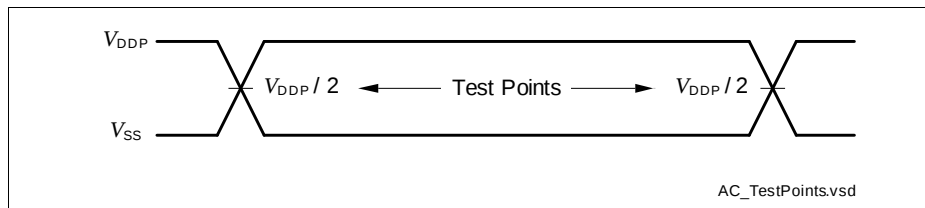


Figure 23 Testing Waveform, Output Delay

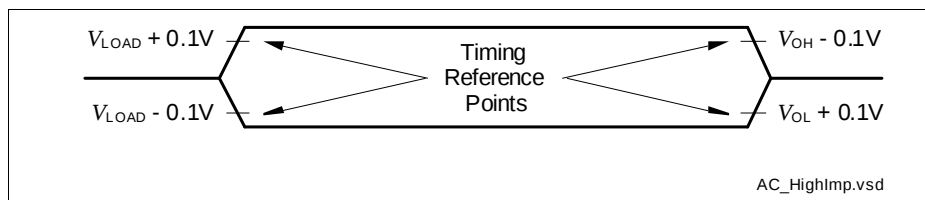


Figure 24 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

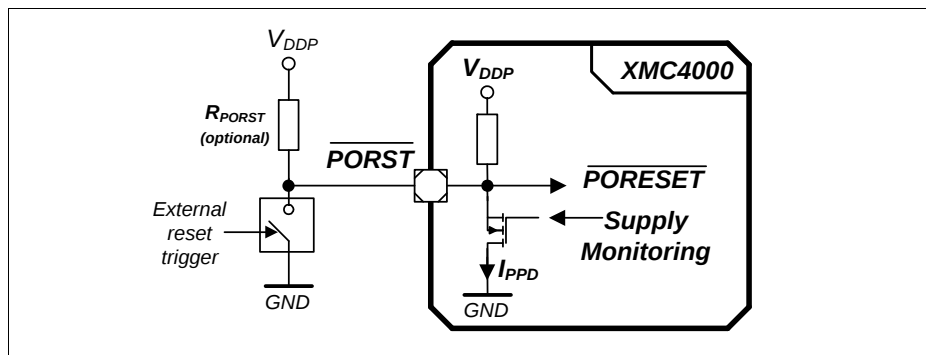


Figure 25 **$\overline{\text{PORST}}$ Circuit**

Table 37 **Supply Monitoring Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79 ¹⁾	–	3.05 ²⁾	V	³⁾
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	μs	⁴⁾
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	μs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

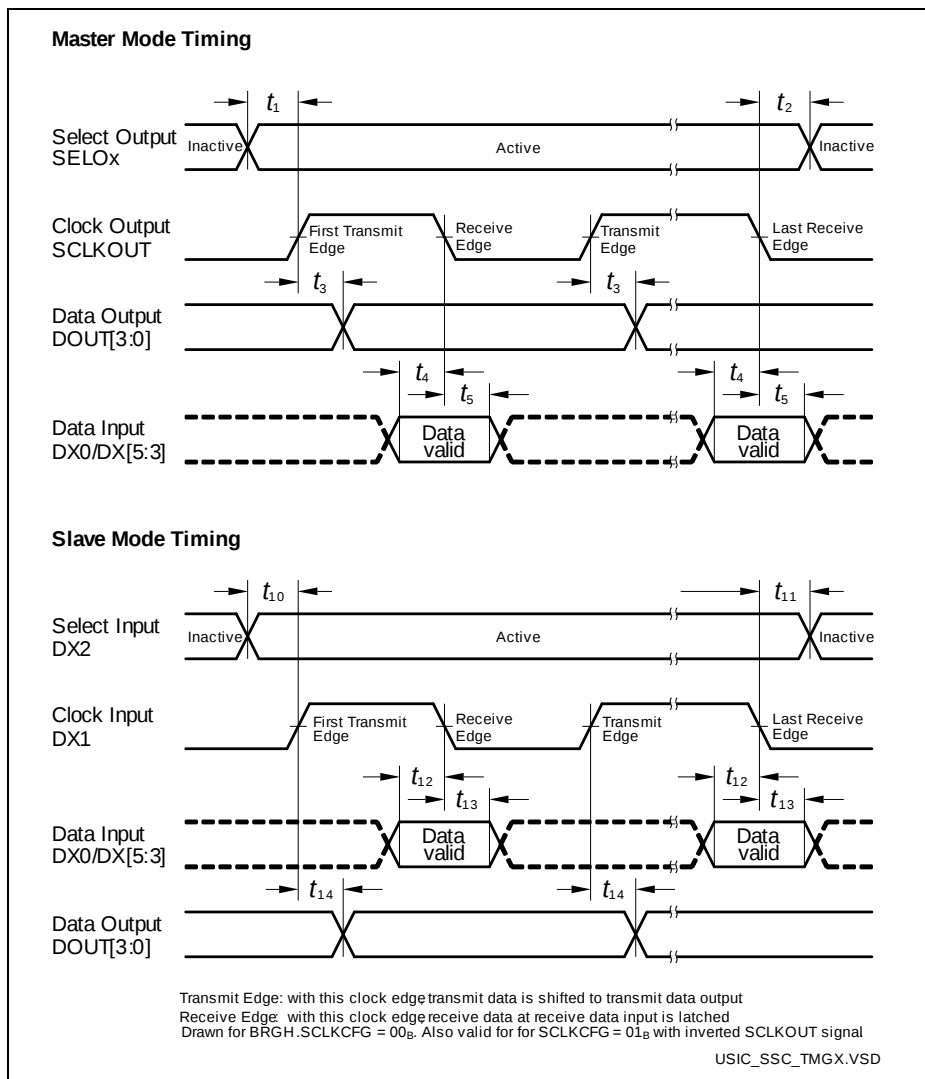


Figure 33 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

Table 49 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + $0.1 \cdot C_b$ ²⁾	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + $0.1 \cdot C_b$ ²⁾	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

High-Speed Read Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(12)

$$t_{CLK_DELAY} + t_{OH} + t_{DATA_DELAY} + t_{TAP_DELAY} > t_{IH_H}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} > t_{IH_H} - t_{OH} - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} > 2 - 2,5 - t_{TAP_DELAY}$$

$$t_{CLK_DELAY} + t_{DATA_DELAY} > -0,5 - t_{TAP_DELAY}$$

The data + clock delay must be greater than -0.5 ns for a 20 ns clock cycle. This is always fulfilled.

3.3.10 EBU Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16$ pF.

3.3.10.1 EBU Asynchronous Timing

Note: For each timing, the accumulated PLL jitter must be added separately.

Table 56 Common Timing Parameters for all Asynchronous Timings

Parameter		Sym bol	Limit Values		Unit	Edge Setting
			Min.	Max.		
Pulse width deviation from the ideal programmed width due to the A2 pad asymmetry, strong driver mode, rise delay - fall delay. $C_L = 16$ pF.	CC	t_a	-1	1.5	ns	sharp
			-2	1		medium
AD(24:16) output delay	to ADV rising	CC t_{13}	-5.5	2		—
AD(24:16) output delay	edge, multiplexed read / write	CC t_{14}	-5.5	2		—

3.3.10.4 EBU SDRAM Access Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply, with Class A2 pins and $C_L = 16$ pF.

Note: With EBU_CLC.SYNC = 1_B frequency must be limited to $f_{CPU} = 120$ MHz.

Table 61 EBU SDRAM Access SDCLKO Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SDCLKO period	t_1	CC	12.5	—	—	ns	—
SDCLKO high time	t_2	SR	5.5	—	—	ns	—
SDCLKO low time	t_3	SR	3.75	—	—	ns	—
SDCLKO rise time	t_4	SR	—	—	3.0	ns	—
SDCLKO fall time	t_5	SR	—	—	3.0	ns	—

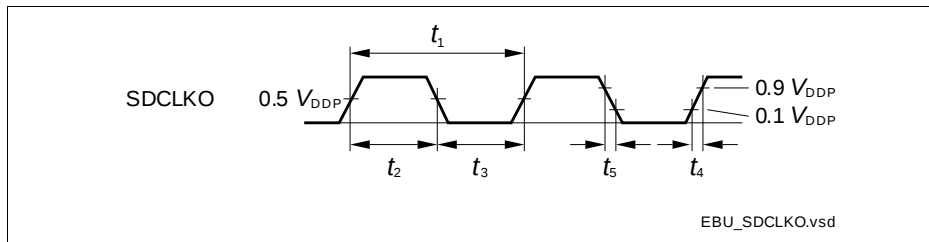


Figure 47 EBU SDRAM Access CLKOUT Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{\text{SYS}} \geq 100 \text{ MHz}$.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

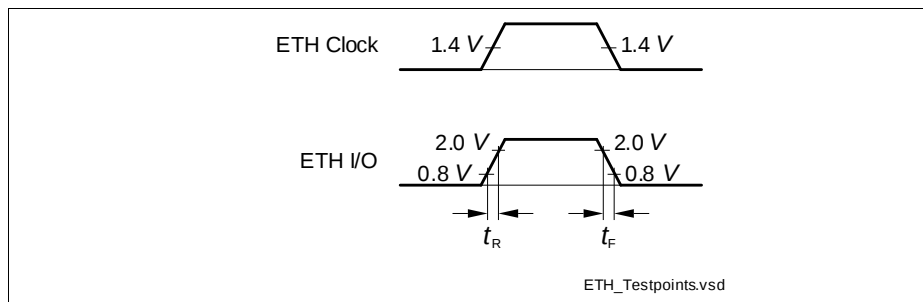


Figure 51 ETH Measurement Reference Points

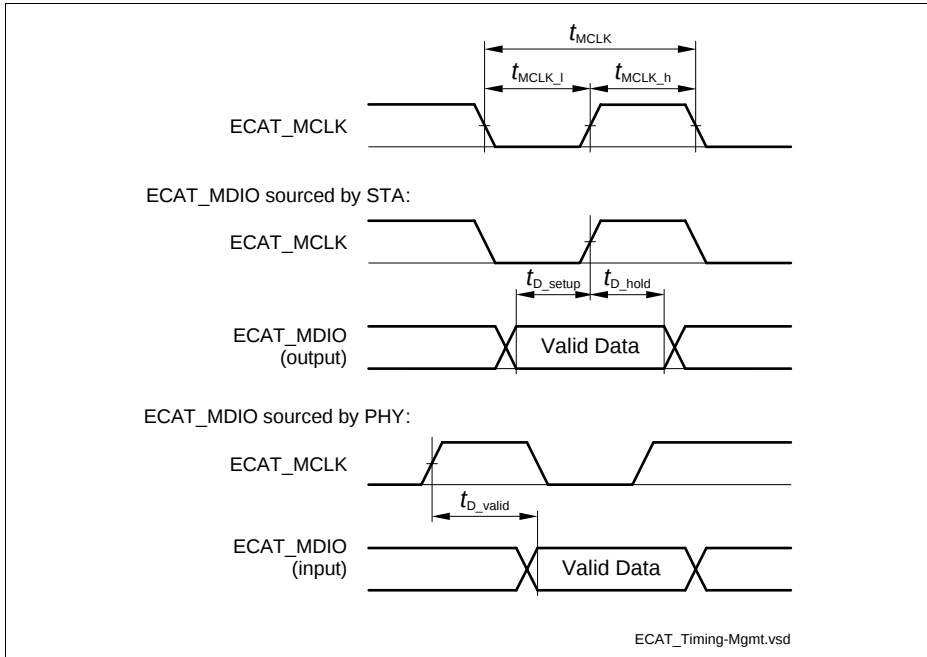


Figure 56 ECAT Management Signal Timing

3.3.13.3 MII Timing TX Characteristics

Table 68 ETH MII TX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PHY_CLK25, TX_CLK period	t_{TX_CLK} SR	—	40	—	ns	
Delay between PHY clock source PHY_CLK25 and TX_CLK output of the PHY	t_{PHY_delay} SR	—	—	—	ns	PHY dependent

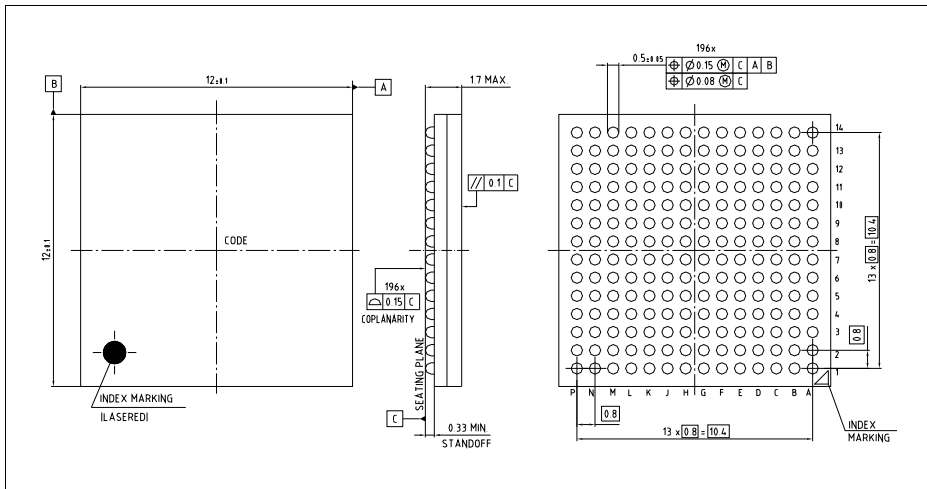


Figure 62 PG-LFBGA-196-2 (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": <http://www.infineon.com/packages>

www.infineon.com