Infineon Technologies - XMC4800F144F1536AAXQMA1 Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	119
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-24
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800f144f1536aaxqma1

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

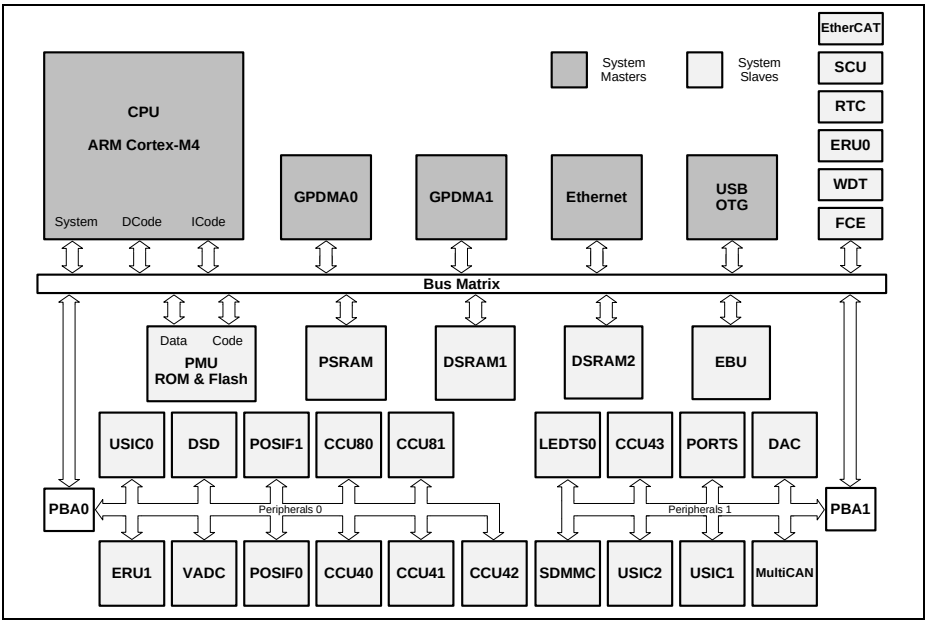

Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High Performance 32-bit ARM Cortex-M4 CPU
  - 16-bit and 32-bit Thumb2 instruction set
  - DSP/MAC instructions
  - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

On-Chip Memories

- 16 KB on-chip boot ROM
- 96 KB on-chip high-speed program memory
- 128 KB on-chip high speed data memory
- 128 KB on-chip high-speed communication memory
- 2,048 KB on-chip Flash Memory with 8 KB instruction cache

Communication Peripherals

- Ethernet MAC module capable of 10/100 Mbit/s transfer rates
- EtherCATSlave interface (ECAT) capable of 100 Mbit/s transfer rates with 2 MII ports, 8 Fieldbus Memory Management Units (FMMU), 8 Sync Manager, 64 bit distributed clocks
- Universal Serial Bus, USB 2.0 host, Full-Speed OTG, with integrated PHY
- Controller Area Network interface (MultiCAN), Full-CAN/Basic-CAN with 6 nodes, 256 message objects (MO), data rate up to 1 MBaud
- Six Universal Serial Interface Channels (USIC),providing 6 serial channels, usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces
- LED and Touch-Sense Controller (LEDTS) for Human-Machine interface
- SD and Multi-Media Card interface (SDMMC) for data storage memory cards
- External Bus Interface Unit (EBU) enabling communication with external memories and off-chip peripherals

Analog Frontend Peripherals

- Four Analog-Digital Converters (VADC) of 12-bit resolution, 8 channels each, with input out-of-range comparators
- Delta Sigma Demodulator with four channels, digital input stage for A/D signal conversion
- Digital-Analog Converter (DAC) with two channels of 12-bit resolution

Industrial Control Peripherals

- Two Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Four Capture/Compare Units 4 (CCU4) for use as general purpose timers
- Two Position Interfaces (POSIF) for servo motor positioning
- Window Watchdog Timer (WDT) for safety sensitive applications
- Die Temperature Sensor (DTS)
- Real Time Clock module with alarm support
- System Control Unit (SCU) for system configuration and control

Input/Output Lines

- Programmable port driver control module (PORTS)
- Individual bit addressability

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P0.11	G5	139	95	A1+	
P0.12	F5	138	94	A1+	
P0.13	E5	137	-	A1+	
P0.14	G6	136	-	A1+	
P0.15	E6	135	-	A1+	
P1.0	F9	112	79	A1+	
P1.1	G9	111	78	A1+	
P1.2	E11	110	77	A2	
P1.3	E12	109	76	A2	
P1.4	E10	108	75	A1+	
P1.5	F10	107	74	A1+	
P1.6	D9	116	83	A2	
P1.7	D10	115	82	A2	
P1.8	C10	114	81	A2	
P1.9	D11	113	80	A2	
P1.10	F12	106	73	A1+	
P1.11	F11	105	72	A1+	
P1.12	G11	104	71	A2	
P1.13	G12	103	70	A2	
P1.14	G10	102	69	A2	
P1.15	J12	94	68	A2	
P2.0	L11	74	52	A2	
P2.1	M12	73	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	M11	72	50	A2	
P2.3	N11	71	49	A2	
P2.4	N10	70	48	A2	
P2.5	P10	69	47	A2	
P2.6	L9	76	54	A1+	
P2.7	M9	75	53	A1+	
P2.8	N9	68	46	A2	
P2.9	P9	67	45	A2	

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P2.10	N8	66	44	A2	
P2.11	P8	65	-	A2	
P2.12	N7	64	-	A2	
P2.13	P7	63	-	A2	
P2.14	M7	60	41	A2	
P2.15	L6	59	40	A2	
P3.0	E1	7	7	A2	
P3.1	D2	6	6	A2	
P3.2	D3	5	5	A2	
P3.3	H7	132	93	A1+	
P3.4	G7	131	92	A1+	
P3.5	D6	130	91	A2	
P3.6	C7	129	90	A2	
P3.7	G4	14	-	A1+	
P3.8	G3	13	-	A1+	
P3.9	H5	12	-	A1+	
P3.10	H6	11	-	A1+	
P3.11	F3	10	-	A1+	
P3.12	F2	9	-	A2	
P3.13	E2	8	-	A2	
P3.14	F6	134	-	A1+	
P3.15	F7	133	-	A1+	
P4.0	D8	124	85	A2	
P4.1	C9	123	84	A2	
P4.2	G8	122	-	A1+	
P4.3	H8	121	-	A1+	
P4.4	E7	120	-	A1+	
P4.5	F8	119	-	A1+	
P4.6	E8	118	-	A1+	
P4.7	E9	117	-	A1+	
P5.0	K9	84	58	A1+	
P5.1	K8	83	57	A1+	
P5.2	K7	82	56	A1+	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P4.3	U2C1. SELO2	U0C0. SELO5	CCU43. OUT3	ECAT0. MCLK									CCU43. IN3A			
P4.4		U0C0. SELO4	CCU43. OUT2		U2C1. DOUT3		U2C1. HWIN3						CCU43. IN2A			
P4.5		U0C0. SELO3	CCU43. OUT1		U2C1. DOUT2		U2C1. HWIN2						CCU43. IN1A			
P4.6		U0C0. SELO2	CCU43. OUT0		U2C1. DOUT1		U2C1. HWIN1		CAN. N2_RXDC			U2C1. DX0E	CCU43. IN0A			
P4.7	U2C1. DOUT0	CAN. N2_TXD			U2C1. DOUT0		U2C1. HWIN0		U0C0. DX0C				CCU43. IN0C			
P5.0	U2C0. DOUT0	DSD. CGPWMN	CCU81. OUT33	ERU1. PDOUT0	U2C0. DOUT0		U2C0. HWIN0		U2C0. DX0B	ETH0. RXD0D	U0C0. DX0D	ECAT0. P0_RXD0B	CCU81. IN0A	CCU81. IN1A	CCU81. IN2A	CCU81. IN3A
P5.1	U0C0. DOUT0	DSD. CGPWMP	CCU81. OUT32	ERU1. PDOUT1	U2C0. DOUT1		U2C0. HWIN1		U2C0. DX0A	ETH0. RXD1D		ECAT0. P0_RXD1B	CCU81. IN0B			
P5.2	U2C0. SCLKOUT	ECAT0. P0_LINK_ACT	CCU81. OUT23	ERU1. PDOUT2					U2C0. DX1A	ETH0. CRS_DVD		ECAT0. P0_RXD2B	CCU81. IN1B			ETH0. RXDVD
P5.3	U2C0. SELO0		CCU81. OUT22	ERU1. PDOUT3	EBU. CKE	EBU. A20			U2C0. DX2A	ETH0. RXERD			CCU81. IN2B			
P5.4	U2C0. SELO1		CCU81. OUT13		$\overline{\text{EBU.}}$ RAS	EBU. A21				ETH0. CRSD			CCU81. IN3B			ECAT0. P0_RX_CLKB
P5.5	U2C0. SELO2		CCU81. OUT12		$\overline{\text{EBU.}}$ CAS	EBU. A22				ETH0. COLD						ECAT0. P0_TX_CLKB
P5.6	U2C0. SELO3		CCU81. OUT03		EBU. BFCLKO	EBU. A23			EBU. BFCLKI							ECAT0. P0_RX_DVB
P5.7	ECAT0. SYNC0		CCU81. OUT02	LEDTS0. COLA	U2C0. DOUT2		U2C0. HWIN2					ECAT0. P0_RXD3B				
P5.8	ECAT0. P1_TX_ENA	U1C0. SCLKOUT	CCU80. OUT01	CAN. N4_TXD	EBU. SDCLKO	$\overline{\text{EBU.}}$ CS2			ETH0. RXD2A	U1C0. DX1B						
P5.9		U1C0. SELO0	CCU80. OUT20	ETH0. TX_EN	EBU. BFCLKO	$\overline{\text{EBU.}}$ CS3			ETH0. RXD3A	U1C0. DX2B					ECAT0. P1_TX_CLKB	
P5.10		U1C0. MCLKOUT	CCU80. OUT10	LEDTS0. LINE7	LEDTS0. EXTENDED7		LEDTS0. TSIN7A		ETH0. CLK_TXA		CAN. N5_RXDA					
P5.11		U1C0. SELO1	CCU80. OUT00	CAN. N5_TXD					ETH0. CRSA							
P6.0	ETH0. TXD2	U0C1. SELO1	CCU81. OUT31	ECAT0. PHY_CLK25	DB. ETM_TRACECLK	EBU. A16										
P6.1	ETH0. TXD3	U0C1. SELO0	CCU81. OUT30	ECAT0. P0_TX_ENA	DB. ETM_TRACEDATA3	EBU. A17			U0C1. DX2C							
P6.2	ETH0. TXER	U0C1. SCLKOUT	CCU43. OUT3	ECAT0. P0_TXD0	DB. ETM_TRACEDATA2	EBU. A18			U0C1. DX1C							
P6.3			CCU43. OUT2	ECAT0. P0_LINK_ACT					U0C1. DX0C	ETH0. RXD3B						
P6.4		U0C1. DOUT0	CCU43. OUT1	ECAT0. P0_TXD1	EBU. SDCLKO	EBU. A19			EBU. SDCLKI	ETH0. RXD2B						
P6.5	CAN. N3_TXD	U0C1. MCLKOUT	CCU43. OUT0	ECAT0. P0_TXD2	DB. ETM_TRACEDATA1	$\overline{\text{EBU.}}$ BC2			DSD. DIN3A	ETH0. CLK_RMIID		U2C0. DX0D				ETH0. CLKRXD

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs											
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
XTAL1									U0C0. DX0F	U0C1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F				
XTAL2																		
RTC_XTAL1											ERU0. 1B1							
RTC_XTAL2																		

2.3 Power Connection Scheme

Figure 9. shows a reference power connection scheme for the XMC4[78]00.

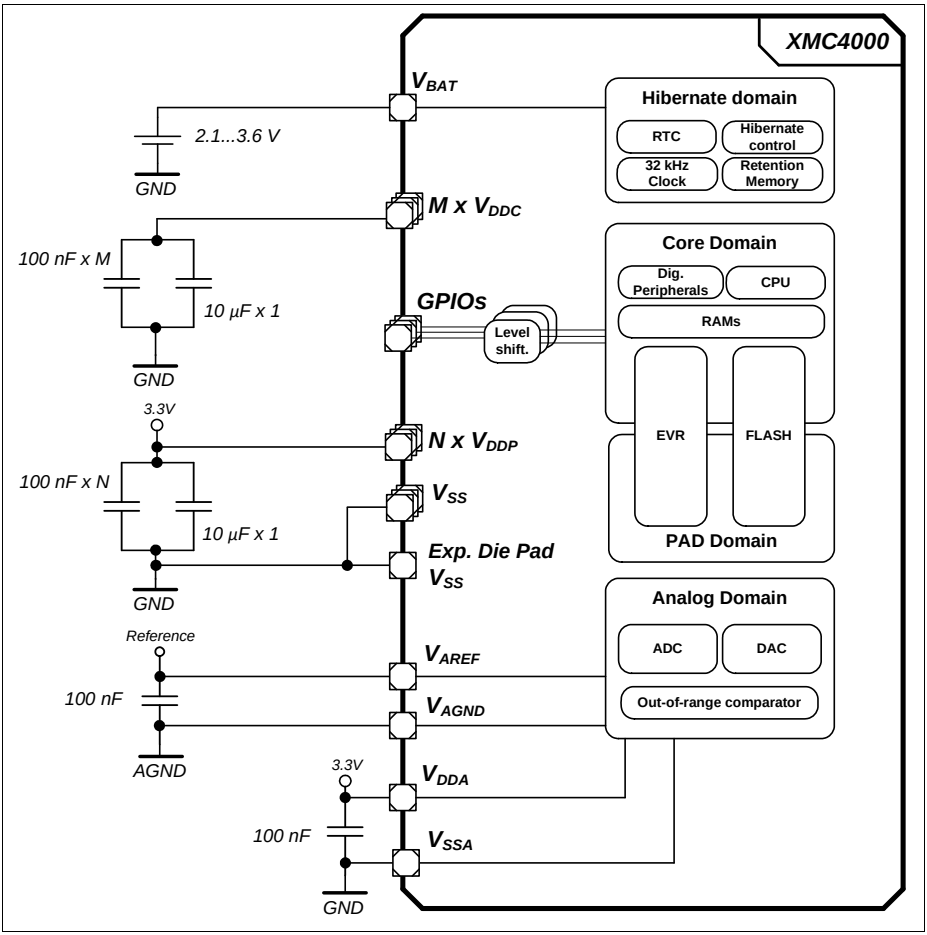

Figure 9 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 10 uF capacitor to the V_{DDC} nets.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–		10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ SR	150		–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–		10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ SR	–		10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100		–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ CC	$0.1 \times V_{DDP}$		–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–		10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100		–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13		–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

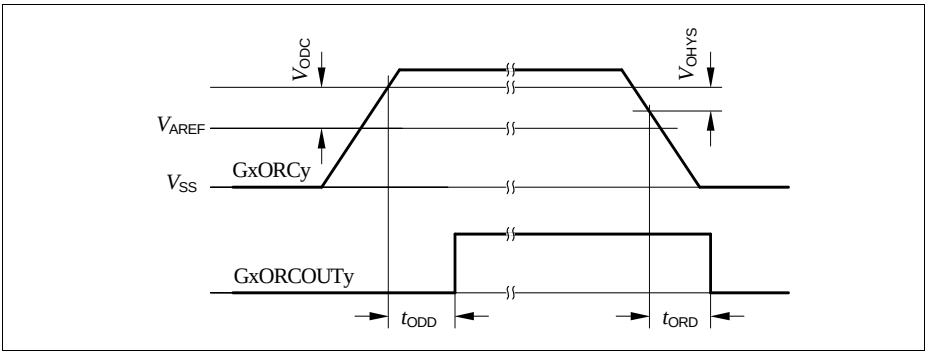

Figure 18 GxORCOUTy Trigger Generation

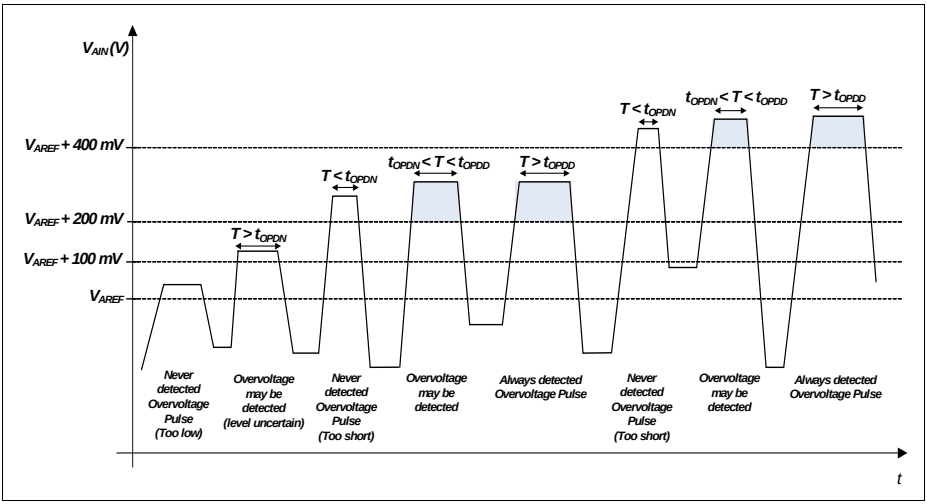

Figure 19 ORC Detection Ranges

3.3 AC Parameters

3.3.1 Testing Waveforms

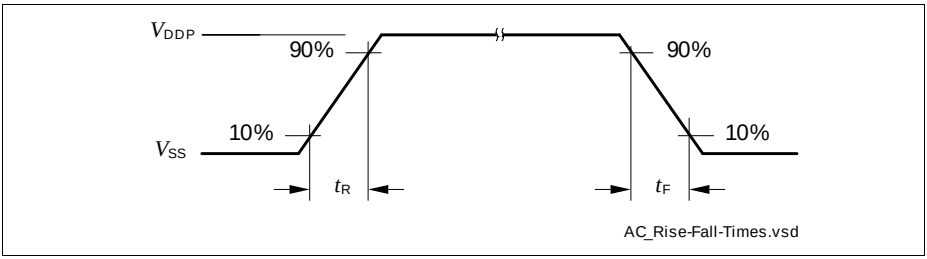

Figure 22 Rise/Fall Time Parameters

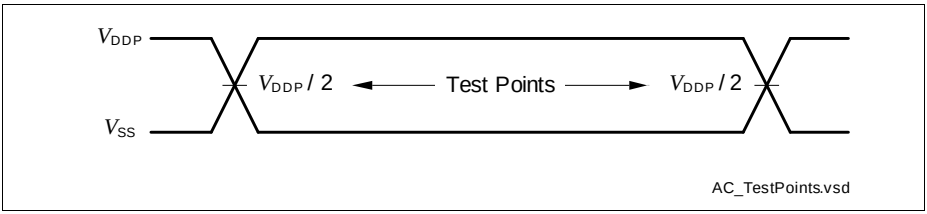

Figure 23 Testing Waveform, Output Delay

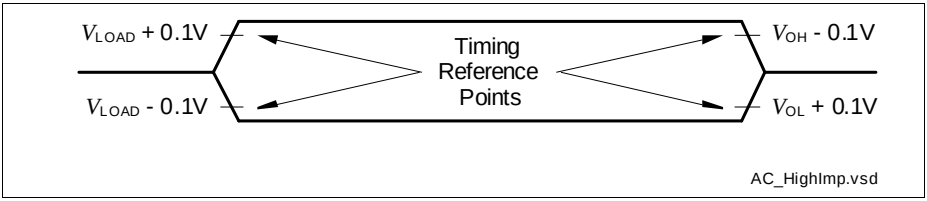

Figure 24 Testing Waveform, Output High Impedance

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

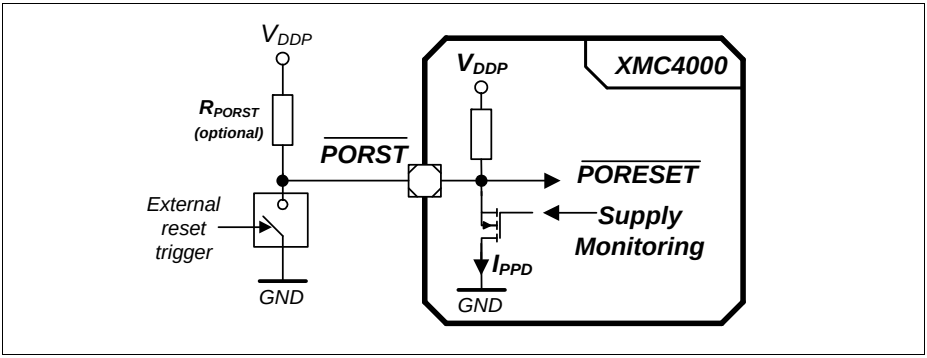

Figure 25 $\overline{\text{PORST}}$ Circuit

Table 37 Supply Monitoring Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79[1]	–	3.05[2]	V	[3]
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	µs	[4]
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	µs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

3.3.7 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply.

Table 43 SWD Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SWDCLK clock period	t_{SC}	SR	25	–	–	ns	C_L = 30 pF
			40	–	–	ns	C_L = 50 pF
SWDCLK high time	t_1	SR	10	–	500000	ns	
SWDCLK low time	t_2	SR	10	–	500000	ns	
SWDIO input setup to SWDCLK rising edge	t_3	SR	6	–	–	ns	
SWDIO input hold after SWDCLK rising edge	t_4	SR	6	–	–	ns	
SWDIO output valid time after SWDCLK rising edge	t_5	CC	–	–	17	ns	C_L = 50 pF
			–	–	13	ns	C_L = 30 pF
SWDIO output hold time from SWDCLK rising edge	t_6	CC	3	–	–	ns	

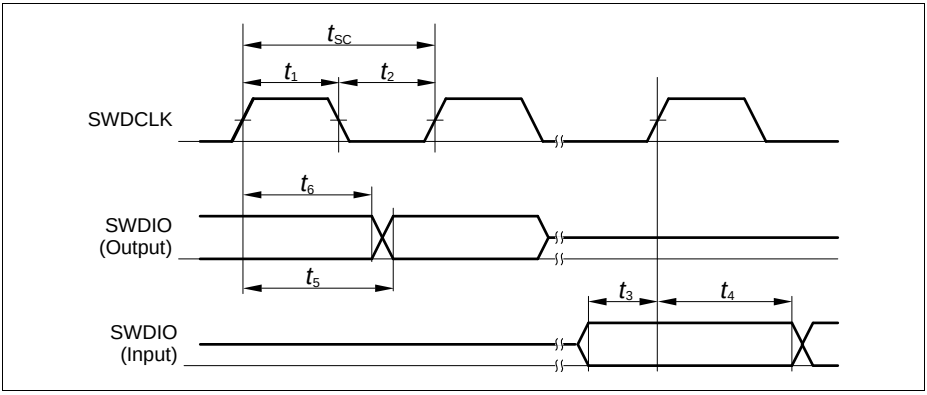

Figure 29 SWD Timing

3.3.8 Embedded Trace Macro Cell (ETM) Timing

The data timing refers to the active clock edge. The XMC4[78]00 ETM uses the half-rate clocking mode. In this mode both, the rising and falling clock edges are active clock edges.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating conditions apply, with $C_L \leq 15$ pF.

Table 44 ETM Interface Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TRACECLK period	t_1	CC	13.8	–	–	ns	–
TRACECLK high time	t_2	CC	2	–	–	ns	–
TRACECLK low time	t_3	CC	2	–	–	ns	–
TRACECLK and TRACEDATA rise time	t_4	CC	–	–	3	ns	–
TRACECLK and TRACEDATA fall time	t_5	CC	–	–	3	ns	–
TRACEDATA output valid time	t_6	CC	-2	–	3	ns	–

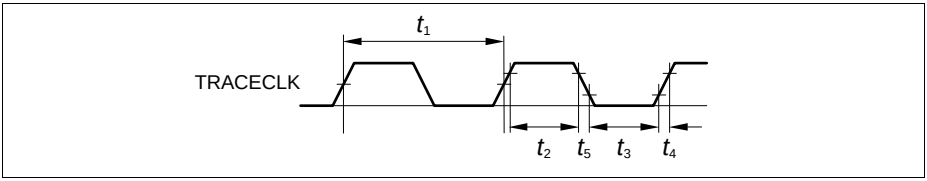

Figure 30 ETM Clock Timing

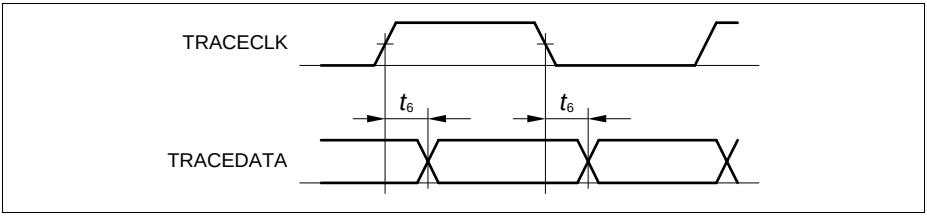

Figure 31 ETM Data Timing

With clock delay:

(2)

$$t_{ODLY\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY}$$

(3)

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{WL} < t_{PP} + t_{CLK\_DELAY} - t_{ISU} - t_{ODLY\_F}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} + 20 < 40 + t_{CLK\_DELAY} - 5 - 10$$

$$t_{DATA\_DELAY} < 5 + t_{CLK\_DELAY} - t_{TAP\_DELAY}$$

The data can be delayed versus clock up to 5 ns in ideal case of t_{WL}= 20 ns.

Full-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

(4)

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_F} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} < 20 + t_{DATA\_DELAY} + t_{TAP\_DELAY} - 5$$

$$t_{DATA\_DELAY} < 15 + t_{CLK\_DELAY} + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 18.2 ns (external delay line) in ideal case of t_{WL}= 20 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

Full-Speed Input Path (Read)

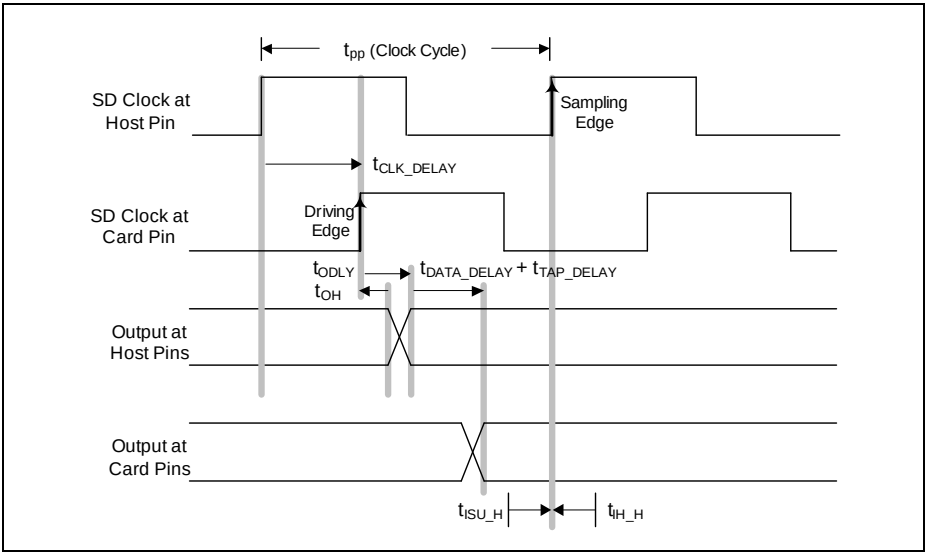

Figure 38 Full-Speed Input Path

Full-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(5)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_F} < 0{,}5 \times t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 0{,}5 \times t_{pp} - t_{ODLY} - t_{ISU\_F} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 40 ns clock cycle.

Table 55 SD Card Bus Timing for High-Speed Mode[1)]

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
SD card input setup time	t_{ISU}	6	–	ns	
SD card input hold time	t_{IH}	2	–	ns	
SD card output valid time	t_{ODLY}	–	14	ns	
SD card output hold time	t_{OH}	2.5	–	ns	

1) Reference card timing values for calculation examples. Not subject to production test and not characterized.

High-Speed Output Path (Write)

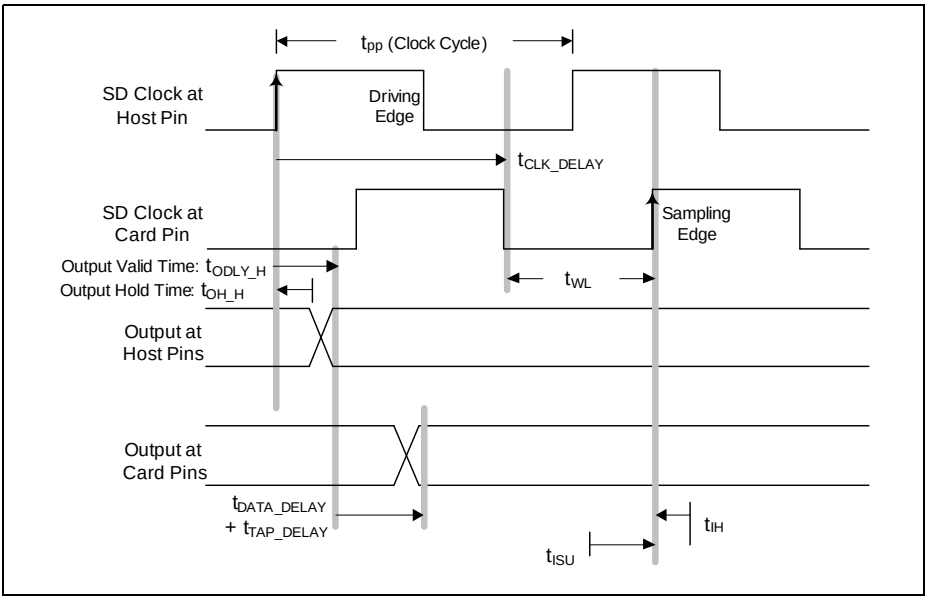

Figure 39 High-Speed Output Path

High-Speed Write Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

3.3.10.3 EBU Arbitration Signal Timing

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 60 EBU Arbitration Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Output delay from BFCLKO rising edge	t_1	CC	–	–	16	ns	C_L = 50 pF
Data setup to BFCLKO falling edge	t_2	SR	11	–	–	ns	–
Data hold from BFCLKO falling edge	t_3	SR	2	–	–	ns	–

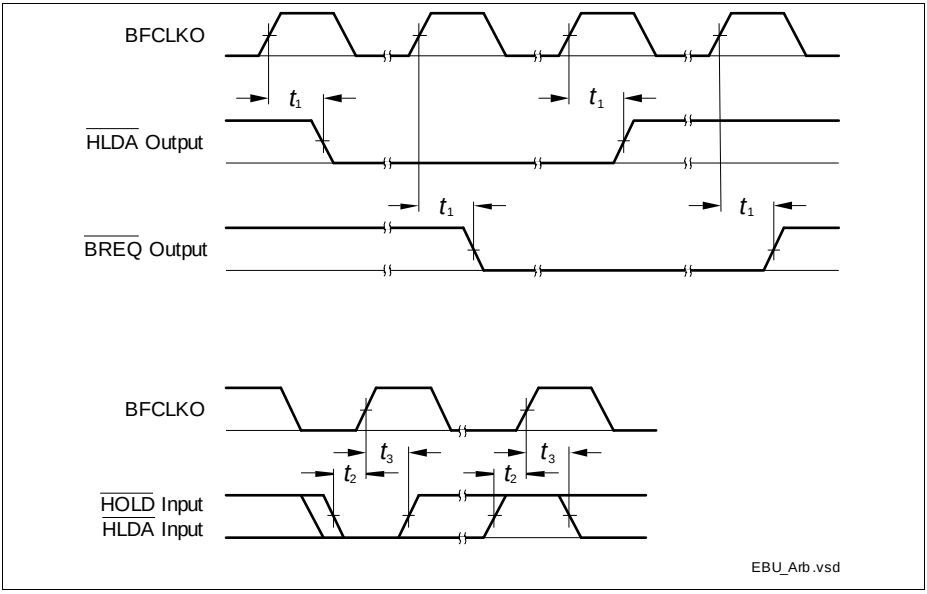

Figure 46 EBU Arbitration Signal Timing

3.3.12 Ethernet Interface (ETH) Characteristics

For proper operation of the Ethernet Interface it is required that $f_{SYS} \geq 100$ MHz.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.12.1 ETH Measurement Reference Points

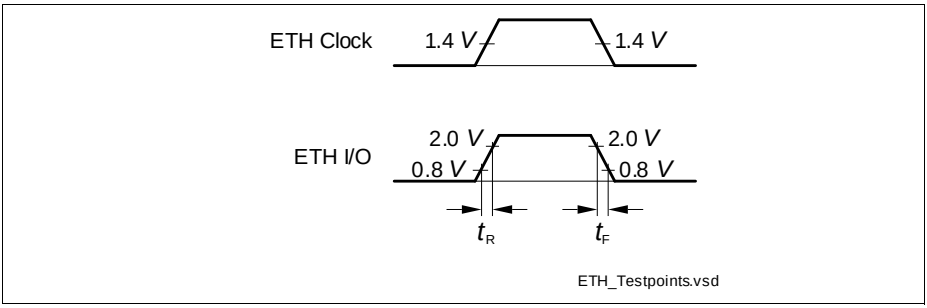

Figure 51 ETH Measurement Reference Points

3.3.12.4 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 66 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	4	–	15	ns	

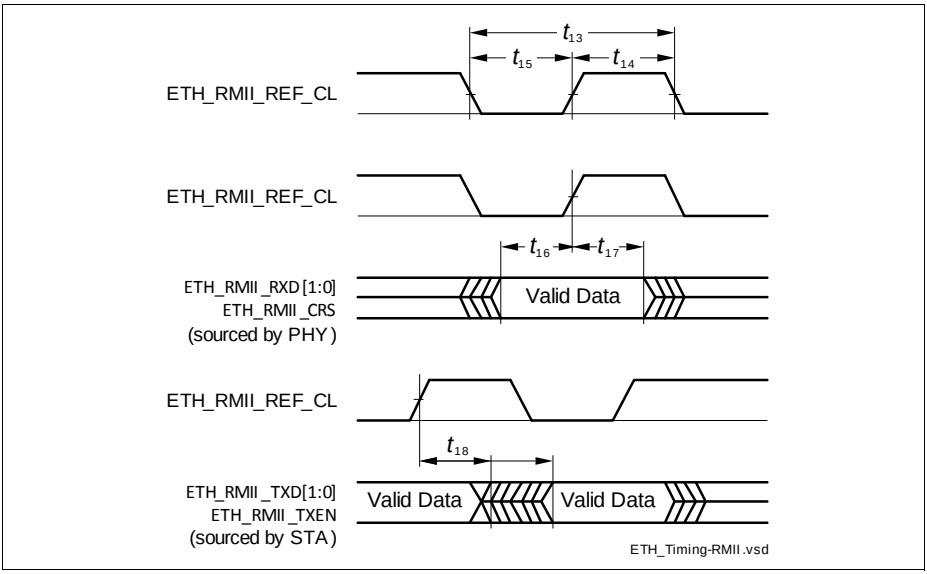

Figure 54 ETH RMII Signal Timing

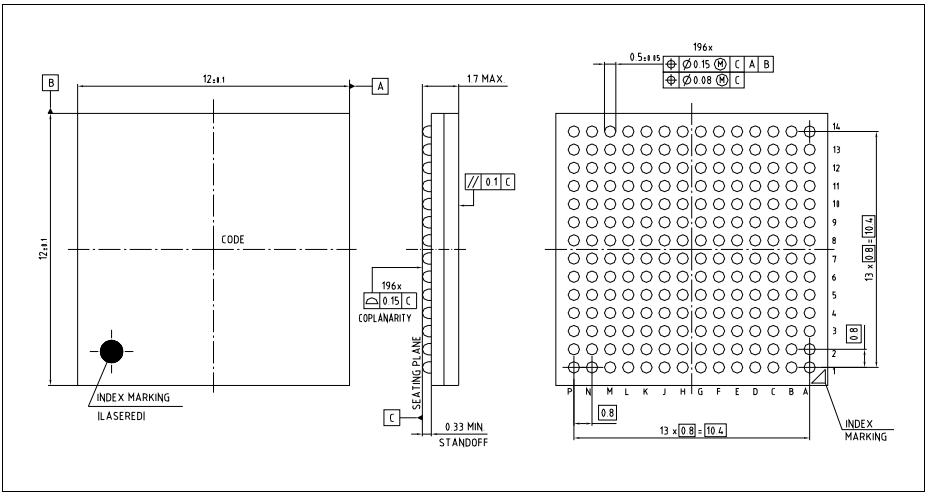

Figure 62 PG-LFBGA-196-2 (Plastic Green Low Profile Fine Pitch Ball Grid Array)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**