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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I ² C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I ² S, LED, POR, Touch-Sense, WDT
Number of I/O	119
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	200K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-24
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800f144k1024aaxqma1

1 Summary of Features

The XMC4[78]00 devices are members of the XMC4000 Family of microcontrollers based on the ARM Cortex-M4 processor core. The XMC4000 is a family of high performance and energy efficient microcontrollers optimized for Industrial Connectivity, Industrial Control, Power Conversion, Sense & Control.

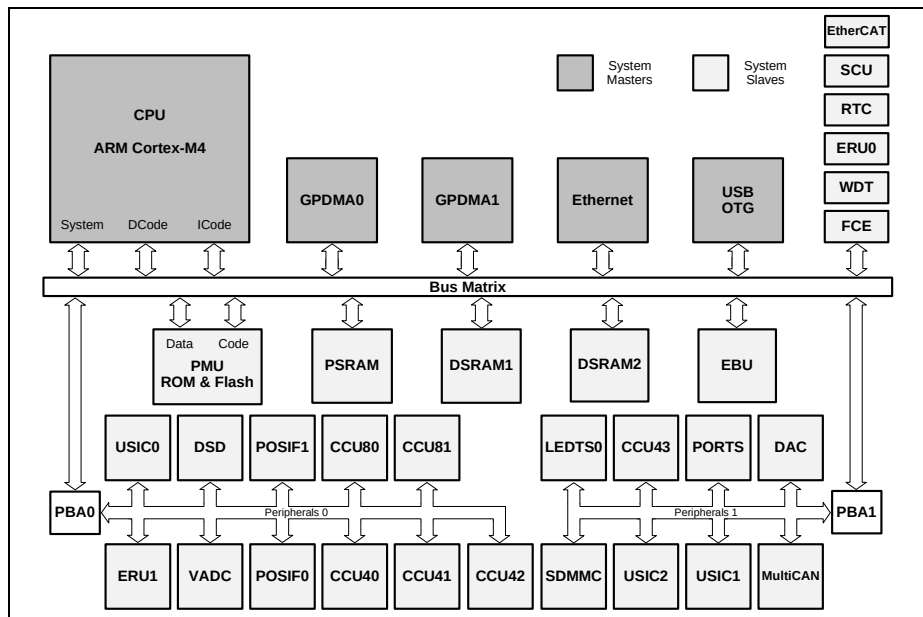


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
 - High Performance 32-bit ARM Cortex-M4 CPU
 - 16-bit and 32-bit Thumb2 instruction set
 - DSP/MAC instructions
 - System timer (SysTick) for Operating System support
- Floating Point Unit
- Memory Protection Unit
- Nested Vectored Interrupt Controller
- General Purpose DMA with up-to channels
- Event Request Unit (ERU) for programmable processing of external and internal service requests
- Flexible CRC Engine (FCE) for multiple bit error detection

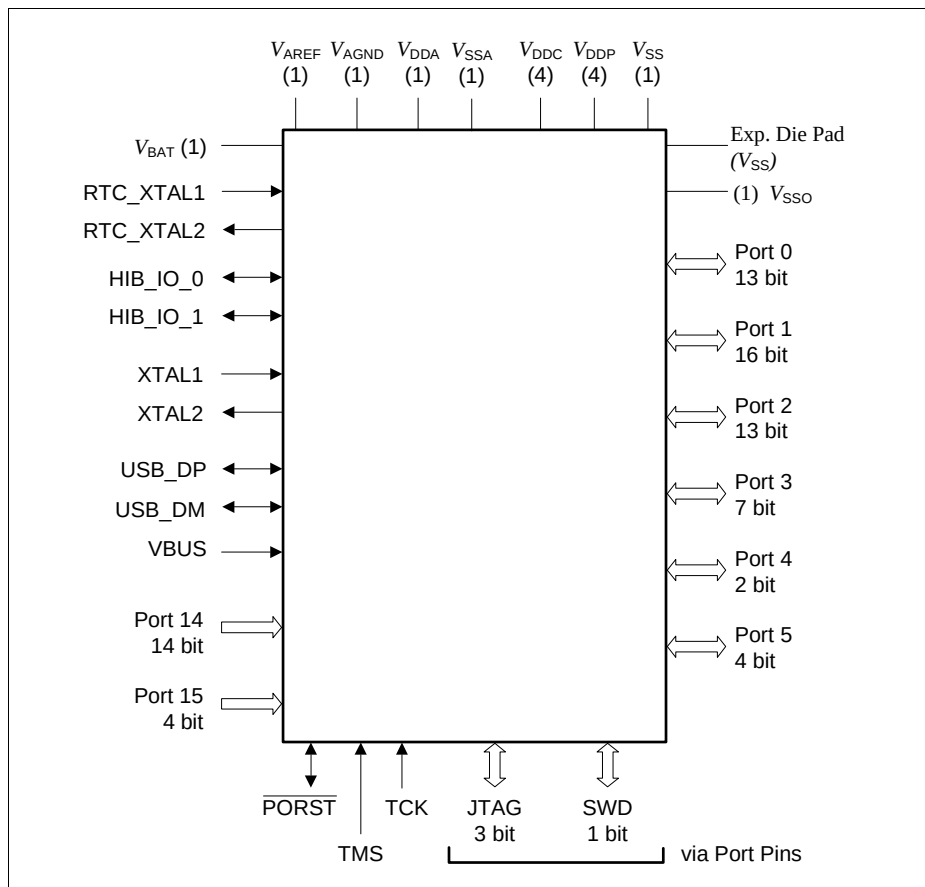


Figure 4 XMC4[78]00 Logic Symbol PG-LQFP-100

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the four sides of the different packages.

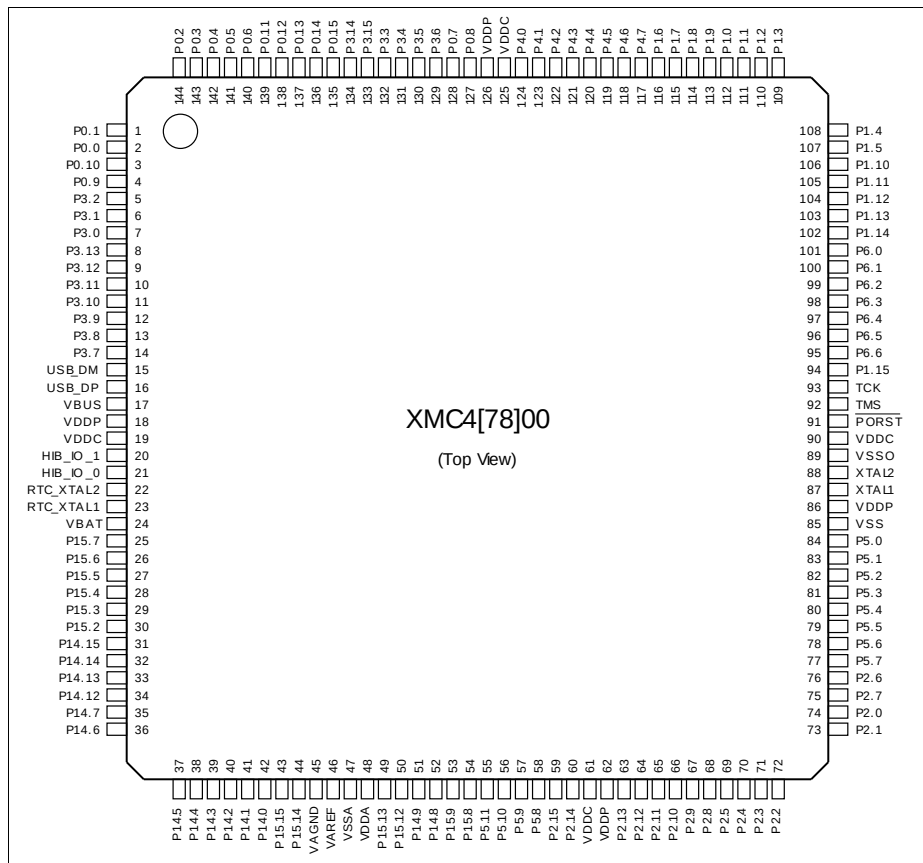


Figure 5 XMC4[78]00 PG-LQFP-144 Pin Configuration (top view)

General Device Information

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	VSS	P8.6	P8.8	P8.10	P8.9	P8.11	P8.1	P9.8	P9.7	P9.9	P9.5	P9.4	n.c.	VSS	A
B	n.c.	P8.3	P8.2	P8.7	P8.5	P8.4	P8.0	P9.10	P9.11	n.c.	P9.6	n.c.	VSS	n.c.	B
C	VSS	VDDC	P0.2	P0.3	P0.5	P0.6	P3.6	P0.8	P4.1	P1.8	VDDP	VSS	n.c.	n.c.	C
D	VDDP	P3.1	P3.2	P0.10	P0.4	P3.5	P0.7	P4.0	P1.6	P1.7	P1.9	VDDC	P9.3	P9.2	D
E	P3.0	P3.13	P0.1	P0.0	P0.13	P0.15	P4.4	P4.6	P4.7	P1.4	P1.2	P1.3	n.c.	P9.1	E
F	USB_D M	P3.12	P3.11	P0.9	P0.12	P3.14	P3.15	P4.5	P1.0	P1.5	P1.11	P1.10	P9.0	P7.11	F
G	USB_D P	VBUS	P3.8	P3.7	P0.11	P0.14	P3.4	P4.2	P1.1	P1.14	P1.12	P1.13	P7.9	P7.10	G
H	RTC_X TAL1	RTC_X TAL2	HIB_I O_1	HIB_I O_0	P3.9	P3.10	P3.3	P4.3	P6.1	P6.4	P6.5	P6.6	n.c.	P7.8	H
J	VBAT	P15.3	P15.5	P15.4	P15.6	P15.7	TMS	TCK	P6.3	P6.0	$\overline{\text{PORST}}$	P1.15	n.c.	P7.7	J
K	P15.2	P14.15	P14.14	P14.13	P5.10	P5.8	P5.2	P5.1	P5.0	P6.2	XTAL1	XTAL2	n.c.	P7.6	K
L	P14.12	P14.7	P14.6	P14.3	P5.11	P2.15	P5.7	P5.5	P2.6	P5.3	P2.0	VSSO	P7.0	P7.5	L
M	P14.4	P14.5	P14.2	P15.15	P15.12	P5.9	P2.14	P5.6	P2.7	P5.4	P2.2	P2.1	P7.1	P7.3	M
N	VDDA	P14.1	P14.0	P15.14	P14.9	P15.9	P2.12	P2.10	P2.8	P2.4	P2.3	VDDP	P7.2	P7.4	N
P	VSSA	VAGND	VAREF	P15.13	P14.8	P15.8	P2.13	P2.11	P2.9	P2.5	VDDC	VSS	n.c.	VSS	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

XMC4[78]00 - (top view)

Figure 6 XMC4[78]00 PG-LFBGA-196 Pin Configuration (top view)

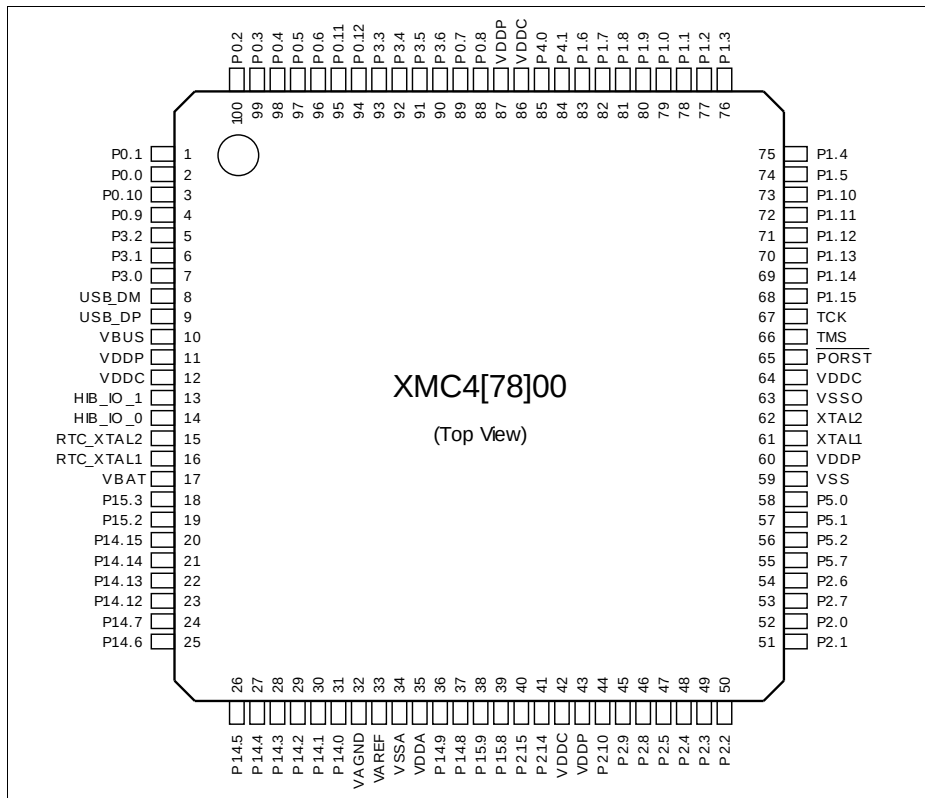


Figure 7 XMC4[78]00 PG-LQFP-100 Pin Configuration (top view)

General Device Information

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
VSS	C12	-	-	Power	
VSS	P12	-	-	Power	
VSS	P14	-	-	Power	
VSSO	L12	89	63	Power	
VSS	-	Exp. Pad	Exp. Pad	Power	Exposed Die Pad The exposed die pad is connected internally to VSS. For proper operation, it is mandatory to connect the exposed pad directly to the common ground on the board. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.
n.c.	A13	-	-	Power	
n.c.	B1	-	-	Power	
n.c.	B10	-	-	Power	
n.c.	B12	-	-	Power	
n.c.	B14	-	-	Power	
n.c.	C13	-	-	Power	
n.c.	C14	-	-	Power	
n.c.	E13	-	-	Power	
n.c.	H13	-	-	Power	
n.c.	J13	-	-	Power	
n.c.	K13	-	-	Power	
n.c.	P13	-	-	Power	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
XTAL1									UBC0. DX0F	UBC1. DX0F	U1C0. DX0F	U1C1. DX0F	U2C0. DX0F	U2C1. DX0F		
XTAL2																
RTC_XTAL1											ERU0. 1B1					
RTC_XTAL2																

The XMC4[78]00 has a common ground concept, all V_{SS} , V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.

V_{AGND} is the low potential to the analog reference V_{AREF} . Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT} , the V_{BAT} pin can also be connected directly to V_{DDP} .

Table 15 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}, T_J = -40 \text{ }^{\circ}\text{C}$	$I_{OV} = 5 \text{ mA}, T_J = 150 \text{ }^{\circ}\text{C}$
A1 / A1+	$V_{IN} = V_{DDP} + 1.0 \text{ V}$	$V_{IN} = V_{DDP} + 0.75 \text{ V}$
A2	$V_{IN} = V_{DDP} + 0.7 \text{ V}$	$V_{IN} = V_{DDP} + 0.6 \text{ V}$
AN/DIG_IN	$V_{IN} = V_{DDP} + 1.0 \text{ V}$	$V_{IN} = V_{DDP} + 0.75 \text{ V}$

Table 16 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}, T_J = -40 \text{ }^{\circ}\text{C}$	$I_{OV} = 5 \text{ mA}, T_J = 150 \text{ }^{\circ}\text{C}$
A1 / A1+	$V_{IN} = V_{SS} - 1.0 \text{ V}$	$V_{IN} = V_{SS} - 0.75 \text{ V}$
A2	$V_{IN} = V_{SS} - 0.7 \text{ V}$	$V_{IN} = V_{SS} - 0.6 \text{ V}$
AN/DIG_IN	$V_{IN} = V_{DDP} - 1.0 \text{ V}$	$V_{IN} = V_{DDP} - 0.75 \text{ V}$

Table 17 Port Groups for Overload and Short-Circuit Current Sum Parameters

Group	Pins
1	P0.[15:0], P3.[15:0], P8.[11:0]
2	P14.[15:0], P15.[15:0]
3	P2.[15:0], P5.[11:0], P7.[11:0]
4	P1.[15:0], P4.[7:0], P6.[6:0], P9.[11:0]

Table 23 Standard Pads Class_A2

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input Leakage current	I_{OZA2} CC	-6	6	μA	$0\text{ V} \leq V_{\text{IN}} < 0.5 \cdot V_{\text{DDP}} - 1\text{ V};$ $0.5 \cdot V_{\text{DDP}} + 1\text{ V} < V_{\text{IN}} \leq V_{\text{DDP}}$
		-3	3	μA	$0.5 \cdot V_{\text{DDP}} - 1\text{ V} < V_{\text{IN}} < 0.5 \cdot V_{\text{DDP}} + 1\text{ V}$
Input high voltage	V_{IHA2} SR	$0.6 \times V_{\text{DDP}}$	$V_{\text{DDP}} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA2} SR	-0.3	$0.36 \times V_{\text{DDP}}$	V	
Output high voltage, POD = weak	V_{OHA2} CC	$V_{\text{DDP}} - 0.4$	–	V	$I_{\text{OH}} \geq -400\text{ }\mu\text{A}$
		2.4	–	V	$I_{\text{OH}} \geq -500\text{ }\mu\text{A}$
$V_{\text{DDP}} - 0.4$		–	V	$I_{\text{OH}} \geq -1.4\text{ mA}$	
		2.4	–	V	$I_{\text{OH}} \geq -2\text{ mA}$
Output high voltage, POD = strong		$V_{\text{DDP}} - 0.4$	–	V	$I_{\text{OH}} \geq -1.4\text{ mA}$
		2.4	–	V	$I_{\text{OH}} \geq -2\text{ mA}$
Output low voltage, POD = weak	V_{OLA2} CC	–	0.4	V	$I_{\text{OL}} \leq 500\text{ }\mu\text{A}$
Output low voltage, POD = medium		–	0.4	V	$I_{\text{OL}} \leq 2\text{ mA}$
Output low voltage, POD = strong		–	0.4	V	$I_{\text{OL}} \leq 2\text{ mA}$

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Input leakage current	I_{OZHIB} CC	-500	500	nA	$0\text{ V} \leq V_{IN} \leq V_{BAT}$
Input high voltage	V_{IHIB} SR	$0.6 \times V_{BAT}$	$V_{BAT} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3	$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins ¹⁾	$HYSHIB$ CC	$0.1 \times V_{BAT}$	–	V	$V_{BAT} \geq 3.13\text{ V}$
		$0.06 \times V_{BAT}$	–	V	$V_{BAT} < 3.13\text{ V}$
Output high voltage, POD ¹⁾ = medium	V_{OHIB} CC	$V_{BAT} - 0.4$	–	V	$I_{OH} \geq -1.4\text{ mA}$
Output low voltage	V_{OLHIB} CC	–	0.4	V	$I_{OL} \leq 2\text{ mA}$
Fall time	t_{FHIB} CC	–	50	ns	$V_{BAT} \geq 3.13\text{ V}$ $C_L = 50\text{ pF}$
		–	100	ns	$V_{BAT} < 3.13\text{ V}$ $C_L = 50\text{ pF}$
Rise time	t_{RHIB} CC	–	50	ns	$V_{BAT} \geq 3.13\text{ V}$ $C_L = 50\text{ pF}$
		–	100	ns	$V_{BAT} < 3.13\text{ V}$ $C_L = 50\text{ pF}$

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.5 Die Temperature Sensor

The Die Temperature Sensor (DTS) measures the junction temperature T_J .

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 29 Die Temperature Sensor Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Temperature sensor range	T_{SR} SR	-40	–	150	°C	
Linearity Error (to the below defined formula)	ΔT_{LE} CC	–	±1	–	°C	per $\Delta T_J \leq 30$ °C
Offset Error	ΔT_{OE} CC	–	±6	–	°C	$\Delta T_{OE} = T_J - T_{DTS}$ $V_{DDP} \leq 3.3$ V ¹⁾
Measurement time	t_M CC	–	–	100	µs	
Start-up time after reset inactive	t_{TSST} SR	–	–	10	µs	

1) At $V_{DDP_max} = 3.63$ V the typical offset error increases by an additional $\Delta T_{OE} = \pm 1$ °C.

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

$$\text{Temperature } T_{DTS} = (\text{RESULT} - 605) / 2.05 \text{ [°C]}$$

This formula and the values defined in [Table 29](#) apply with the following calibration values:

- DTSCON.BGTRIM = 8_H
- DTSCON.REFTRIM = 4_H

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:

$$V_{DDP} = 3.3 \text{ V}, T_A = 25 \text{ }^{\circ}\text{C}$$

Table 34 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Active supply current ¹⁾¹¹⁾ Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	I_{DDPA} CC	–	135	–	mA	144 / 144 / 144
		–	125	–		144 / 72 / 72
		–	97	–		72 / 72 / 144
		–	80	–		24 / 24 / 24
		–	68	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA} CC	–	108	–	mA	144 / 144 / 144
		–	98	–		144 / 72 / 72
Active supply current ²⁾ Peripherals disabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	I_{DDPA} CC	–	86	–	mA	144 / 144 / 144
		–	85	–		144 / 72 / 72
		–	70	–		72 / 72 / 144
		–	55	–		24 / 24 / 24
		–	50	–		1 / 1 / 1
Sleep supply current ³⁾ Peripherals enabled Frequency: $f_{CPU} / f_{PERIPH} / f_{CCU}$ in MHz	I_{DDPS} CC	–	127	–	mA	144 / 144 / 144
		–	115	–		144 / 72 / 72
		–	93	–		72 / 72 / 144
		–	57	–		24 / 24 / 24
		–	47	–		1 / 1 / 1
$f_{CPU} / f_{PERIPH} / f_{CCU}$ in kHz		–	48	–		100 / 100 / 100

3.3.2 Power-Up and Supply Monitoring

$\overline{\text{PORST}}$ is always asserted when V_{DDP} and/or V_{DDC} violate the respective thresholds.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

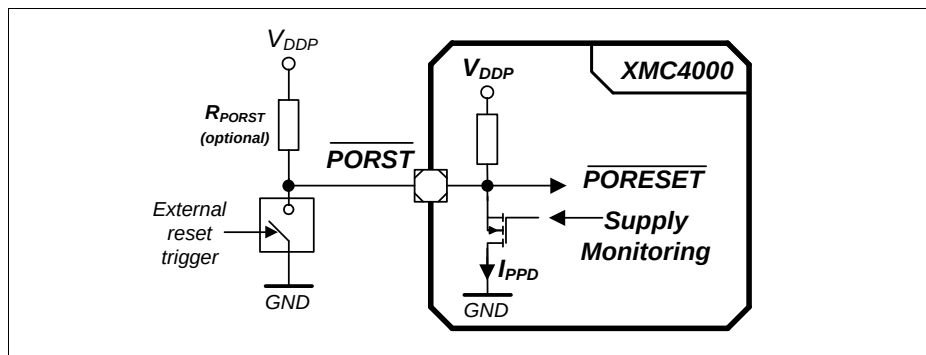


Figure 25 **$\overline{\text{PORST}}$ Circuit**

Table 37 **Supply Monitoring Parameters**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital supply voltage reset threshold	V_{POR} CC	2.79 ¹⁾	–	3.05 ²⁾	V	³⁾
Core supply voltage reset threshold	V_{PV} CC	–	–	1.17	V	
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
$\overline{\text{PORST}}$ rise time	t_{PR} SR	–	–	2	μs	⁴⁾
Startup time from power-on reset with code execution from Flash	t_{SSW} CC	–	2.5	3.5	ms	Time to the first user code instruction
V_{DDC} ramp up time	t_{VCR} CC	–	550	–	μs	Ramp up after power-on or after a reset triggered by a violation of V_{POR} or V_{PV}

1) Minimum threshold for reset assertion.

- 2) Maximum threshold for reset deassertion.
- 3) The V_{DDP} monitoring has a typical hysteresis of $V_{PORHYS} = 180 \text{ mV}$.
- 4) If t_{PR} is not met, low spikes on $\overline{\text{PORST}}$ may be seen during start up (e.g. reset pulses generated by the supply monitoring due to a slow ramping V_{DDP}).

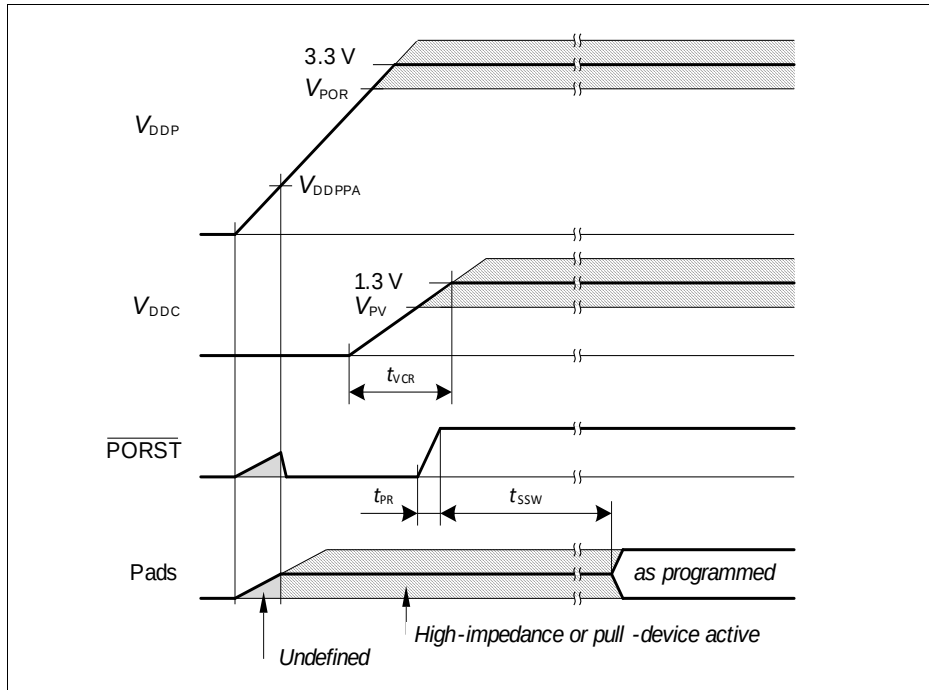


Figure 26 Power-Up Behavior

3.3.3 Power Sequencing

While starting up and shutting down as well as when switching power modes of the system it is important to limit the current load steps. A typical cause for such load steps is changing the CPU frequency f_{CPU} . Load steps exceeding the below defined values may cause a power on reset triggered by the supply monitor.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 48 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

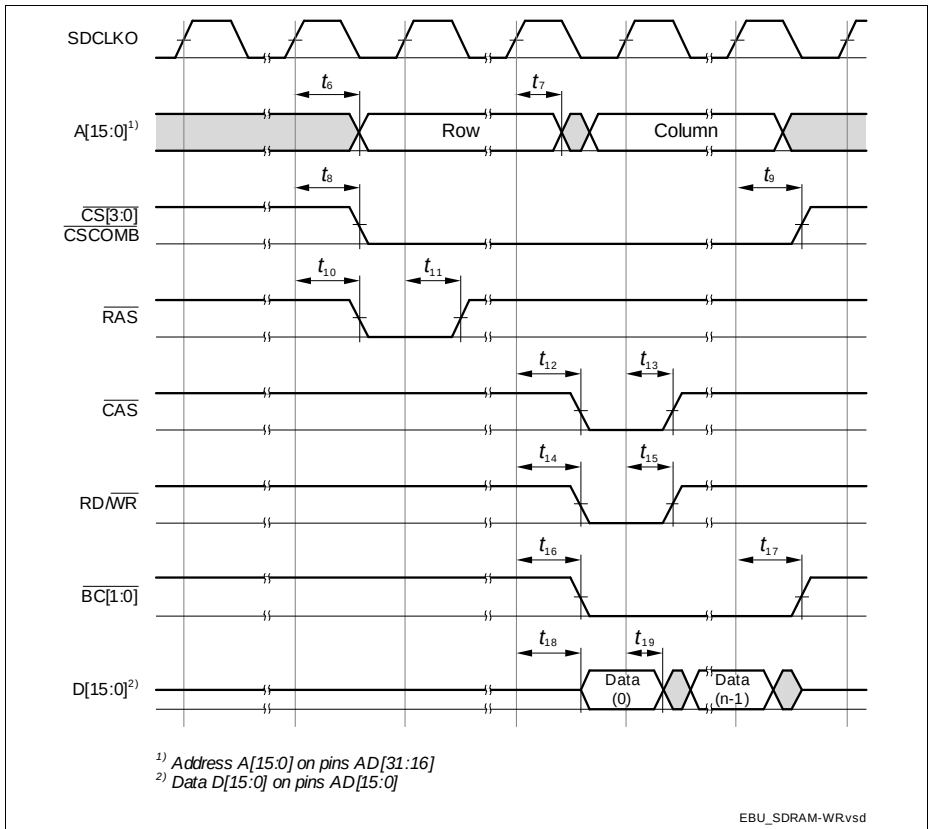


Figure 49 EBU SDRAM Write Access Timing

3.3.12.2 ETH Management Signal Parameters (ETH_MDC, ETH_MDIO)

Table 64 ETH Management Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condi tion
			Min.	Typ.	Max.		
ETH_MDC period	t_1	CC	400	—	—	ns	$C_L = 25 \text{ pF}$
ETH_MDC high time	t_2	CC	160	—	—	ns	
ETH_MDC low time	t_3	CC	160	—	—	ns	
ETH_MDIO setup time (output)	t_4	CC	10	—	—	ns	
ETH_MDIO hold time (output)	t_5	CC	10	—	—	ns	
ETH_MDIO data valid (input)	t_6	SR	0	—	300	ns	

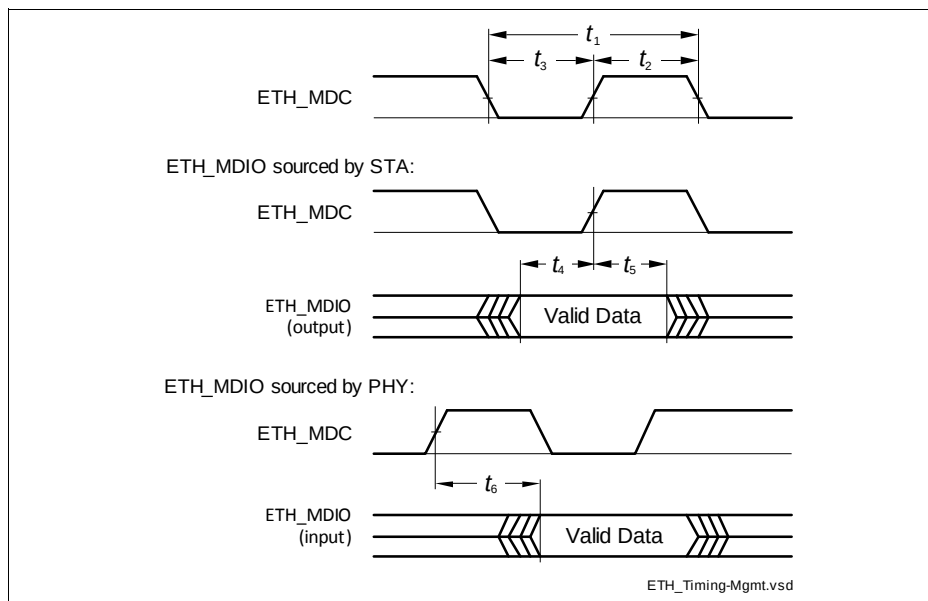


Figure 52 ETH Management Signal Timing

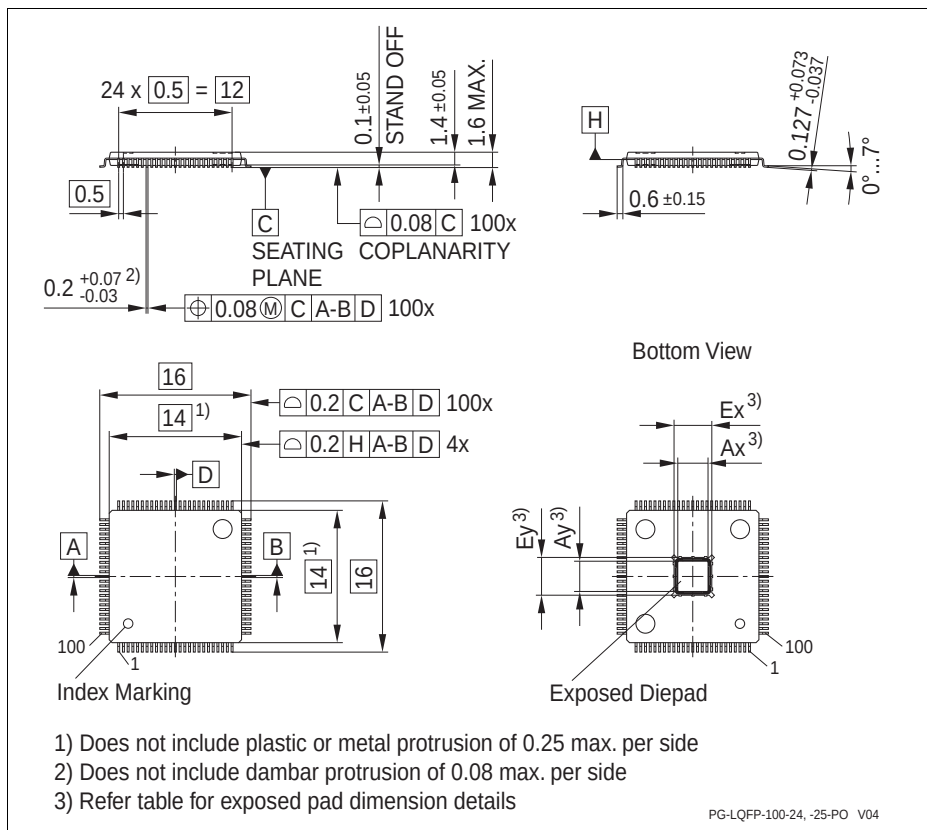


Figure 61 PG-LQFP-100-25 (Plastic Green Low Profile Quad Flat Package)

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