Infineon Technologies - XMC4800F144K1536AAXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, EBI/EMI, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	119
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	276K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-144-24
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4800f144k1536aaxqma1

Table of Contents

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4[78]00 series devices.

The document describes the characteristics of a superset of the XMC4[78]00 series devices. For simplicity, the various device types are referred to by the collective term XMC4[78]00 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

Table 3 Features of XMC4[78]00 Device Types (cont'd)

Derivative[1)]	ADC Chan.	DSD Chan.	DAC Chan.	CCU4 Slice	CCU8 Slice	POSIF Intf.
XMC4800-F144x2048	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x2048	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1536	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1536	24	4	2	4 x 4	2 x 4	2
XMC4800-E196x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F144x1024	32	4	2	4 x 4	2 x 4	2
XMC4800-F100x1024	24	4	2	4 x 4	2 x 4	2

1) x is a placeholder for the supported temperature range.

1.4 Definition of Feature Variants

The XMC4[78]00 types are offered with several memory sizes and number of available VADC channels. **Table 4** describes the location of the available Flash memory, **Table 5** describes the location of the available SRAMs, **Table 6** the available VADC channels.

Table 4 Flash Memory Ranges

Total Flash Size	Cached Range	Uncached Range
1,024 Kbytes	$0800\ 0000_H$ – $080F\ FFFF_H$	$0C00\ 0000_H$ – $0C0F\ FFFF_H$
1,536 Kbytes	$0800\ 0000_H$ – $0817\ FFFF_H$	$0C00\ 0000_H$ – $0C17\ FFFF_H$
2,048 Kbytes	$0800\ 0000_H$ – $081F\ FFFF_H$	$0C00\ 0000_H$ – $0C1F\ FFFF_H$

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P5.3	L10	81	-	A2	
P5.4	M10	80	-	A2	
P5.5	L8	79	-	A2	
P5.6	M8	78	-	A2	
P5.7	L7	77	55	A1+	
P5.8	K6	58	-	A2	
P5.9	M6	57	-	A2	
P5.10	K5	56	-	A1+	
P5.11	L5	55	-	A1+	
P6.0	J10	101	-	A2	
P6.1	H9	100	-	A2	
P6.2	K10	99	-	A2	
P6.3	J9	98	-	A1+	
P6.4	H10	97	-	A2	
P6.5	H11	96	-	A2	
P6.6	H12	95	-	A2	
P7.0	L13	-	-	A2	
P7.1	M13	-	-	A2	
P7.2	N13	-	-	A2	
P7.3	M14	-	-	A2	
P7.4	N14	-	-	A1+	
P7.5	L14	-	-	A1+	
P7.6	K14	-	-	A1+	
P7.7	J14	-	-	A1+	
P7.8	H14	-	-	A2	
P7.9	G13	-	-	A1+	
P7.10	G14	-	-	A1+	
P7.11	F14	-	-	A1+	
P8.0	B7	-	-	A2	
P8.1	A7	-	-	A2	
P8.2	B3	-	-	A2	
P8.3	B2	-	-	A2	
P8.4	B6	-	-	A1+	

Table 10 Package Pin Mapping (cont'd)

Function	LFBGA-196	LQFP-144	LQFP-100	Pad Type	Notes
P8.5	B5	-	-	A1+	
P8.6	A2	-	-	A1+	
P8.7	B4	-	-	A1+	
P8.8	A3	-	-	A2	
P8.9	A5	-	-	A1+	
P8.10	A4	-	-	A1+	
P8.11	A6	-	-	A1+	
P9.0	F13	-	-	A2	
P9.1	E14	-	-	A2	
P9.2	D14	-	-	A1+	
P9.3	D13	-	-	A2	
P9.4	A12	-	-	A1+	
P9.5	A11	-	-	A1+	
P9.6	B11	-	-	A1+	
P9.7	A9	-	-	A1+	
P9.8	A8	-	-	A1+	
P9.9	A10	-	-	A1+	
P9.10	B8	-	-	A1+	
P9.11	B9	-	-	A1+	
P14.0	N3	42	31	AN/DIG_IN	
P14.1	N2	41	30	AN/DIG_IN	
P14.2	M3	40	29	AN/DIG_IN	
P14.3	L4	39	28	AN/DIG_IN	
P14.4	M1	38	27	AN/DIG_IN	
P14.5	M2	37	26	AN/DIG_IN	
P14.6	L3	36	25	AN/DIG_IN	
P14.7	L2	35	24	AN/DIG_IN	
P14.8	P5	52	37	AN/DAC/DIG_IN	
P14.9	N5	51	36	AN/DAC/DIG_IN	
P14.12	L1	34	23	AN/DIG_IN	
P14.13	K4	33	22	AN/DIG_IN	

Table 12 Port I/O Functions (cont'd)

Function	Outputs						Inputs									
	ALT1	ALT2	ALT3	ALT4	HWO0	HWO1	HWI0	HWI1	Input	Input	Input	Input	Input	Input	Input	Input
P1.5	CAN. N1_TXD	U0C0. DOUT0	CCU80. OUT23	CCU81. OUT10	U0C0. DOUT0		U0C0. HWIN0		U0C0. DX0A	CAN. N0_RXDA	ERU0. 2A0	ERU1. 0A0	CCU41. IN1C	DSD. DIN2B		ECAT0. P0_RXD1A
P1.6	ECAT0. P0_TXD0	U0C0. SCLKOUT			SDMMC. DATA1_OUT	EBU. AD10	SDMMC. DATA1_IN	EBU. D10	DSD. DIN2A							
P1.7	ECAT0. P0_TXD1	U0C0. DOUT0	DSD. MCLK2	U1C1. SELO2	SDMMC. DATA2_OUT	EBU. AD11	SDMMC. DATA2_IN	EBU. D11		DSD. MCLK2A			DSD. MCLK0C			
P1.8	ECAT0. P0_TXD2	U0C0. SELO1	DSD. MCLK1	U1C1. SCLKOUT	SDMMC. DATA4_OUT	EBU. AD12	SDMMC. DATA4_IN	EBU. D12	CAN. N2_RXDA	DSD. MCLK1A			DSD. MCLK0D	DSD. MCLK2D	DSD. MCLK3D	
P1.9	U0C0. SCLKOUT	CAN. N2_TXD	DSD. MCLK0	U1C1. DOUT0	SDMMC. DATA5_OUT	EBU. AD13	SDMMC. DATA5_IN	EBU. D13		DSD. MCLK0A			DSD. MCLK1C	DSD. MCLK2C	DSD. MCLK3C	ECAT0. P0_RX_DVA
P1.10	ETH0. MDC	U0C0. SCLKOUT	CCU81. OUT21	ECAT0. LED_ERR			SDMMC. SDCD						CCU41. IN2C			ECAT0. P0_RXD2A
P1.11	ECAT0. LED_STATE_RUN	U0C0. SELO0	CCU81. OUT11	ECAT0. LED_RUN	ETH0. MDO		ETH0. MDIC						CCU41. IN3C			ECAT0. P0_RXD3A
P1.12	ETH0. TX_EN	CAN. N1_TXD	CCU81. OUT01	ECAT0. P0_LINK_ACT	SDMMC. DATA6_OUT	EBU. AD16	SDMMC. DATA6_IN	EBU. D16								
P1.13	ETH0. TXD0	U0C1. SELO3	CCU81. OUT20	ECAT0. PHY_CLK25	SDMMC. DATA7_OUT	EBU. AD17	SDMMC. DATA7_IN	EBU. D17	CAN. N1_RXDC							
P1.14	ETH0. TXD1	U0C1. SELO2	CCU81. OUT10	ECAT0. SYNC0		EBU. AD18		EBU. D18	U1C0. DX0E							
P1.15	SCU. EXTCLK	DSD. MCLK2	CCU81. OUT00	U1C0. DOUT0		EBU. AD19		EBU. D19		DSD. MCLK2B		ERU1. 1A0				ECAT0. P0_LINKB
P2.0	CAN. N0_TXD	CCU81. OUT21	DSD. CGPWMN	LEDTS0. COL1	ETH0. MDO	EBU. AD20	ETH0. MDIB	EBU. D20			ERU0. 0B3		CCU40. IN1C			
P2.1	CAN. N5_TXD	CCU81. OUT11	DSD. CGPWMP	LEDTS0. COL0	DB.TDO/ TRACESWO	EBU. AD21		EBU. D21	ETH0. CLK_RMIIA			ERU1. 0B0	CCU40. IN0C			ETH0. CLKRXA
P2.2	VADC. EMUX00	CCU81. OUT01	CCU41. OUT3	LEDTS0. LINE0	LEDTS0. EXTENDED0	EBU. AD22	LEDTS0. TSIN0A	EBU. D22	ETH0. RXD0A	U0C1. DX0A	ERU0. 1B2		CCU41. IN3A			
P2.3	VADC. EMUX01	U0C1. SELO0	CCU41. OUT2	LEDTS0. LINE1	LEDTS0. EXTENDED1	EBU. AD23	LEDTS0. TSIN1A	EBU. D23	ETH0. RXD1A	U0C1. DX2A	ERU0. 1A2	POSIF1. IN2A	CCU41. IN2A			
P2.4	VADC. EMUX02	U0C1. SCLKOUT	CCU41. OUT1	LEDTS0. LINE2	LEDTS0. EXTENDED2	EBU. AD24	LEDTS0. TSIN2A	EBU. D24	ETH0. RXERA	U0C1. DX1A	ERU0. 0B2	POSIF1. IN1A	CCU41. IN1A			
P2.5	ETH0. TX_EN	U0C1. DOUT0	CCU41. OUT0	LEDTS0. LINE3	LEDTS0. EXTENDED3	EBU. AD25	LEDTS0. TSIN3A	EBU. D25	ETH0. RXDVA	U0C1. DX0B	ERU0. 0A2	POSIF1. IN0A	CCU41. IN0A			ETH0. CRS_DVA
P2.6	U2C0. SELO4	ERU1. PDOUT3	CCU80. OUT13	LEDTS0. COL3	U2C0. DOUT3		U2C0. HWIN3		DSD. DIN1B	CAN. N1_RXDA	ERU0. 1B3	CAN. N5_RXDB	CCU40. IN3C	ECAT0. P0_RX_ERRB		
P2.7	ETH0. MDC	CAN. N1_TXD	CCU80. OUT03	LEDTS0. COL2					DSD. DIN0B			ERU1. 1B0	CCU40. IN2C			
P2.8	ETH0. TXD0	ERU1. PDOUT1	CCU80. OUT32	LEDTS0. LINE4	LEDTS0. EXTENDED4	EBU. AD26	LEDTS0. TSIN4A	EBU. D26	DAC. TRIGGER5				CCU40. IN0B	CCU40. IN1B	CCU40. IN2B	CCU40. IN3B
P2.9	ETH0. TXD1	ERU1. PDOUT2	CCU80. OUT22	LEDTS0. LINE5	LEDTS0. EXTENDED5	EBU. AD27	LEDTS0. TSIN5A	EBU. D27	DAC. TRIGGER4				CCU41. IN0B	CCU41. IN1B	CCU41. IN2B	CCU41. IN3B
P2.10	VADC. EMUX10	ERU1. PDOUT0	ECAT0. PHY_RST	ECAT0. SYNC1	DB. ETM_TRACEDATA3	EBU. AD28		EBU. D28								
P2.11	ETH0. TXER	ECAT0. P1_TXD0	CCU80. OUT22		DB. ETM_TRACEDATA2	EBU. AD29		EBU. D29								

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

Table 18 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

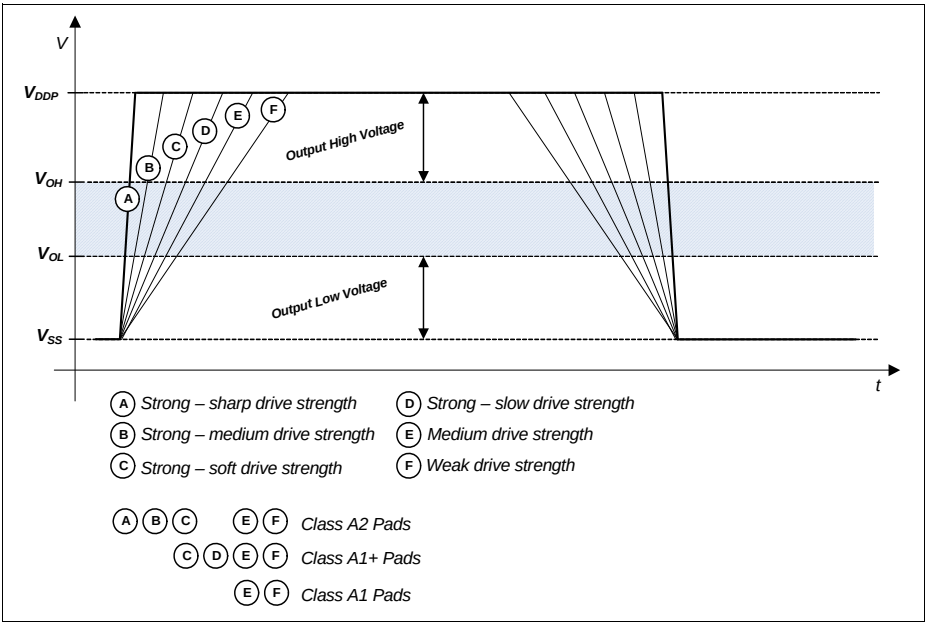

Figure 12 Output Slopes with different Pad Driver Modes

Figure 12 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

3.2 DC Parameters

3.2.1 Input/Output Pins

The digital input stage of the shared analog/digital input pins is identical to the input stage of the standard digital input/output pins.
The Pull-up on the $\overline{\text{PORST}}$ pin is identical to the Pull-up on the standard digital input/output pins.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Standard Pad Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–		10	pF	
Pull-down current	$\lvert I_{PDL}\rvert$ SR	150		–	µA	1) $V_{IN} \geq 0.6 \times V_{DDP}$
		–		10	µA	2) $V_{IN} \leq 0.36 \times V_{DDP}$
Pull-Up current	$\lvert I_{PUH}\rvert$ SR	–		10	µA	2) $V_{IN} \geq 0.6 \times V_{DDP}$
		100		–	µA	1) $V_{IN} \leq 0.36 \times V_{DDP}$
Input Hysteresis for pads of all A classes[3]	$HYSA$ CC	$0.1 \times V_{DDP}$		–	V	
$\overline{\text{PORST}}$ spike filter always blocked pulse duration	t_{SF1} CC	–		10	ns	
$\overline{\text{PORST}}$ spike filter pass-through pulse duration	t_{SF2} CC	100		–	ns	
$\overline{\text{PORST}}$ pull-down current	$\lvert I_{PPD}\rvert$ CC	13		–	mA	V_{IN} = 1.0 V

1) Current required to override the pull device with the opposite logic level (“force current”). With active pull device, at load currents between force and keep current the input state is undefined.

2) Load current at which the pull device still maintains the valid logic level (“keep current”). With active pull device, at load currents between force and keep current the input state is undefined.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 24 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0\ V \le V_{IN} \le V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$		V_{BAT} + 0.3	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$		–	V	$V_{BAT} \ge 3.13\ V$
		$0.06 \times V_{BAT}$		–	V	$V_{BAT} < 3.13\ V$
Output high voltage, POD[1] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	$I_{OH} \ge$ -1.4 mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{OL} \le 2$ mA
Fall time	t_{FHIB} CC	–		50	ns	$V_{BAT} \ge 3.13\ V$, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13\ V$, $C_L = 50$ pF
Rise time	t_{RHIB} CC	–		50	ns	$V_{BAT} \ge 3.13\ V$, $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13\ V$, $C_L = 50$ pF

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

Table 25 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Total Unadjusted Error	TUE CC	-4	–	4	LSB	12-bit resolution; V_{DDA} = 3.3 V; $V_{AREF} = V_{DDA}$ 7)
Differential Non-Linearity Error 8)	EA_{DNL} CC	-3	–	3	LSB	
Gain Error 8)	EA_{GAIN} CC	-4	–	4	LSB	
Integral Non-Linearity 8)	EA_{INL} CC	-3	–	3	LSB	
Offset Error 8)	EA_{OFF} CC	-4	–	4	LSB	
Worst case ADC V_{DDA} power supply current per active converter	I_{DDAA} CC	–	1.5	2	mA	during conversion V_{DDP} = 3.6 V, T_J = 150 °C
Charge consumption on V_{AREF} per conversion 5)	Q_{CONV} CC	–	30	–	pC	0 V ≤ V_{AREF} ≤ V_{DDA} 9)
ON resistance of the analog input path	R_{AIN} CC	–	600	1 200	Ohm	
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	
Resistance of the reference voltage input path	R_{AREF} CC	–	700	1 700	Ohm	

1) A running conversion may become imprecise in case the normal conditions are violated (voltage overshoot).

2) If the analog reference voltage is below V_{DDA}, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE, DNL, INL, Gain, and Offset errors increase also by the factor 1/k.

3) The leakage current definition is a continuous function, as shown in figure ADCx Analog Inputs Leakage. The numerical values defined determine the characteristic points of the given continuous linear approximation - they do not define step function (see **Figure 16**).

4) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements, the voltage measured at AINx can deviate from V_{AREF}/2.

5) Applies to AINx, when used as alternate reference input.

6) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead, smaller capacitances are successively switched to the reference voltage.

7) For 10-bit conversions, the errors are reduced to 1/4; for 8-bit conversions, the errors are reduced to 1/16. Never less than ±1 LSB.

8) The sum of DNL/INL/GAIN/OFF errors does not exceed the related total unadjusted error TUE.

9) The resulting current for a conversion can be calculated with $I_{AREF} = Q_{CONV} / t_c$.
The fastest 12-bit post-calibrated conversion of t_c = 459 ns results in a typical average current of I_{AREF} = 65.4 µA.

3.2.4 Out-of-Range Comparator (ORC)

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the analog reference[1] (V_{AREF}) on selected input pins (GxORCy) and generates a service request trigger (GxORCOUTy).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

The parameters in **Table 28** apply for the maximum reference voltage $V_{AREF} = V_{DDA} + 50$ mV.

Table 28 ORC Parameters (Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	100	125	210	mV	$V_{AIN} \geq V_{AREF} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	50	–	V_{ODC}	mV	
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	50	–	450	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			45	–	105	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Always detected Overvoltage Pulse	t_{OPDD}	CC	440	–	–	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			90	–	–	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	45	ns	$V_{AIN} \geq V_{AREF} + 210$ mV
			–	–	30	ns	$V_{AIN} \geq V_{AREF} + 400$ mV
Release Delay	t_{ORD}	CC	65	–	105	ns	$V_{AIN} \leq V_{AREF}$
Enable Delay	t_{OED}	CC	–	100	200	ns	

1) Always the standard VADC reference, alternate references do not apply to the ORC.

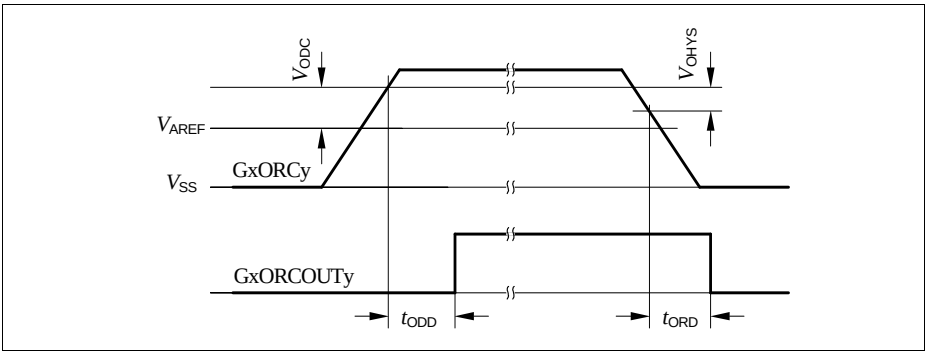

Figure 18 GxORCOUTy Trigger Generation

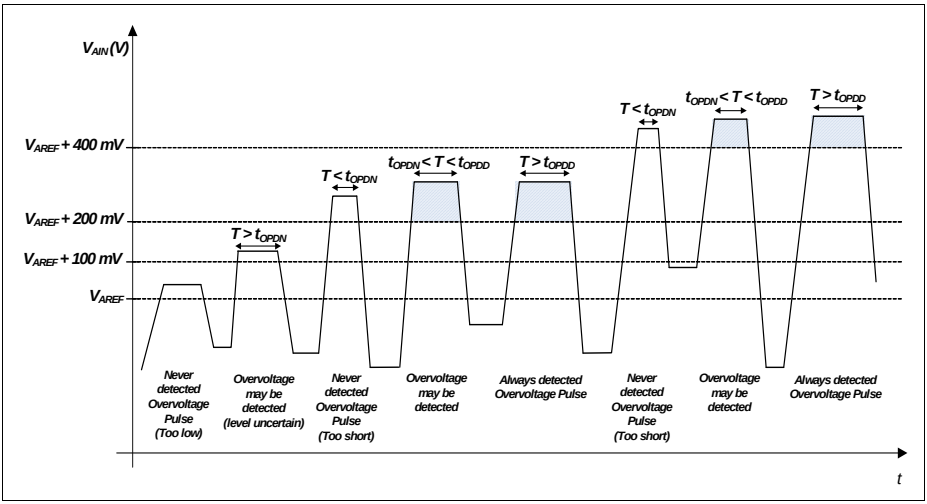

Figure 19 ORC Detection Ranges

3.2.6 USB OTG Interface DC Characteristics

The Universal Serial Bus (USB) Interface is compliant to the USB Rev. 2.0 Specification and the OTG Specification Rev. 1.3. High-Speed Mode is not supported.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 30 USB OTG VBUS and ID Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
VBUS input voltage range	V_{IN} CC	0.0	–	5.25	V	
A-device VBUS valid threshold	V_{B1} CC	4.4	–	–	V	
A-device session valid threshold	V_{B2} CC	0.8	–	2.0	V	
B-device session valid threshold	V_{B3} CC	0.8	–	4.0	V	
B-device session end threshold	V_{B4} CC	0.2	–	0.8	V	
VBUS input resistance to ground	R_{VBUS_IN} CC	40	–	100	kOhm	
B-device VBUS pull-up resistor	R_{VBUS_PU} CC	281	–	–	Ohm	Pull-up voltage = 3.0 V
B-device VBUS pull-down resistor	R_{VBUS_PD} CC	656	–	–	Ohm	
USB.ID pull-up resistor	R_{UID_PU} CC	14	–	25	kOhm	
VBUS input current	I_{VBUS_IN} CC	–	–	150	µA	$0\ V \le V_{IN} \le 5.25\ V$: T_{AVG} = 1 ms

3.2.8 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

If not stated otherwise, the operating conditions for the parameters in the following table are:
V_{DDP} = 3.3 V, T_A = 25 °C

Table 34 Power Supply Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Active supply current[1)11)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	135	–	mA	144 / 144 / 144
			–	125	–		144 / 72 / 72
			–	97	–		72 / 72 / 144
			–	80	–		24 / 24 / 24
			–	68	–		1 / 1 / 1
Active supply current Code execution from RAM Flash in Sleep mode	I_{DDPA}	CC	–	108	–	mA	144 / 144 / 144
			–	98	–		144 / 72 / 72
Active supply current[2)] Peripherals disabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPA}	CC	–	86	–	mA	144 / 144 / 144
			–	85	–		144 / 72 / 72
			–	70	–		72 / 72 / 144
			–	55	–		24 / 24 / 24
			–	50	–		1 / 1 / 1
Sleep supply current[3)] Peripherals enabled Frequency: f_{CPU} / f_{PERIPH} / f_{CCU} in MHz	I_{DDPS}	CC	–	127	–	mA	144 / 144 / 144
			–	115	–		144 / 72 / 72
			–	93	–		72 / 72 / 144
			–	57	–		24 / 24 / 24
			–	47	–		1 / 1 / 1
f_{CPU} / f_{PERIPH} / f_{CCU} in kHz			–	48	–		100 / 100 / 100

Peripheral Idle Currents

Default test conditions:

- f_{sys} and derived clocks at 144 MHz
- V_{DDP} = 3.3 V, T_a =25 °C
- all peripherals are held in reset (see the PRSTAT registers in the Reset Control Unit of the SCU)
- the peripheral clocks are disabled (see CGATSTAT registers in the Clock Control Unit of the SCU
- no I/O activity

The given values are a result of differential measurements with asserted and deasserted peripheral reset as well as disabled and enabled clock of the peripheral under test.

The tested peripheral is left in the state after the peripheral reset is deasserted, no further initialisation or configuration is done. E.g. no timer is running in the CCUs, no communication active in the USICs, etc.

Table 35 Peripheral Idle Currents

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
PORTS FCE WDT POSIFx[1)]	I_{PER} CC	–	≤ 0.3	–	mA	
MultiCAN ERU LEDTSCU0 ETH CCU4x[1)], CCU8x[1)]		–	≤ 1.0	–		
DAC (digital)[2)]		–	1.3	–		
USICx DMA1 SDMMC		–	3.0	–		
DSD, EBU VADC (digital)[2)]		–	4.5	–		
DMA0, USB, EtherCAT		–	6.0	–		

1) Enabling the f_{CCU} clock for the POSIFx/CCU4x/CCU8x modules adds approximately I_{PER} = 4.8 mA, disregarding which and how many of those peripherals are enabled.

2) The current consumption of the analog components are given in the dedicated Data Sheet sections of the respective peripheral.

Table 38 Power Sequencing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Positive Load Step Current	ΔI_{PLS} SR	-	–	50	mA	Load increase on V_{DDP} $\Delta t \leq 10$ ns
Negative Load Step Current	ΔI_{NLS} SR	-	–	150	mA	Load decrease on V_{DDP} $\Delta t \leq 10$ ns
V_{DDC} Voltage Over- / Undershoot from Load Step	ΔV_{LS} CC	-	–	±100	mV	For maximum positive or negative load step
Positive Load Step Settling Time	t_{PLSS} SR	50	–	-	µs	
Negative Load Step Settling Time	t_{NLSS} SR	100	–	-	µs	
External Buffer Capacitor on V_{DDC}	C_{EXT} SR	-	10	-	µF	In addition C = 100 nF capacitor on each V_{DDC} pin

Positive Load Step Examples

System assumptions:
$f_{CPU} = f_{SYS}$, target frequency f_{CPU} = 144 MHz, main PLL f_{VCO} = 288 MHz, stepping done by K2 divider, t_{PLSS} between individual steps:

24 MHz - 48 MHz - 72 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 4 - 3 - 2)
24 MHz - 48 MHz - 96 MHz - 144 MHz (K2 steps 12 - 6 - 3 - 2)
24 MHz - 72 MHz - 144 MHz (K2 steps 12 - 4 - 2)

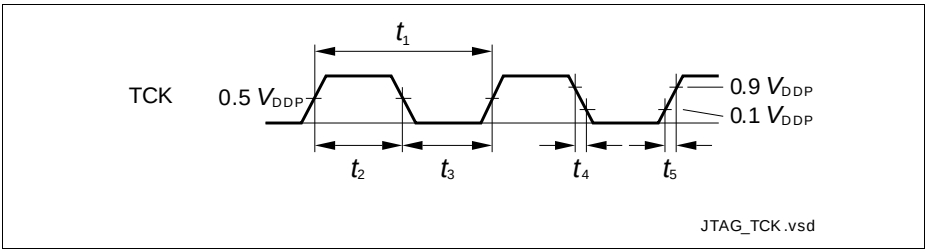

Figure 27 Test Clock Timing (TCK)

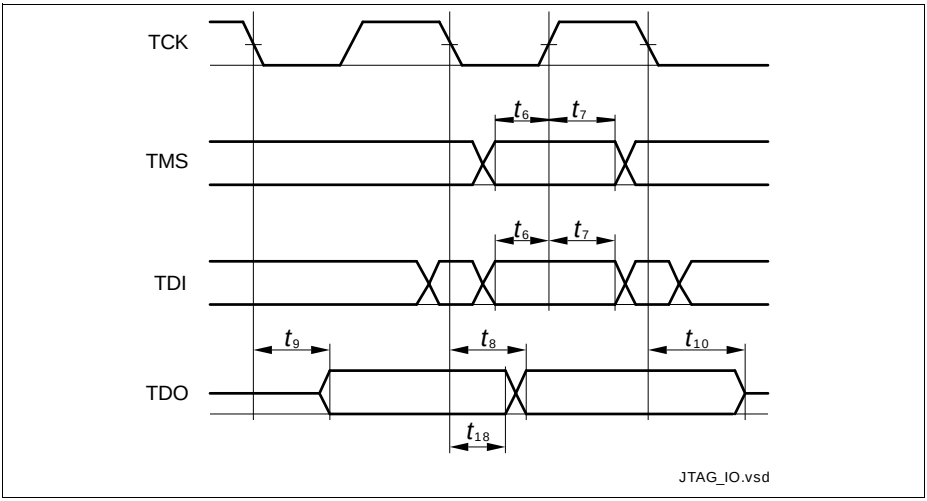

Figure 28 JTAG Timing

3.3.9.3 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 48 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Multiplexed Write Timing

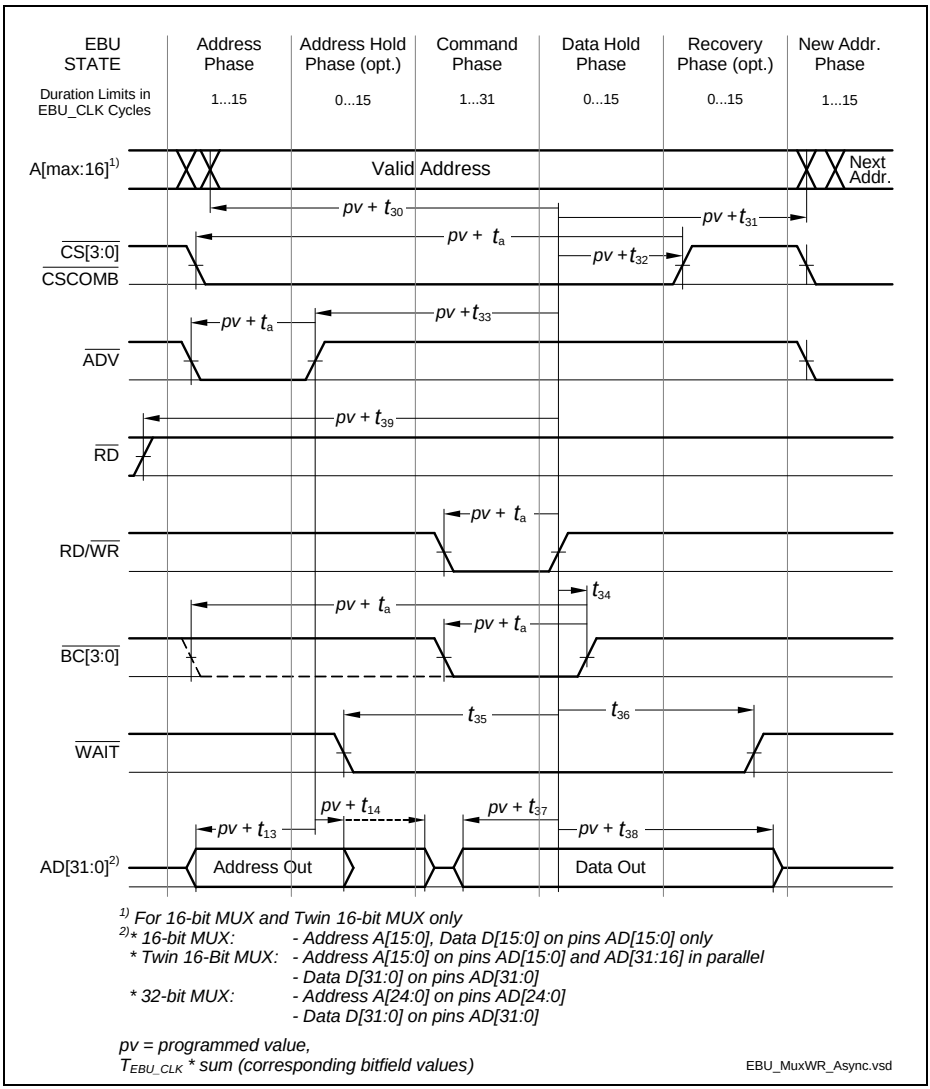

Figure 43 Multiplexed Write Access

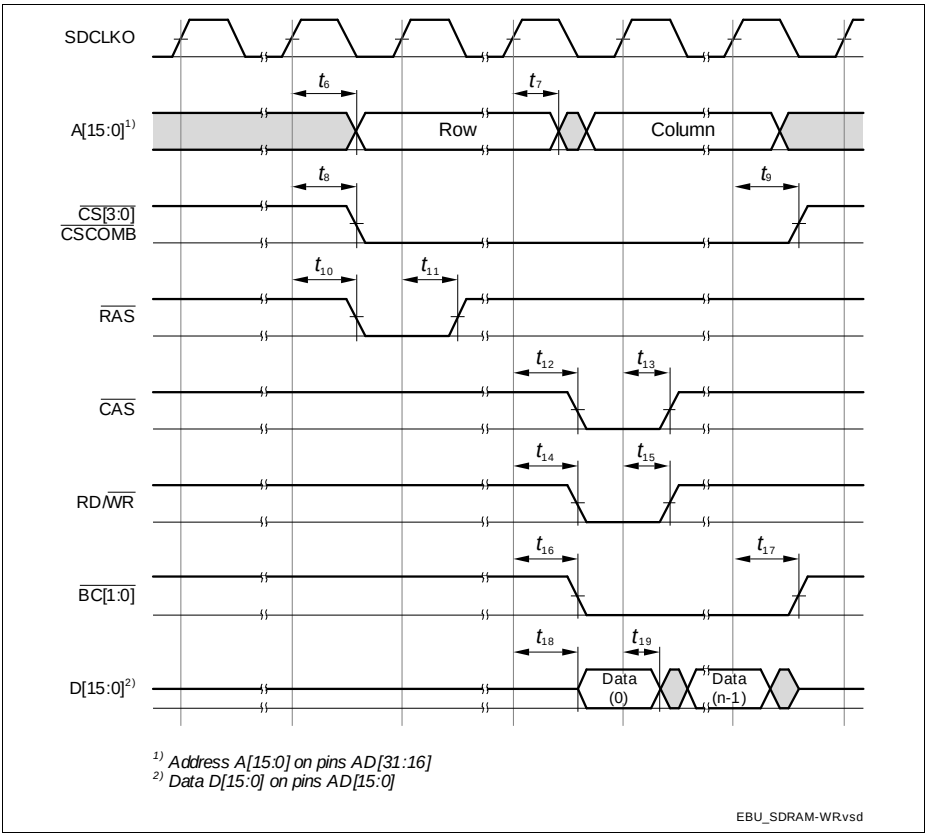

Figure 49 EBU SDRAM Write Access Timing