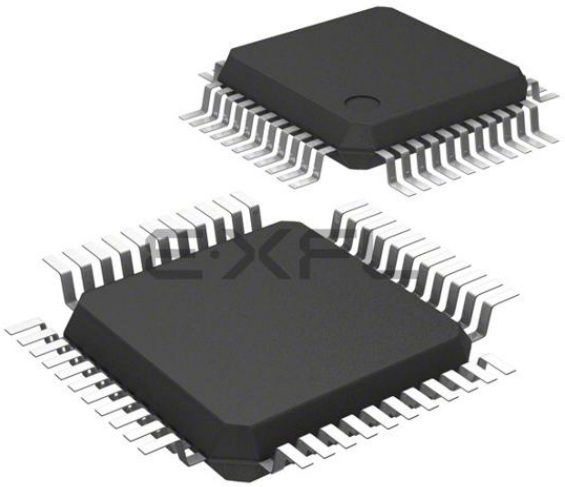
Renesas Electronics America Inc - UPD78F1000GB-GAF-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1000gb-gaf-ax

(2/2)

Item		78K0R/KF3-L					78K0R/KG3-L			
		μPD78F1010	μPD78F1011	μPD78F1012	μPD78F1027	μPD78F1028	μPD78F1013	μPD78F1014	μPD78F1029 Note 1	μPD78F1030 Note 1
Clock output/buzzer output		2								
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
10-bit resolution A/D converter (AV_{REF} = 1.8 to 5.5 V)		12 channels					16 channels			
Comparators		–								
Programmable gain amplifiers		–								
Serial interface		• CSI: 2 channels/UART: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART supporting LIN-bus: 1 channel • CSI: 2 channels/UART: 1 channel (μPD78F1027, 78F1028, 78F1029, 78F1030)								
	I^2C bus	1 channel								
Multiplier/divider		• 16 bits × 16 bits = 32 bits (multiplication) • 32 bits ÷ 32 bits = 32 bits (division)								
DMA controller		2 channels								
Vectored interrupt sources	Internal	33			35		33			35
	External	13								
Key interrupt		8 channels (KR0 to KR7)								
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by a reset processing check error								
Power-on-clear circuit		• Power-on-reset: 1.61 ±0.09 V • Power-down-reset: 1.59 ±0.09 V								
Low-voltage detector		1.91 V to 4.22 V (16 stages)								
On-chip debug function		Provided								
Power supply voltage		V_{DD} = 1.8 to 5.5 V								
Operating ambient temperature		T_A = −40 to +85 °C								

Notes 1. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(1) Port functions (2/2): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7. 8-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{SCK01}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{SCK00}$
P76				KR6
P77				KR7
P80	I/O	Port 8. 4-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P82				CMP1P/INTP7
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P140	Output	Port 14. 1-bit output port and 1-bit I/O port. For only P141, input/output can be specified. For only P141, use of an on-chip pull-up resistor can be specified by a software setting.	Output port	PCLBUZ0
P141	I/O		Input port	PCLBUZ1
P150 to P153	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI11

(1) Port functions (2/3): 78K0R/KG3-L

Function Name	I/O	Function	After Reset	Alternate Function
P50	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	$\overline{SCK40}$ Note
P51				SI40/RxD4 Note
P52				SO40/TxD4 Note
P53				$\overline{SCK41}$ Note
P54				SI41 Note
P55				SO41 Note
P56				–
P57				–
P60	I/O	Port 6. 8-bit I/O port. Output of P60 to P63 can be set to N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units. For only P64 to P67, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SCL0
P61				SDA0
P62, P63				–
P64 to P67				TI10/TO10 to TI13/TO13
P70 to P73	I/O	Port 7. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0 to KR3
P74 to P77				KR4/INTP8 to KR7/INTP11
P80 to P87	I/O	Port 8. 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P91	I/O	Port 9. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P110, P111	I/O	Port 11. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	–
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P130	Output	Port 13. 1-bit output port and 1-bit I/O port. For only P131, use of an on-chip pull-up resistor can be specified by a software setting.	Output port	–
P131	I/O		Input port	TI06/TO06

Note $\overline{SCK40}$, $\overline{SCK41}$, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

3.2.17 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

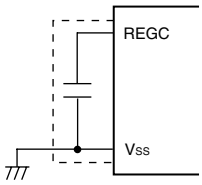
When the external reset pin is not used, connect this pin directly or via a resistor to EV_{DD0} or EV_{DD1}.

When the external reset pin is used, design the circuit based on V_{DD}.

3.2.18 REGC

This is the pin for connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF: target).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

3.2.19 FLMD0

This is a pin for setting flash memory programming mode.

Perform either of the following processing.

(a) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = “0”, default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **26.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

(b) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

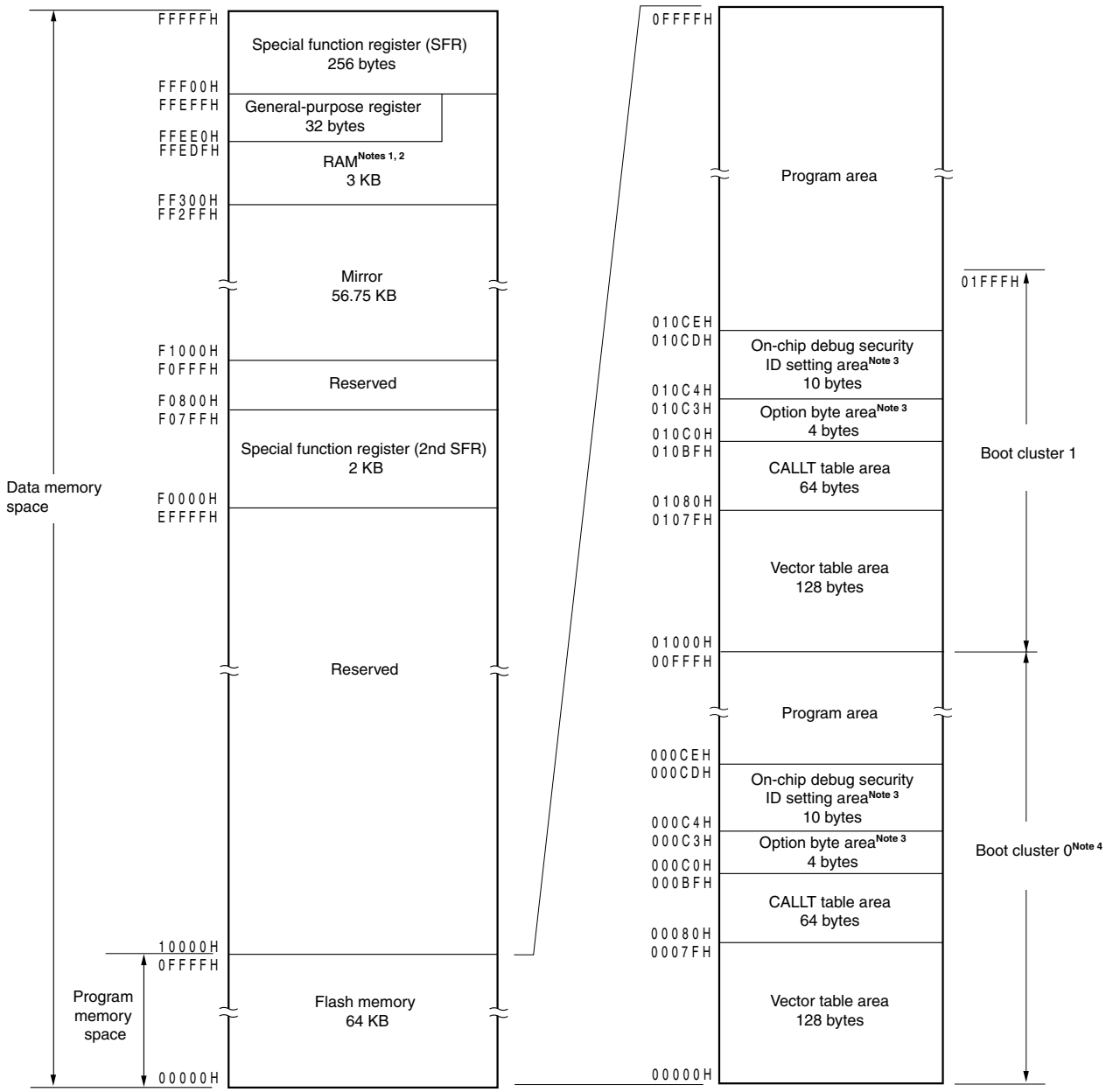
In the self programming mode, the setting is switched to pull up in the self programming library.

(c) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

Figure 4-4. Memory Map (μPD78F1003, 78F1006, 78F1009)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009.

2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Table 4-6. Extended SFR (2nd SFR) List (7/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit							
F01DCH	Timer channel stop register 1	TT1L	TT1	R/W	√	√	√	0000H	–	–	–	–	√	√
F01DDH		–			–	–			–	–	–	–	√	√
F01DEH	Timer clock select register 1	TPS1L	TPS1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01DFH		–			–	–			–	–	–	–	√	√
F01E0H	Timer output register 1	TO1L	TO1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01E1H		–			–	–			–	–	–	–	√	√
F01E2H	Timer output enable register 1	TOE1L	TOE1	R/W	√	√	√	0000H	–	–	–	–	√	√
F01E3H		–			–	–			–	–	–	–	√	√
F01E4H	Timer output level register 1	TOL1L	TOL1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01E5H		–			–	–			–	–	–	–	√	√
F01E6H	Timer output mode register 1	TOM1L	TOM1	R/W	–	√	√	0000H	–	–	–	–	√	√
F01B7H		–			–	–			–	–	–	–	√	√
F0200H	Serial status register 20	SSR20L	SSR20	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0201H		–			–	–			–	–	–	–	Note	Note
F0202H	Serial status register 21	SSR21L	SSR21	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0203H		–			–	–			–	–	–	–	Note	Note
F0204H	Serial flag clear trigger register 20	SIR20L	SIR20	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0205H		–			–	–			–	–	–	–	Note	Note
F0206H	Serial flag clear trigger register 21	SIR21L	SIR21	R/W	–	√	√	0000H	–	–	–	–	Note	Note
F0207H		–			–	–			–	–	–	–	Note	Note
F0208H	Serial mode register 20	SMR20		R/W	–	–	√	0020H	–	–	–	–	Note	Note
F0209H														
F020AH	Serial mode register 21	SMR21		R/W	–	–	√	0020H	–	–	–	–	Note	Note
F020BH														
F020CH	Serial communication operation setting register 20	SCR20		R/W	–	–	√	0087H	–	–	–	–	Note	Note
F020DH														
F020EH	Serial communication operation setting register 21	SCR21		R/W	–	–	√	0087H	–	–	–	–	Note	Note
F020FH														
F0210H	Serial channel enable status register 2	SE2L	SE2	R	√	√	√	0000H	–	–	–	–	Note	Note
F0211H		–			–	–			–	–	–	–	Note	Note
F0212H	Serial channel start register 2	SS2L	SS2	R/W	√	√	√	0000H	–	–	–	–	Note	Note
F0213H		–			–	–			–	–	–	–	Note	Note
F0214H	Serial channel stop register 2	ST2L	ST2	R/W	√	√	√	0000H	–	–	–	–	Note	Note
F0215H		–			–	–			–	–	–	–	Note	Note
F0216H	Serial clock select register2	SPS2L	SPS2	R/W	√	√	√	0000H	–	–	–	–	Note	Note
F0217H		–			–	–			–	–	–	–	Note	Note

Note Those are only mounted in the 78K0R/KF3-L (μPD78F1027 and 78F1028) and the 78K0R/KG3-L (μPD78F1029 and 78F1030).

(6) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 5-41. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching											
					Port 15				Port 2							
					ANI11 /P153	ANI10 /P152	ANI9 /P151	ANI8 /P150	ANI7 /P27	ANI6 /P26	ANI5 /P25	ANI4 /P24	ANI3 /P23	ANI2 /P22	ANI1 /P21	ANI0 /P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D
Other than the above					Setting prohibited											

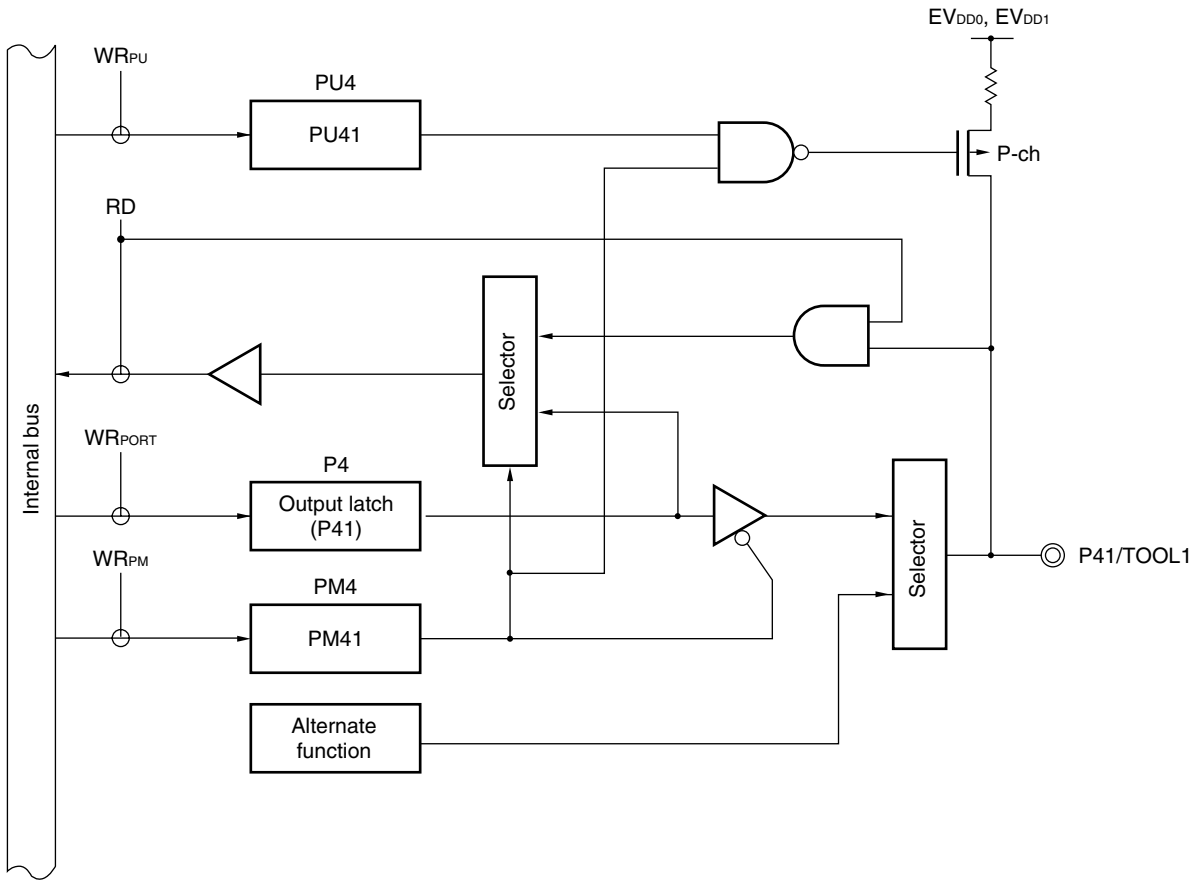
Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 and 15 (PM2, PM15).

2. Do not set the pin that is set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

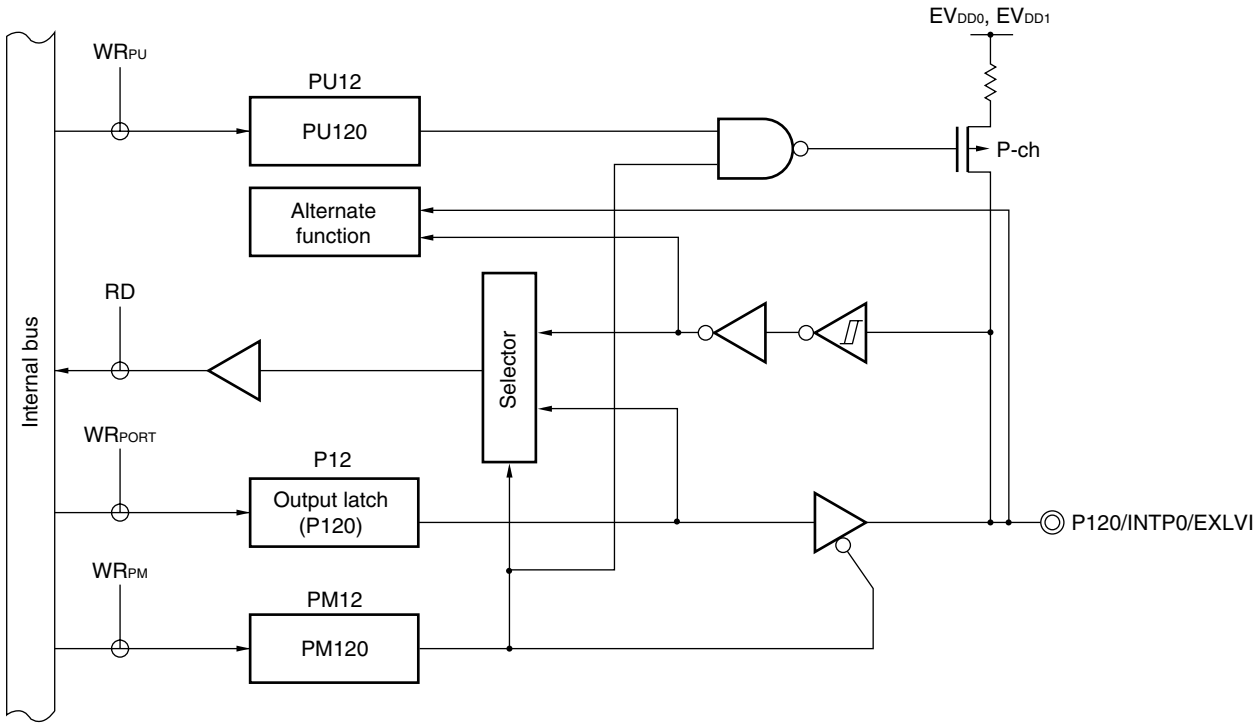
Remark P20/ANI0 to P27/ANI7, P150/ANI8, and P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L

Figure 6-16. Block Diagram of P41



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-42. Block Diagram of P120



P12: Port register 12
PU12: Pull-up resistor option register 12
PM12: Port mode register 12
RD: Read signal
WR××: Write signal

(6) A/D port configuration register (ADPC)

This register switches the P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 6-60. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching															
					Port 15								Port 2							
					ANI15/P157	ANI14/P156	ANI13/P155	ANI12/P154	ANI11/P153	ANI10/P152	ANI9/P151	ANI8/P150	ANI7/P27	ANI6/P26	ANI5/P25	ANI4/P24	ANI3/P23	ANI2/P22	ANI1/P21	ANI0/P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	A	A	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	0	A	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	1	A	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	0	A	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	1	A	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
Other than above					Setting prohibited															

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode registers 2 and 15 (PM2, PM15).

2. Do not set the pin set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 are set as analog inputs in the order of P157/ANI15, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P157/ANI15 as analog inputs, start designing from P157/ANI15.

4. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

Remark P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KF3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P157/ANI15: 78K0R/KG3-L

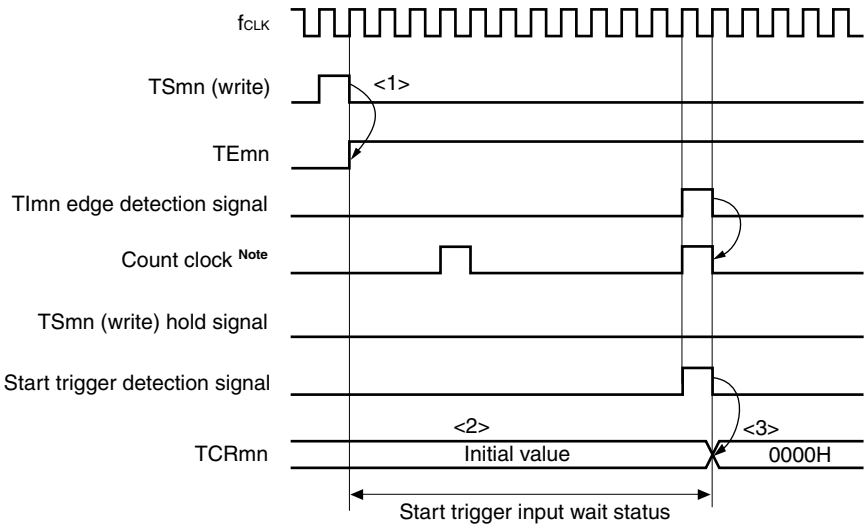
(e) Start timing in capture & one-count mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

<2> Enters the start trigger input wait status, and timer/counter register mn (TCRmn) holds the initial value.

<3> On start trigger detection, 0000H is loaded to the TCRmn register and count starts.

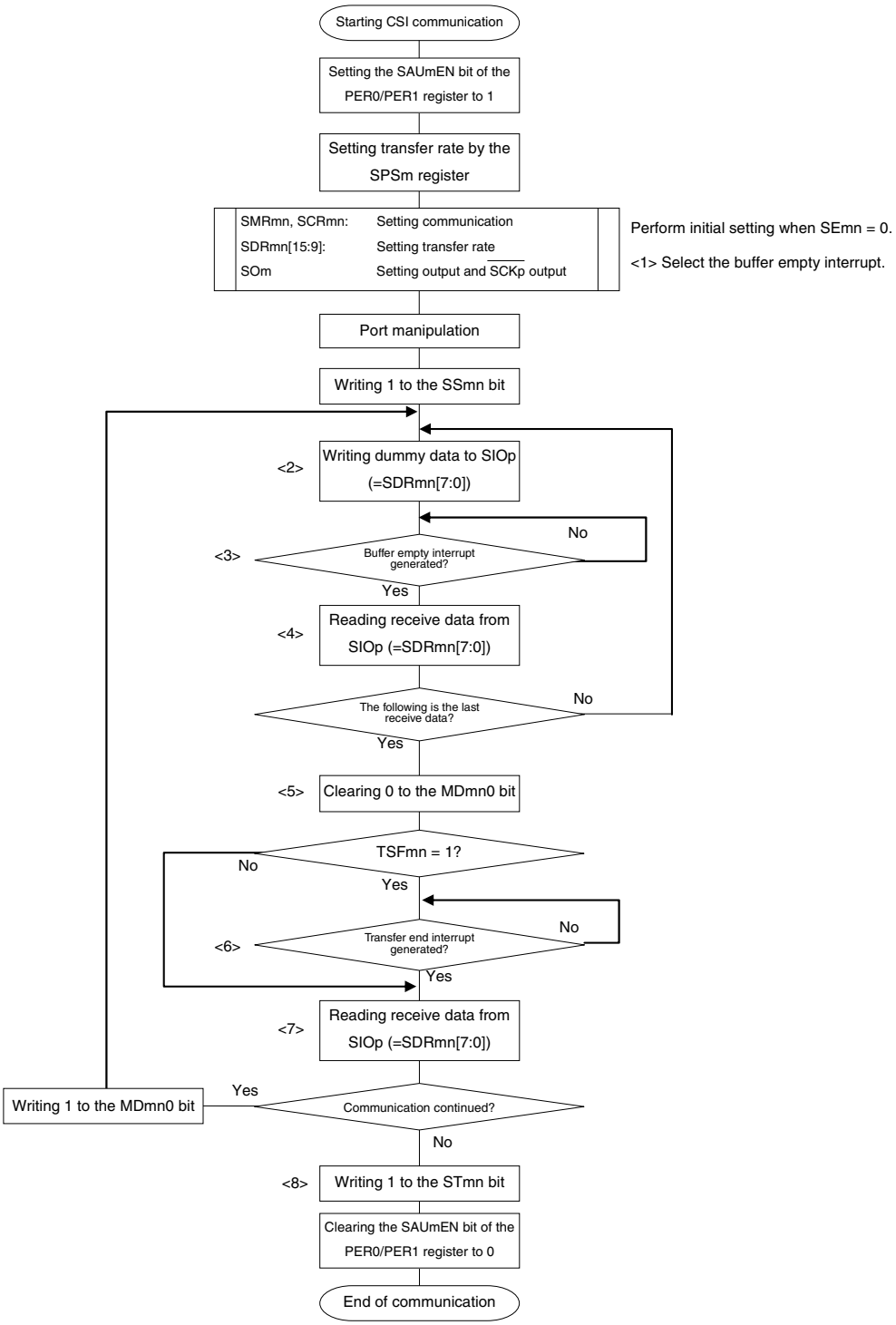
Figure 8-19. Start Timing (In Capture & One-count Mode)



Note When the capture & one-count mode is set, the operation clock (f_{MCK}) is selected as count clock (CCSmn = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (If the TImn pin input signal is used as a start trigger, an error of one count clock occurs.)

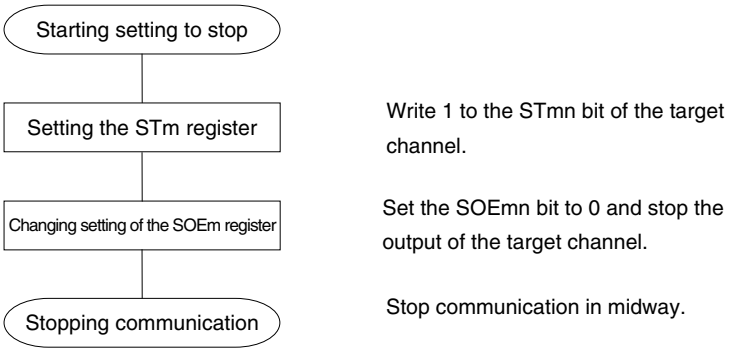
Figure 14-43. Flowchart of Master Reception (in Continuous Reception Mode)



Caution After setting the PER0/PER1 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.

Remark <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-42 Timing Chart of Master Reception (in Continuous Reception Mode)**.

Figure 14-54. Procedure for Stopping Slave Transmission



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set the SOm register (see **Figure 14-55 Procedure for Resuming Slave Transmission**).

14.6 Operation of UART (UART0 to UART4) Communication

This is a start-stop synchronization function using two lines: serial data transmission (TxD) and serial data reception (RxD) lines. By using these two communication lines, each data frame, which consist of a start bit, data, parity bit, and stop bit, is transferred asynchronously (using the internal baud rate) between the microcontroller and the other communication party. Full-duplex UART communication can be performed by using a channel dedicated to transmission (even-numbered channel) and a channel dedicated to reception (odd-numbered channel). The LIN-bus can be implemented by using timer array unit 0 with an external interrupt (INTP0).

[Data transmission/reception]

- Data length of 5, 7, or 8 bits
- Select the MSB/LSB first
- Level setting of transmit/receive data and select of reverse
- Parity bit appending and parity check functions
- Stop bit appending

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt
- Error interrupt in case of framing error, parity error, or overrun error

[Error detection flag]

- Framing error, parity error, or overrun error

The LIN-bus is accepted in UART0 of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L and UART3 of the 78K0R/KF3-L, 78K0R/KG3-L.

[LIN-bus functions]

- Wakeup signal detection
- Sync break field (SBF) detection
- Sync field measurement, baud rate calculation

} Using the external interrupt (INTP0) and timer array unit 0

(1) Multiplication/division data register A (MDAH, MDAL)

The MDAH and MDAL registers set the values that are used for a multiplication or division operation and store the operation result. They set the multiplier and multiplicand data in the multiplication mode, and set the dividend data in the division mode. Furthermore, the operation result (quotient) is stored in the MDAH and MDAL registers in the division mode.

The MDAH and MDAL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 16-2. Format of Multiplication/Division Data Register A (MDAH, MDAL)

Address: FFFF0H, FFFF1H, FFFF2H, FFFF3H After reset: 0000H, 0000H R/W

Symbol FFFF3H FFFF2H

MDAH	MDAH 15	MDAH 14	MDAH 13	MDAH 12	MDAH 11	MDAH 10	MDAH 9	MDAH 8	MDAH 7	MDAH 6	MDAH 5	MDAH 4	MDAH 3	MDAH 2	MDAH 1	MDAH 0

Symbol FFFF1H FFFF0H

MDAL	MDAL 15	MDAL 14	MDAL 13	MDAL 12	MDAL 11	MDAL 10	MDAL 9	MDAL 8	MDAL 7	MDAL 6	MDAL 5	MDAL 4	MDAL 3	MDAL 2	MDAL 1	MDAL 0

Cautions 1. Do not rewrite the MDAH and MDAL registers values during division operation processing (while the multiplication/division control register (MDUC) is 81H). The operation will be executed in this case, but the operation result will be an undefined value.

2. The MDAH and MDAL registers values read during division operation processing (while MDUC is 81H) will not be guaranteed.

The following table shows the functions of the MDAH and MDAL registers during operation execution.

Table 16-2. Functions of MDAH and MDAL Registers During Operation Execution

DIVMODE	Operation Mode	Setting	Operation Result
0	Multiplication mode	MDAH: Multiplier MDAL: Multiplicand	–
1	Division mode	MDAH: Divisor (higher 16 bits) MDAL: Dividend (lower 16 bits)	MDAH: Division result (quotient) Higher 16 bits MDAL: Division result (quotient) Lower 16 bits

Remark DIVMODE: Bit 7 of the multiplication/division control register (MDUC)

17.5.2 Consecutive capturing of A/D conversion results

A flowchart of an example of setting for consecutively capturing A/D conversion results is shown below.

- Consecutive capturing of A/D conversion results.
- DMA channel 1 is used for DMA transfer.
- DMA start source: INTAD
- Interrupt of A/D is specified by IFC13 to IFC10 = 1100B.
- Transfers FFF1EH and FFF1FH (2 bytes) of the 10-bit A/D conversion result register (ADCR) to 512 bytes of FFCE0H to FFEDFH of RAM.

Remark IFC13 to IFC10: Bits 3 to 0 of DMA mode control registers 1 (DMC1)

Table 21-2. Hardware Statuses After Reset Acknowledgment (3/4)

Hardware		Status After Reset Acknowledgment[Note 1]
Serial interface IICA	IICA shift register (IICA)	00H
	IICA status register (IICS)	00H
	IICA flag register (IICF)	00H
	IICA control register 0 (IICCTL0)	00H
	IICA control register 1 (IICCTL1)	00H
	IICA low-level width setting register (IICWL)	FFH
	IICA high-level width setting register (IICWH)	FFH
	Slave address register (SVA)	00H
Multiplier/divider	Multiplication/division data register A (L) (MDAL)	0000H
	Multiplication/division data register A (H) (MDAH)	0000H
	Multiplication/division data register B (L) (MDBL)	0000H
	Multiplication/division data register B (H) (MDBH)	0000H
	Multiplication/division data register C (L) (MDCL)	0000H
	Multiplication/division data register C (H) (MDCH)	0000H
	Multiplication/division control register (MDUC)	00H
Key interrupt	Key return mode register (KRM)	00H
Reset function	Reset control flag register (RESF)	00H[Note 2]
Low-voltage detector	Low-voltage detection register (LVIM)	00H[Note 3]
	Low-voltage detection level select register (LVIS)	0EH[Note 2]
Regulator	Regulator mode control register (RMC)	00H
DMA controller	SFR address registers 0, 1 (DSA0, DSA1)	00H
	RAM address registers 0L, 0H, 1L, 1H (DRA0L, DRA0H, DRA1L, DRA1H)	00H
	Byte count registers 0L, 0H, 1L, 1H (DBC0L, DBC0H, DBC1L, DBC1H)	00H
	Mode control registers 0, 1 (DMC0, DMC1)	00H
	Operation control registers 0, 1 (DRC0, DRC1)	00H

Notes 1. During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

2. These values vary depending on the reset source.

Register \ Reset Source		$\overline{\text{RESET}}$ Input	Reset by POC	Reset by Execution of Illegal Instruction	Reset by WDT	Reset by INIRF	Reset by LVI
RESF	TRAP bit	Cleared (0)	Cleared (0)	Set (1)	Held	Held	Held
	WDRF bit			Held	Set (1)	Held	Held
	INIRF bit			Held	Held	Set (1)	Held
	LVIRF bit			Held	Held	Held	Set (1)
LVIS		Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Cleared (0EH)	Held

3. This value varies depending on the reset source and the option byte.

Remark The special function register (SFR) mounted depend on the product. See **4.2.4 Special function registers (SFRs)** and **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

Table 26-2. Pin Connection

Dedicated Flash Memory Programmer			78K0R/Kx3-L	Connection
Signal Name	I/O	Pin Function	Pin Name	
FLMD0	Output	Mode signal	FLMD0	◎
V_{DD}	I/O	V_{DD} voltage generation/power monitoring	V_{DD}, EV_{DD}, EV_{DD0}, EV_{DD1}, AV_{REF}	◎
GND	–	Ground	V_{SS}, EV_{SS}, EV_{SS0}, EV_{SS1}, AV_{SS}	◎
CLK	Output	Clock output	–	×
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	◎
SI/RxD Notes1, 2	Input	Receive signal	TOOL0	◎
SO/TxD Note2	Output	Transmit signal		
SCK	Output	Transfer clock	–	×

Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

Remark ◎: Be sure to connect the pin.

×: The pin does not have to be connected.

26.4 Connection of Pins on Board

To write the flash memory on-board, connectors that connect the dedicated flash memory programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be handled as described below.

26.4.1 FLMD0 pin

(1) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

(2) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = “0”, default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **26.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(3) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
		1.8 V ≤ V_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			80			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK}+50			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+45	ns
			2.7 V ≤ V_{DD} < 4.0 V			2/f_{MCK}+57	ns
			1.8 V ≤ V_{DD} < 2.7 V			2/f_{MCK}+125	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

4. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10), g: PIM and POM number (g = 3, 7)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of the SMR0n register. n: Channel number (n = 0 to 2))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.6 Supply voltage rise time

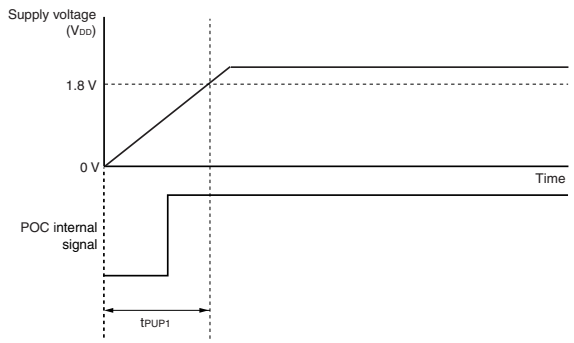
(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (V_{DD}: 0 V → 1.8 V)	t_{PUP1}	LVI default start function stopped is set (LVIOFF (Option Byte) = 1), when $\overline{\text{RESET}}$ input is not used			3.6	ms
Maximum time to rise to 1.8 V (V_{DD} (MIN.))[Note] (releasing $\overline{\text{RESET}}$ input → V_{DD}: 1.8 V)	t_{PUP2}	LVI default start function stopped is set (LVIOFF (Option Byte) = 1), when $\overline{\text{RESET}}$ input is used			1.88	ms

Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

• When the $\overline{\text{RESET}}$ pin input is not used



• When the $\overline{\text{RESET}}$ pin input is used (when external reset is released by the $\overline{\text{RESET}}$ pin, after POC has been released)