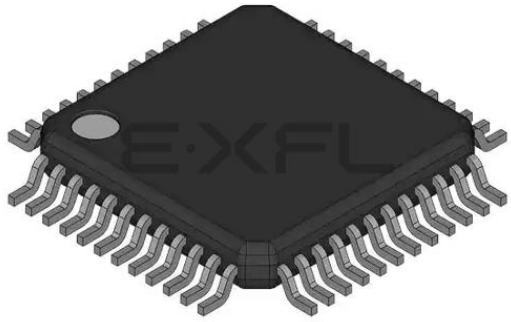
Renesas Electronics America Inc - UPD78F1001GA-HAA-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	41
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1001ga-haa-ax

1.6.2 78K0R/KD3-L

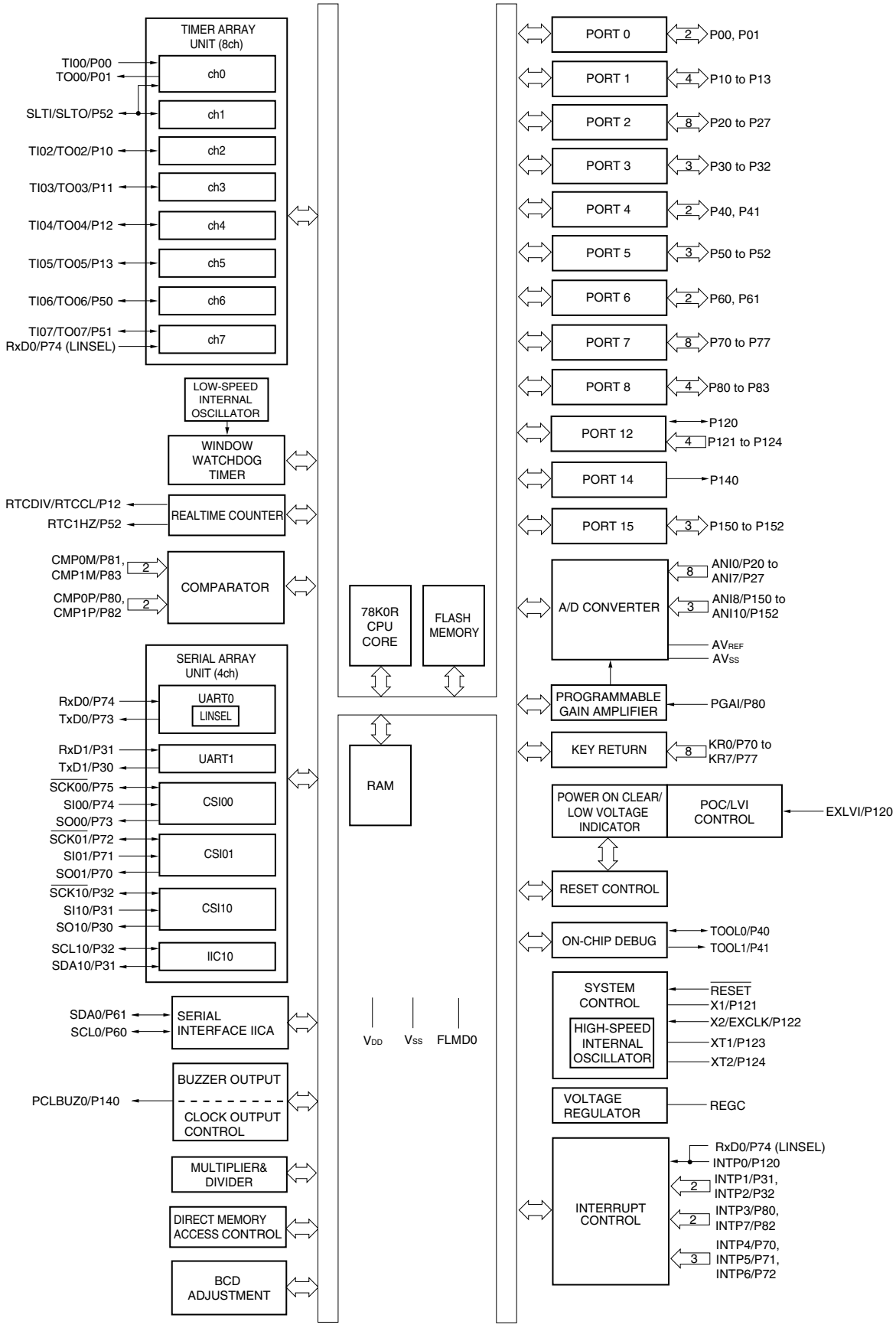
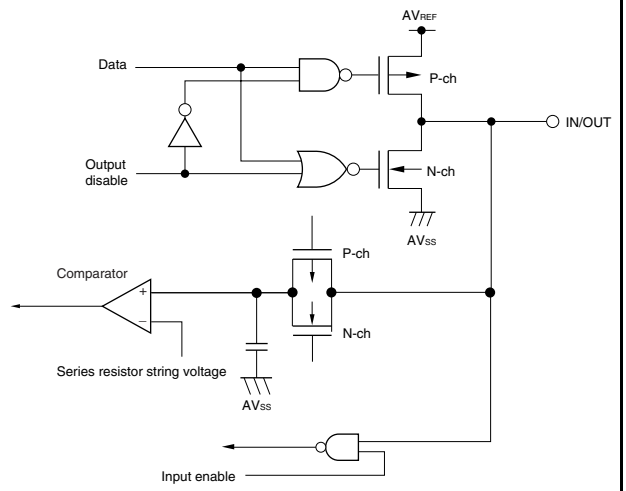
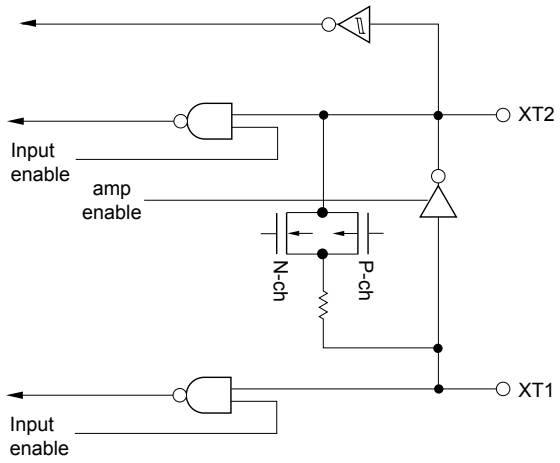


Figure 3-1. Pin I/O Circuit List (2/2)

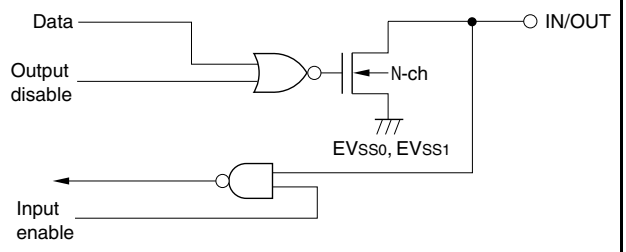
Type 11-G



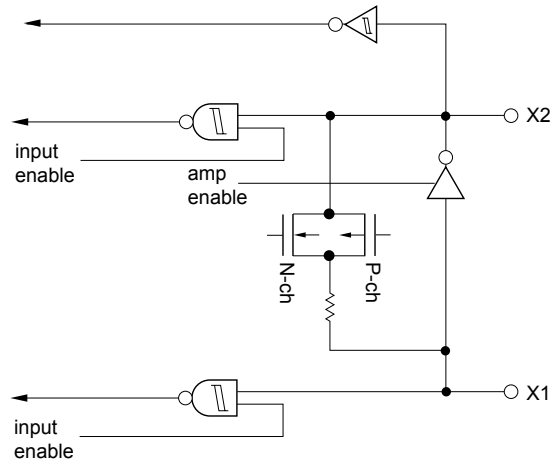
Type 37-B



Type 13-P



Type 37-C



Type 13-R

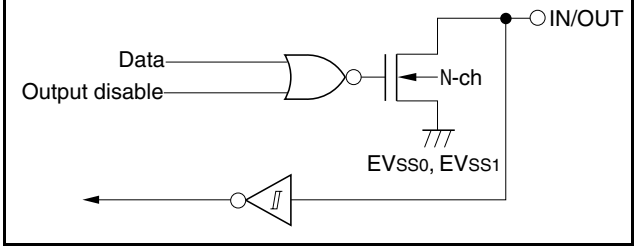
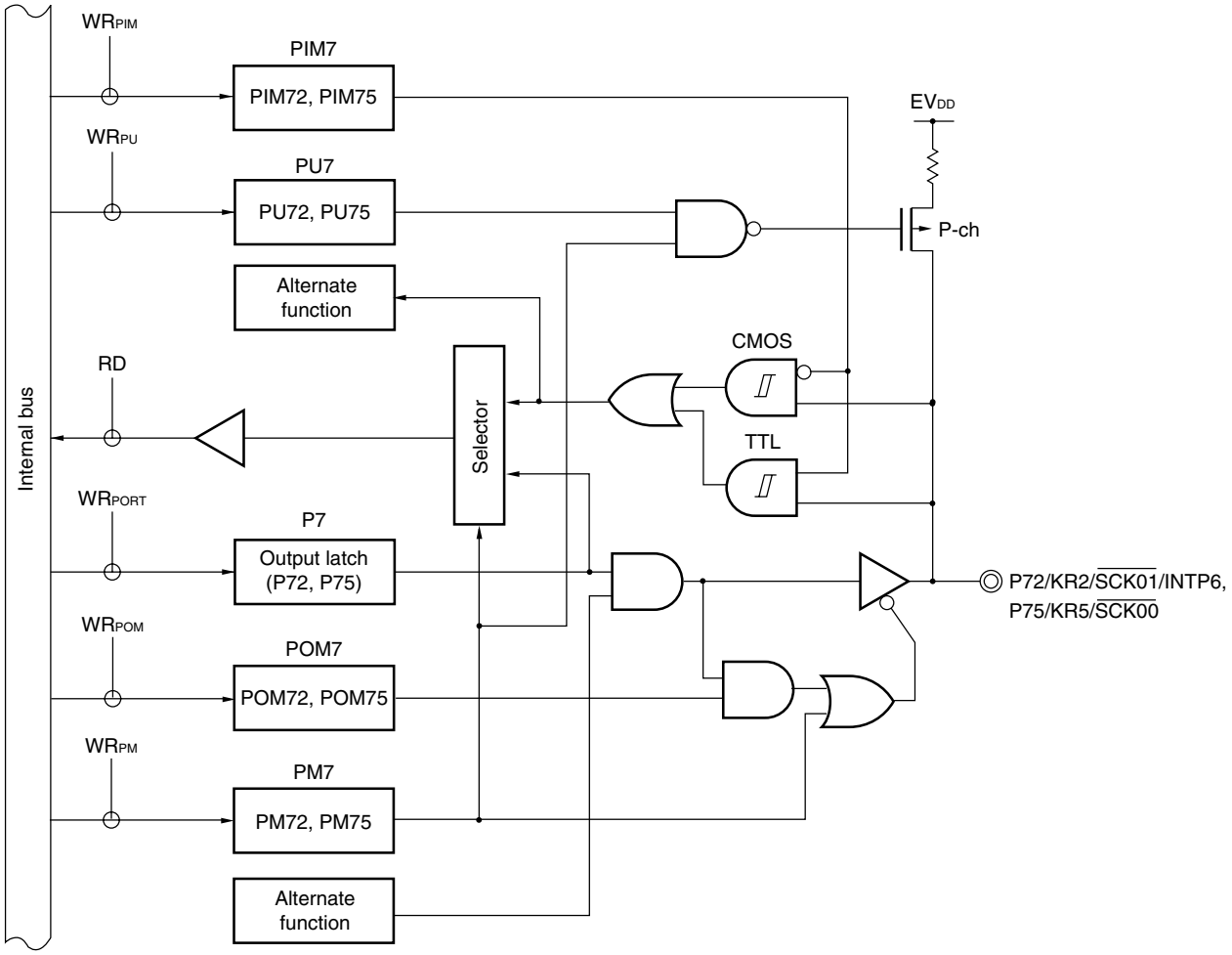


Figure 5-17. Block Diagram of P72 and P75



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
PIM7: Port input mode register 7
POM7: Port output mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

(6) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 5-41. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching											
					Port 15				Port 2							
					ANI11 /P153	ANI10 /P152	ANI9 /P151	ANI8 /P150	ANI7 /P27	ANI6 /P26	ANI5 /P25	ANI4 /P24	ANI3 /P23	ANI2 /P22	ANI1 /P21	ANI0 /P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D
Other than the above					Setting prohibited											

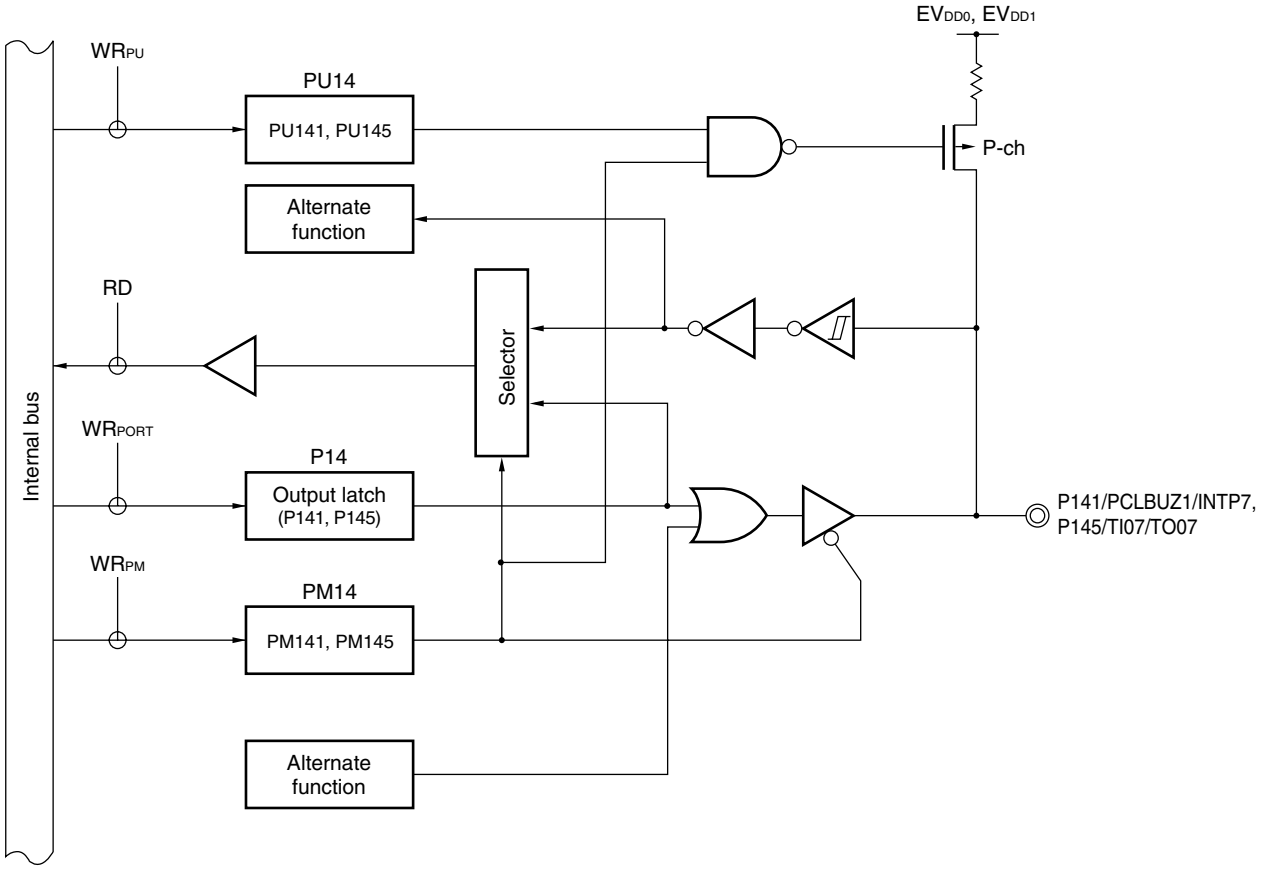
Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 and 15 (PM2, PM15).

2. Do not set the pin that is set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

Remark P20/ANI0 to P27/ANI7, P150/ANI8, and P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L

Figure 6-48. Block Diagram of P141 and P145



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

8.3 Registers Controlling Timer Array Unit

Timer array unit is controlled by the following registers.

- Peripheral enable registers 0, 2 (PER0, PER2) [Note 1]
- Timer clock select register m (TPSm)
- Timer mode register mn (TMRmn)
- Timer status register mn (TSRmn)
- Timer channel enable status register m (TEm)
- Timer channel start register m (TSm)
- Timer channel stop register m (TTm)
- Timer input select register m (TISm)
- Timer output enable register m (TOEm)
- Timer output register m (TOm)
- Timer output level register m (TOLm)
- Timer output mode register m (TOMm)
- Input switch control register (ISC)
- Noise filter enable registers 1, 2 (NFEN1, NFEN2)
- Port mode register (PMxx) [Note 2]
- Port register (Pxx) [Note 2]

Notes 1. Set the PER2 register in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L. Set the PER0 register in the 78K0R/KF3-L and 78K0R/KG3-L.

2. The port mode registers (PMxx) and port registers (Pxx) to be set differ depending on the product. for details, **see 8. 3 (15) Port mode registers 0, 1, 3 to 6, 13, 14 (PM0, PM1, PM3 to PM6, PM13, PM14).**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

(5) Timer channel enable status register m (TEm)

The TEm register is used to enable or stop the timer operation of each channel.

When a bit of timer channel start register m (TSm) is set to 1, the corresponding bit of this register is set to 1.

When a bit of timer channel stop register m (TTm) is set to 1, the corresponding bit of this register is cleared to 0.

The TEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TEmL.

Reset signal generation clears this register to 0000H.

Figure 8-13. Format of Timer Channel Enable Status register m (TEm)

Address: F01B0H, F01B1H After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE0	0	0	0	0	0	0	0	0	TE07	TE06	TE05	TE04	TE03	TE02	TE01	TE00

Address: F01D8H, F01D9H After reset: 0000H R

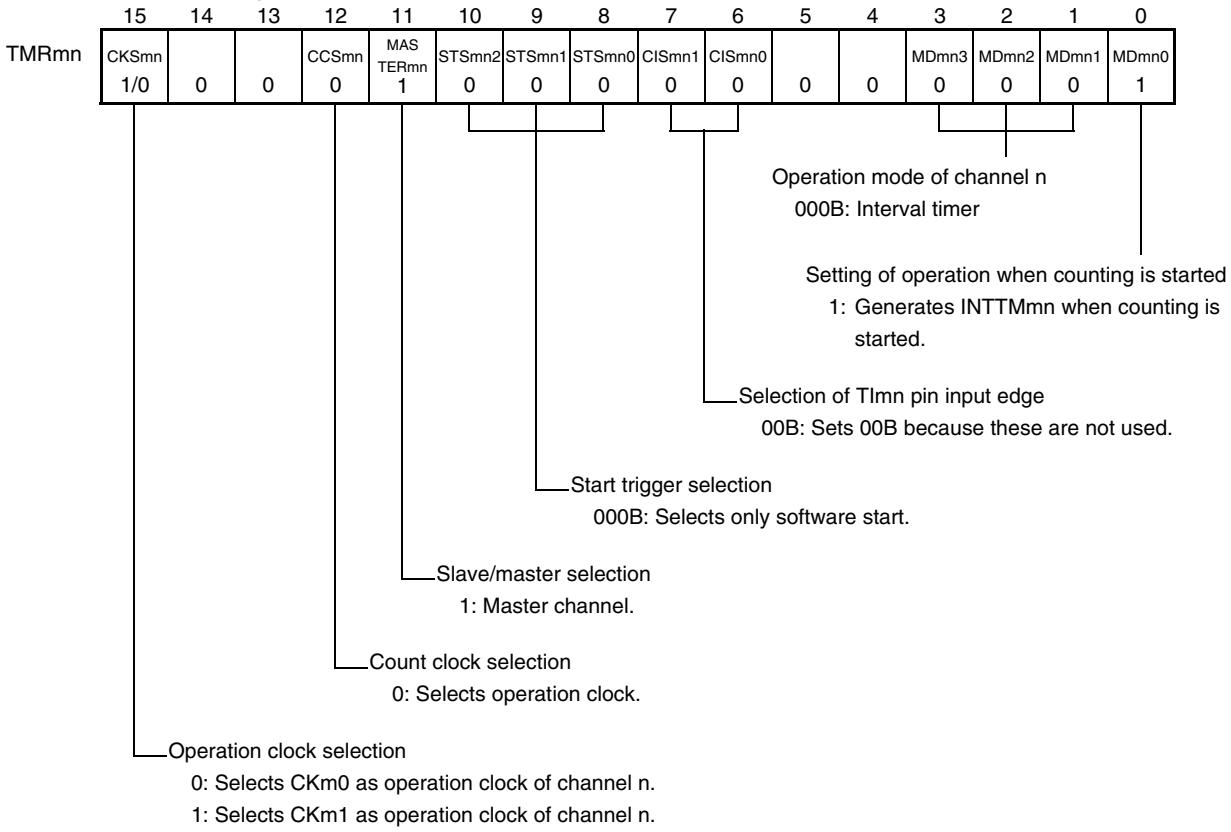
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TE1	0	0	0	0	0	0	0	0	0	0	0	0	TE13	TE12	TE11	TE10

TEmn	Indication of operation enable/stop status of channel n
0	Operation is stopped.
1	Operation is enabled.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-68. Example of Set Contents of Registers When PWM Function (Master Channel) Is Used

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12

Figure 8-70. Operation Procedure When PWM Function Is Used (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	TEmn = 1, TEmp = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn and TMRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers can be changed.	The counter of the master channel loads the TDRmn register value to timer/counter register mn (TCRmn), and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel, the value of the TDRmp register is loaded to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. The TTmn and TTmp bits automatically return to 0 because they are trigger bits.	TEmn, TEmp = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register.	The TOmp pin output level is held by port function.
	When holding the TOmp pin output level is not necessary Switches the port mode register to input mode.	The TOmp pin output level goes into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note]	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

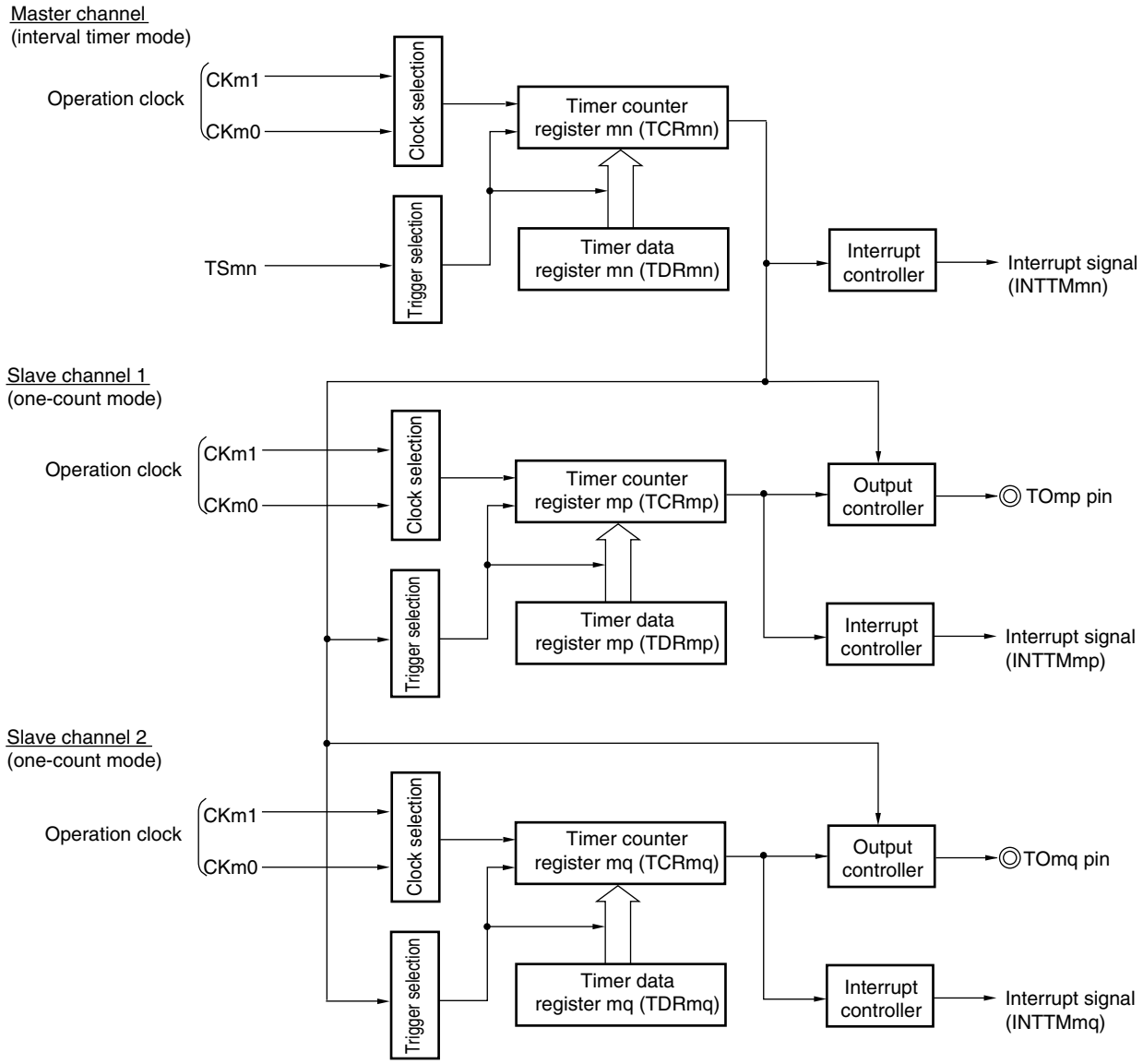
Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: $n < p \leq 7$
When m = 1: $n < p \leq 3$

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-71. Block Diagram of Operation as Multiple PWM Output Function (output two types of PWMs)



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$
When m = 1: $n < p < q \leq 3$
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-72. Example of Basic Timing of Operation as Multiple PWM Output Function (output two types of PWMs) (2/2)

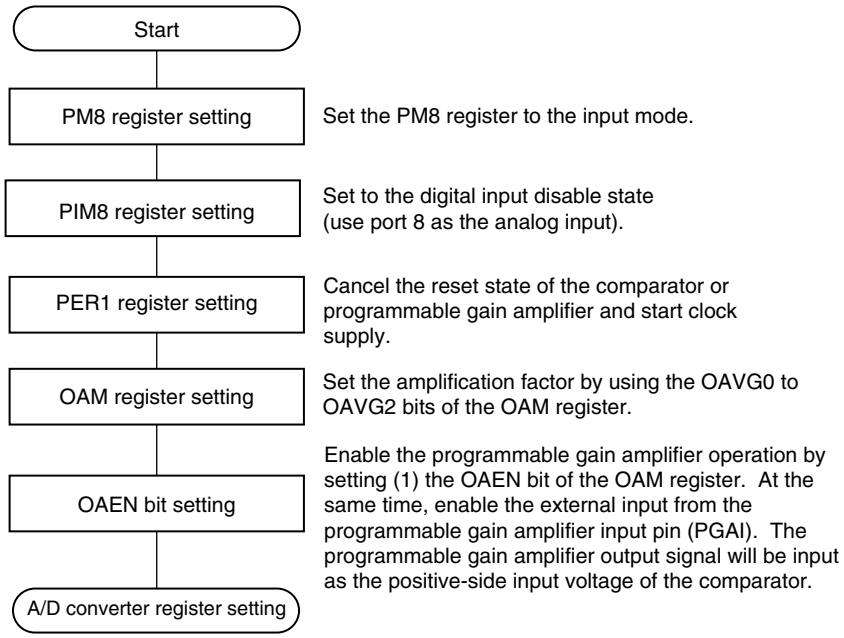
Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$
When m = 1: $n < p < q \leq 3$
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, channel 1 in the 78K0R/KC3-L (40-pin) can not used as slave channel.

2. TSmn, TSmp, TSmq: Bit n, p, q of timer channel start register m (TSm)
TEmn, TEmp, TEmq: Bit n, p, q of timer channel enable status register m (TEm)
TCRmn, TCRmp, TCRmq: Timer/counter registers mn, mp, mq (TCRmn, TCRmp, TCRmq)
TDRmn, TDRmp, TDRmq: Timer data registers mn, mp, mq (TDRmn, TDRmp, TDRmq)
TOmn, TOmp, TOmq: TOmn, TOmp, and TOmq pins output signal

Perform the following settings before selecting the programmable gain amplifier output signal as the analog input by using the analog input channel specification register (ADS) of the A/D converter (refer to **13.4.1 Basic operations of A/D converter**).

Figure 10-13. Using the Programmable Gain Amplifier Output Voltage as the A/D Converter Analog Input



Caution Ensure that 3 μs elapses before A/D conversion starts after setting the OAEN bit.

Remark n = 0, 1

13.4 A/D Converter Operations

13.4.1 Basic operations of A/D converter

<1> Set bit 5 (ADCEN) of peripheral enable register 0 (PER0) to 1 to start the supply of the input clock to the A/D converter.

<2> Set the A/D conversion time by using bits 5 to 1 (FR2 to FR0, LV1, and LV0) of the A/D converter mode register (ADM), and set the operation mode by using bit 6 (ADMD) of the ADM register.

<3> Set bit 0 (ADCE) of the ADM register to 1 to start the operation of the A/D voltage comparator.

<4> Set the channels for A/D conversion to analog input by using the A/D port configuration register (ADPC) and set to input mode by using the port mode registers (PM2, PM15, and PM8).

<5> Set the programmable gain amplifier operation to set the programmable gain amplifier output (PGAI pin) for the analog input channel (refer to **10.4.1 Starting comparator and programmable gain amplifier operation**).

<6> Select one channel for A/D conversion using the analog input channel specification register (ADS).

<7> Start the conversion operation by setting bit 7 (ADCS) of the ADM register to 1.
(<8> to <14> are operations performed by hardware.)

<8> The voltage input to the selected analog input channel is sampled by the sample & hold circuit.

<9> When sampling has been done for a certain time, the sample & hold circuit is placed in the hold state and the sampled voltage is held until the A/D conversion operation has ended.

<10> Bit 9 of the successive approximation register (SAR) is set. The series resistor string voltage tap is set to (1/2) AV_{REF} by the tap selector.

<11> The voltage difference between the series resistor string voltage tap and sampled voltage is compared by the voltage comparator. If the analog input is greater than (1/2) AV_{REF}, the MSB bit of the SAR register remains set to 1. If the analog input is smaller than (1/2) AV_{REF}, the MSB bit is reset to 0.

<12> Next, bit 8 of the SAR register is automatically set to 1, and the operation proceeds to the next comparison. The series resistor string voltage tap is selected according to the preset value of bit 9, as described below.

- Bit 9 = 1: (3/4) AV_{REF}
- Bit 9 = 0: (1/4) AV_{REF}

The voltage tap and sampled voltage are compared and bit 8 of the SAR register is manipulated as follows.

- Sampled voltage ≥ Voltage tap: Bit 8 = 1
- Sampled voltage < Voltage tap: Bit 8 = 0

<13> Comparison is continued in this way up to bit 0 of the SAR register.

<14> Upon completion of the comparison of 10 bits, an effective digital result value remains in the SAR register, and the result value is transferred to the A/D conversion result register (ADCR, ADCRH) and then latched.
At the same time, the A/D conversion end interrupt request (INTAD) can also be generated.

<15> Repeat steps <8> to <14>, until the ADCS bit is cleared to 0.
To stop the A/D converter, clear the ADCS bit to 0.
To restart A/D conversion from the status of ADCE = 1, start from <7>. To start A/D conversion again when ADCE = 0, set the ADCE bit to 1, wait for 1 μs or longer, and start <7>. To change a channel of A/D conversion, start from <6>.

Caution Make sure the period of <3> to <7> is 1 μs or more.

Remark Two types of the A/D conversion result registers are available.
- ADCR register (16 bits): Store 10-bit A/D conversion value
- ADCRH register (8 bits): Store 8-bit A/D conversion value

Figure 14-28. Example of Contents of Registers for Master Transmission of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOEm	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 0/1 Note 2	SOEm1 0/1 Note 1	SOEm0 0/1

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSm	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

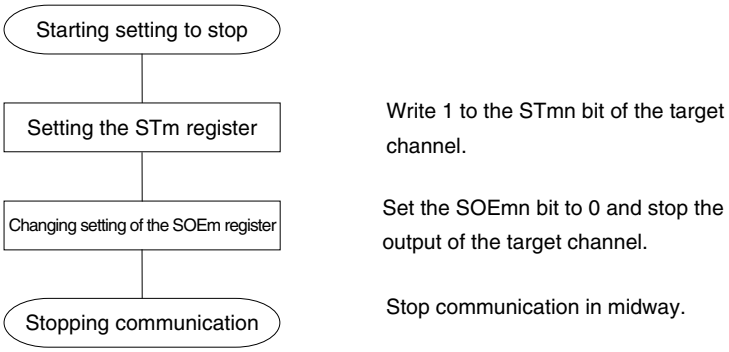
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

2. □: Setting is fixed in the CSI master transmission mode, ■: Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

Figure 14-54. Procedure for Stopping Slave Transmission



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set the SOm register (see **Figure 14-55 Procedure for Resuming Slave Transmission**).

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (1/4)

Address: F0230H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICCTL0	IICE	LREL	WREL	SPIE	WTIM	ACKE	STT	SPT

IICE	I^2C operation enable
0	Stop operation. Reset the IICA status register (IICS)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCL0 and SDA0 lines are at high level.	
Condition for clearing (IICE = 0)	Condition for setting (IICE = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL[Notes 2, 3]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL0 and SDA0 lines are set to high impedance. The following flags of IICA control register 0 (IICCTL0) and the IICA status register (IICS) are cleared to 0. • STT • SPT • MSTS • EXC • COI • TRC • ACKD • STD
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL = 0)	Condition for setting (LREL = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL[Notes 2, 3]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When the WREL bit is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC = 1), the SDA0 line goes into the high impedance state (TRC = 0).	
Condition for clearing (WREL = 0)	Condition for setting (WREL = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICA status register (IICS), the STCF and IICBSY bits of the IICA flag register (IICF), and the CLD and DAD bits of IICA control register 1 (IICCTL1) are reset.

2. The signal of this bit is invalid while IICE0 is 0.

3. When the LREL and WREL bits are read, 0 is always read.

Caution If the operation of I^2C is enabled (IICE = 1) when the SCL0 line is high level, the SDA0 line is low level, and the digital filter is turned on (DFC bit of IICCTL1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICE = 1).

CHAPTER 18 INTERRUPT FUNCTIONS

The number of interrupt sources differs, depending on the product.

<In case of the 78K0R/KC3-L, KD3-L, KE3-L>

		78K0R/KC3-L (40-pin)	78K0R/KC3-L (44-pin)	78K0R/KC3-L (48-pin)	78K0R/KD3-L	78K0R/KE3-L
Maskable interrupts	External	8	9	9	9	9
	Internal	22	24	25	25	25

<In case of the 78K0R/KF3-L, KG3-L>

		78K0R/KF3-L		78K0R/KG3-L	
		(μPD78F10xx : xx = 10, 11, 12)	(μPD78F10xx : xx = 27, 28)	(μPD78F10xx : xx = 13, 14)	(μPD78F10xx : xx = 29, 30)
Maskable interrupts	External	13			
	Internal	33	35	33	35

18.1 Interrupt Function Types

The following two types of interrupt functions are used.

(1) Maskable interrupts

These interrupts undergo mask control. Maskable interrupts can be divided into four priority groups by setting the priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H).

Multiple interrupt servicing can be applied to low-priority interrupts when high-priority interrupts are generated. If two or more interrupt requests, each having the same priority, are simultaneously generated, then they are processed according to the priority of vectored interrupt servicing. For the priority order, see **Table 18-1**.

A standby release signal is generated and STOP and HALT modes are released.

External interrupt requests and internal interrupt requests are provided as maskable interrupts.

(2) Software interrupt

This is a vectored interrupt generated by executing the BRK instruction. It is acknowledged even when interrupts are disabled. The software interrupt does not undergo interrupt priority control.

18.2 Interrupt Sources and Configuration

Interrupt sources include maskable interrupts and software interrupts. In addition, they also have up to five reset sources (see **Table 18-1**). The vector codes that store the program start address when branching due to the generation of a reset or various interrupt requests are two bytes each, so interrupts jump to a 64 K address of 00000H to 0FFFFH.

Figure 18-2. Format of Interrupt Request Flag Registers (IF0L, IF0H, IF1L, IF1H, IF2L) (2/2)

XXIFX	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Cautions 1. Be sure to clear bit 0 of the IF0H register, bits 4 and 5 of the IF1H register (in case of 78K0R/KC3-L (40-pin), bits 1, 2, 4, and 5), and bits 5 to 7 of the IF2L register (in case of 78K0R/KC3-L (40-pin), bits 4 to 7) to 0.

2. When operating a timer, serial interface, or A/D converter after standby release, operate it once after clearing the interrupt request flag. An interrupt request flag may be set by noise.

3. When manipulating a flag of the interrupt request flag register, use a 1-bit memory manipulation instruction (CLR1). When describing in C language, use a bit manipulation instruction such as "IF0L.0 = 0;" or "_asm("clr1 IF0L, 0");" because the compiled assembler must be a 1-bit memory manipulation instruction (CLR1).

If a program is described in C language using an 8-bit memory manipulation instruction such as "IF0L &= 0xfe;" and compiled, it becomes the assembler of three instructions.

```
mov a, IF0L
and a, #0FEH
mov IF0L, a
```

In this case, even if the request flag of another bit of the same interrupt request flag register (IF0L) is set to 1 at the timing between "mov a, IF0L" and "mov IF0L, a", the flag is cleared to 0 at "mov IF0L, a". Therefore, care must be exercised when using an 8-bit memory manipulation instruction in C language.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.2 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS}		−0.5 to + 0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to + 3.6 and −0.3 to V_{DD} + 0.3 Note 2	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120 to P124, P141, EXCLK, $\overline{\text{RESET}}$, FLMD0	−0.3 to EV_{DD} + 0.3 and −0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P80 to P83, P150 to P153	−0.3 to AV_{REF} + 0.3 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P60, P61, P70 to P77, P120, P140, P141	−0.3 to EV_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27, P80 to P83, P150 to P153	−0.3 to AV_{REF} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI11, PGAI, CMP0M, CMP0P, CMP1M, CMP1P	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

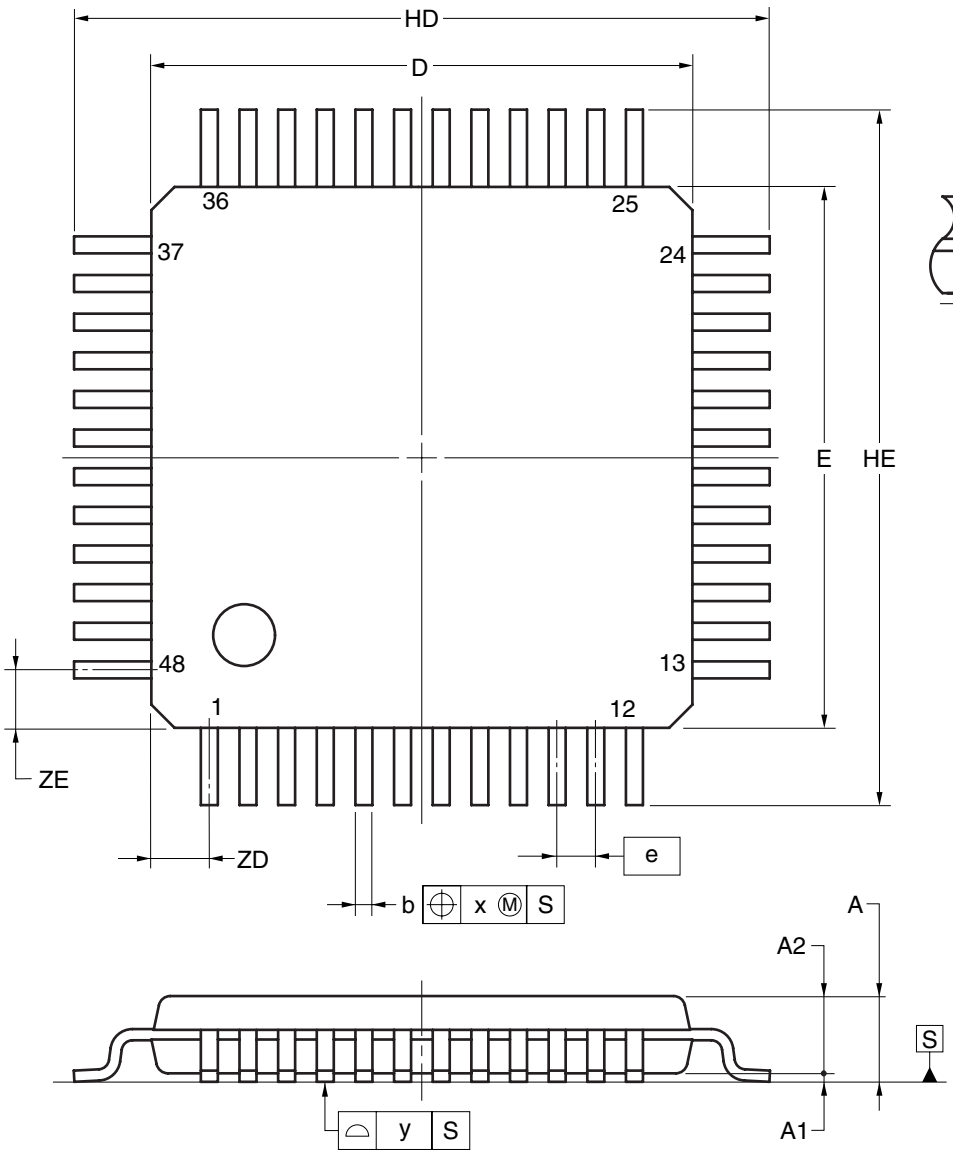
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

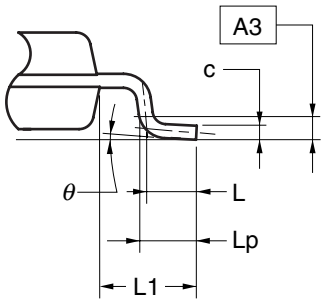
32.3 78K0R/KC3-L (48-pin products)

μPD78F1001GA-HAA-AX, 78F1002GA-HAA-AX, 78F1003GA-HAA-AX

48-PIN PLASTIC TQFP (FINE PITCH) (7x7)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-HAA

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.