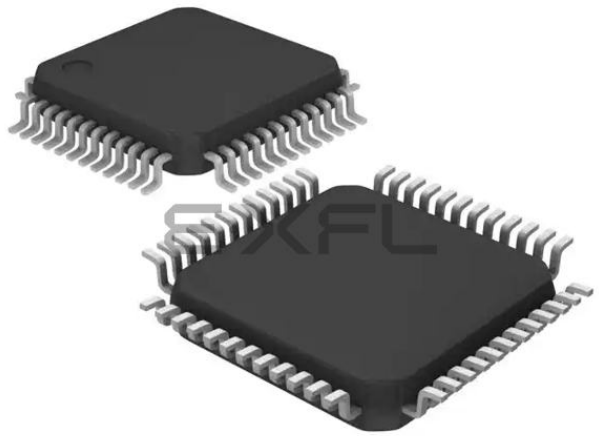
Renesas Electronics America Inc - UPD78F1002GA-HAA-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1002ga-haa-ax

5.2.2 Port 1

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P10/TI02/TO02	√		√	√	√
P11/TO00/TI03/TO03	√		√	√	√
P12/TI04/TO04/RTCDIV/RTCCL	P12/TI04/TO04Note 1	√	√	√	√
P13/TI05/TO05	√		√	√	√
P14/TI06/TO06	–Note 2		–Note 2	–Note 2	√
P15/TI07/TO07	–Note 2		–Note 2	–Note 2	√
P16	–		–	–	√
P17	–		–	–	√

Notes 1. 40-pin product of the 78K0R/KC3-L does not have a RTCDIV/RTCCL pin.

2. TI06/TO06 and TI07/TO07 are shared with P50 and P51, respectively, in products other than the 78K0R/KE3-L.

Remark √: Mounted

Port 1 is an I/O port with an output latch. Port 1 can be set to the input mode or output mode in 1-bit units using port mode register 1 (PM1). When the P10 to P17 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 1 (PU1).

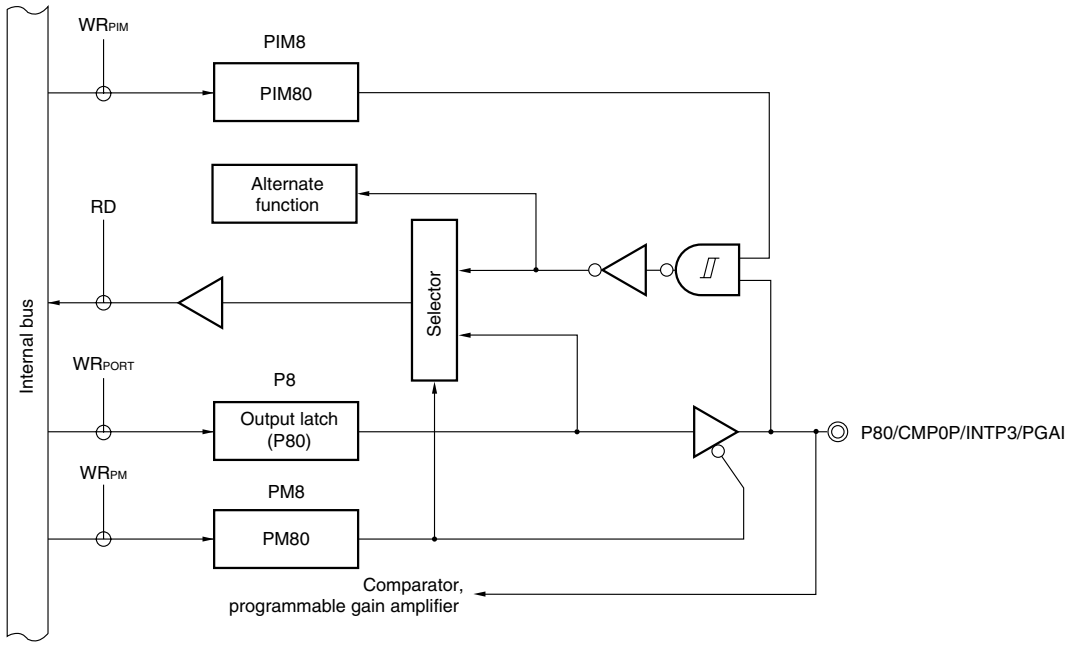
This port can also be used for timer I/O and real-time counter clock output.

Reset signal generation sets port 1 to input mode.

Figures 5-3 and 5-4 show block diagrams of port 1.

Caution To use P10/TI02/TO02, P11/TI03/TO03, P12/TI04/TO04/RTCDIV/RTCCL, P13/TI05/TO05, P14/TI06/TO06, or P15/TI07/TO07 as a general-purpose port, set bits 2 to 7 (TO02 to TO07) of timer output register 0 (TO0) and bits 2 to 7 (TOE02 to TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

Figure 5-19. Block Diagram of P80



P8: Port register 8
PM8: Port mode register 8
PIM8: Port input mode register 8
RD: Read signal
WR××: Write signal

(6) A/D port configuration register (ADPC)

This register switches the ANI0/P20 to ANI7/P27 and ANI8/P150 to ANI11/P153 pins to digital I/O of port or analog input of A/D converter.

The ADPC register can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets this register to 10H.

Figure 5-41. Format of A/D Port Configuration Register (ADPC)

Address: F0017H After reset: 10H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC	0	0	0	ADPC4	ADPC3	ADPC2	ADPC1	ADPC0

ADPC4	ADPC3	ADPC2	ADPC1	ADPC0	Analog input (A)/digital I/O (D) switching											
					Port 15				Port 2							
					ANI11 /P153	ANI10 /P152	ANI9 /P151	ANI8 /P150	ANI7 /P27	ANI6 /P26	ANI5 /P25	ANI4 /P24	ANI3 /P23	ANI2 /P22	ANI1 /P21	ANI0 /P20
0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	A
0	0	0	0	1	A	A	A	A	A	A	A	A	A	A	A	D
0	0	0	1	0	A	A	A	A	A	A	A	A	A	A	D	D
0	0	0	1	1	A	A	A	A	A	A	A	A	A	D	D	D
0	0	1	0	0	A	A	A	A	A	A	A	A	D	D	D	D
0	0	1	0	1	A	A	A	A	A	A	A	D	D	D	D	D
0	0	1	1	0	A	A	A	A	A	A	D	D	D	D	D	D
0	0	1	1	1	A	A	A	A	A	D	D	D	D	D	D	D
0	1	0	0	0	A	A	A	A	D	D	D	D	D	D	D	D
0	1	0	0	1	A	A	A	D	D	D	D	D	D	D	D	D
0	1	0	1	0	A	A	D	D	D	D	D	D	D	D	D	D
0	1	0	1	1	A	D	D	D	D	D	D	D	D	D	D	D
1	0	0	0	0	D	D	D	D	D	D	D	D	D	D	D	D
Other than the above					Setting prohibited											

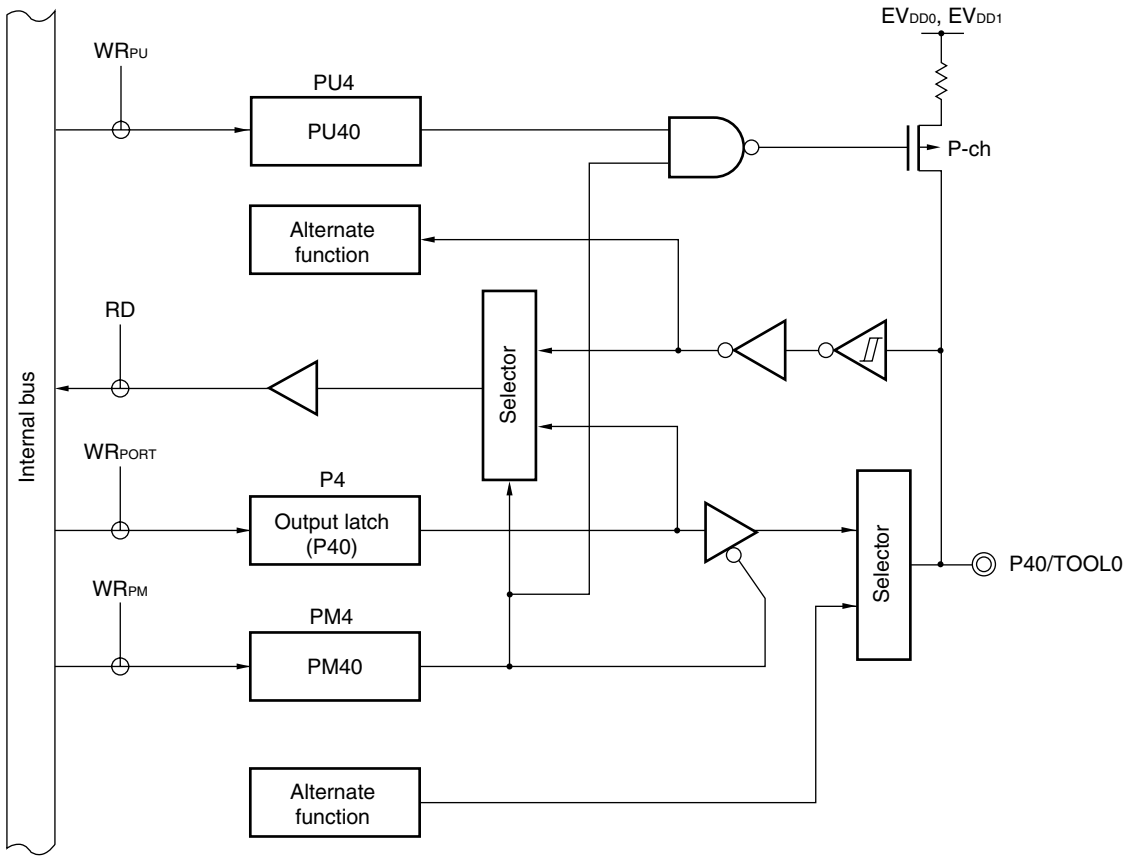
Cautions 1. Set a channel to be used for A/D conversion in the input mode by using port mode register 2 and 15 (PM2, PM15).

2. Do not set the pin that is set by the ADPC register as digital I/O by the analog input channel specification register (ADS).

3. Be sure to first set the ADCEN bit of peripheral enable register 0 (PER0) to 1 when setting up the ADPC register. If ADCEN = 0, writing to the ADPC register is ignored and specified values are returned to the initial values.

Remark P20/ANI0 to P27/ANI7, P150/ANI8, and P151/ANI9: 78K0R/KC3-L (40-pin, 44-pin)
P20/ANI0 to P27/ANI7, P150/ANI8 to P152/ANI10: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
P20/ANI0 to P27/ANI7, P150/ANI8 to P153/ANI11: 78K0R/KE3-L

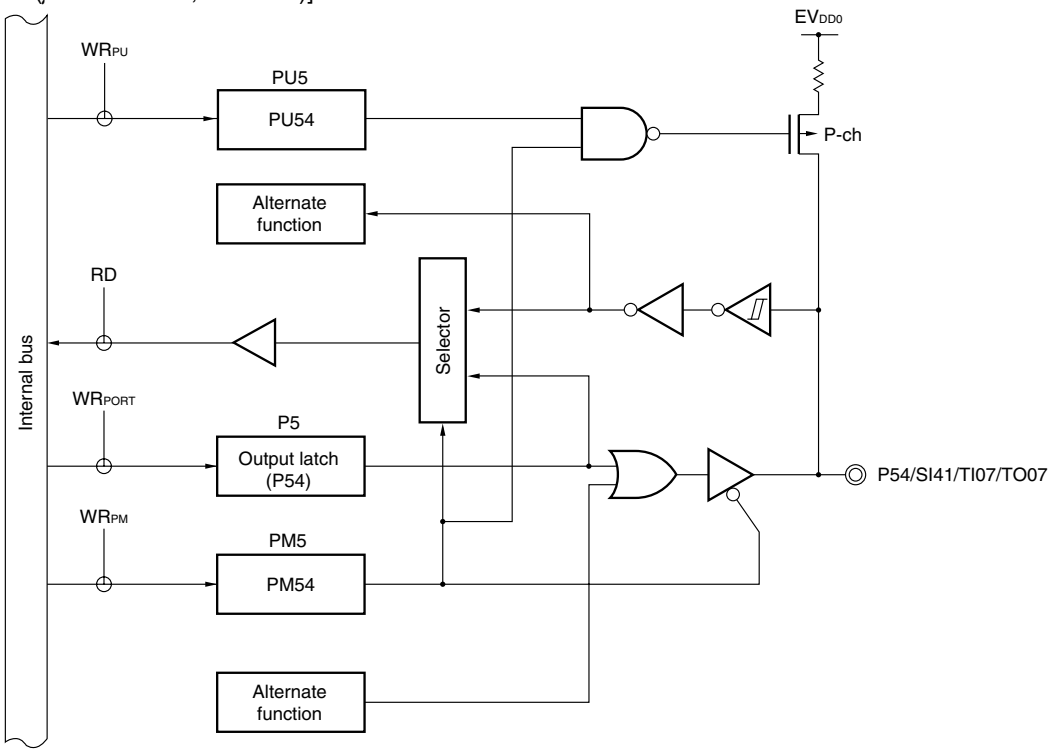
Figure 6-15. Block Diagram of P40



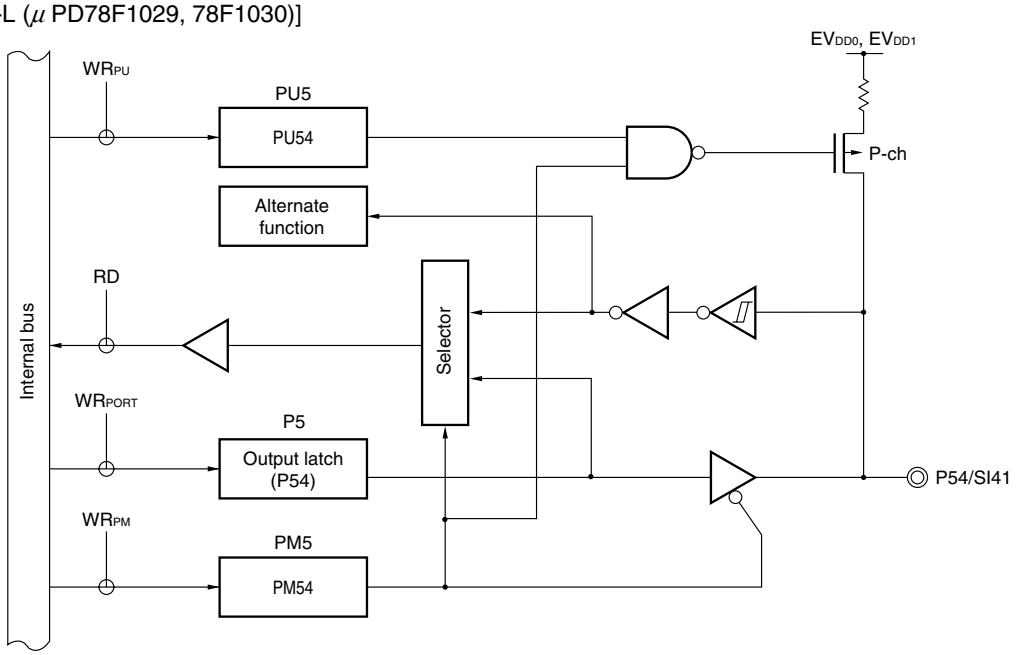
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-30. Block Diagram of P54

[78K0R/KF3-L (μPD78F1027, 78F1028)]

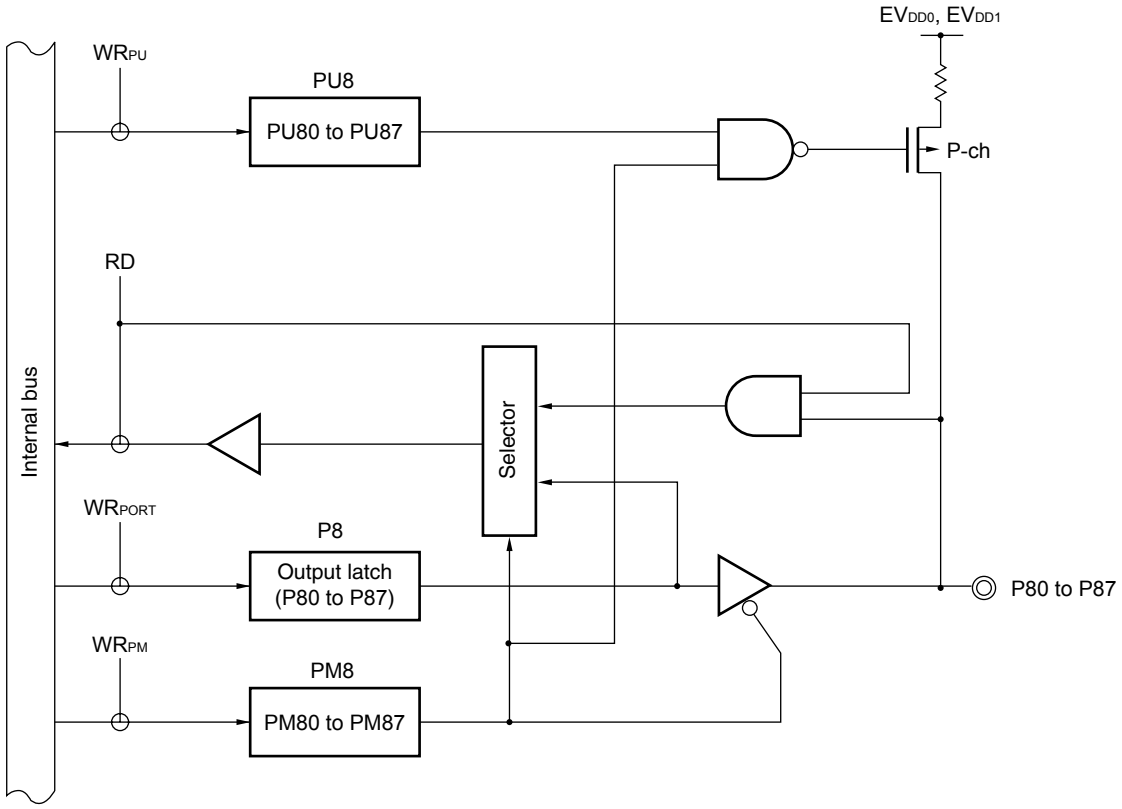


[78K0R/KG3-L (μPD78F1029, 78F1030)]



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

Figure 6-38. Block Diagram of P80 to P87



P8: Port register 8
PU8: Pull-up resistor option register 8
PM8: Port mode register 8
RD: Read signal
WR××: Write signal

6.2.12 Port 11

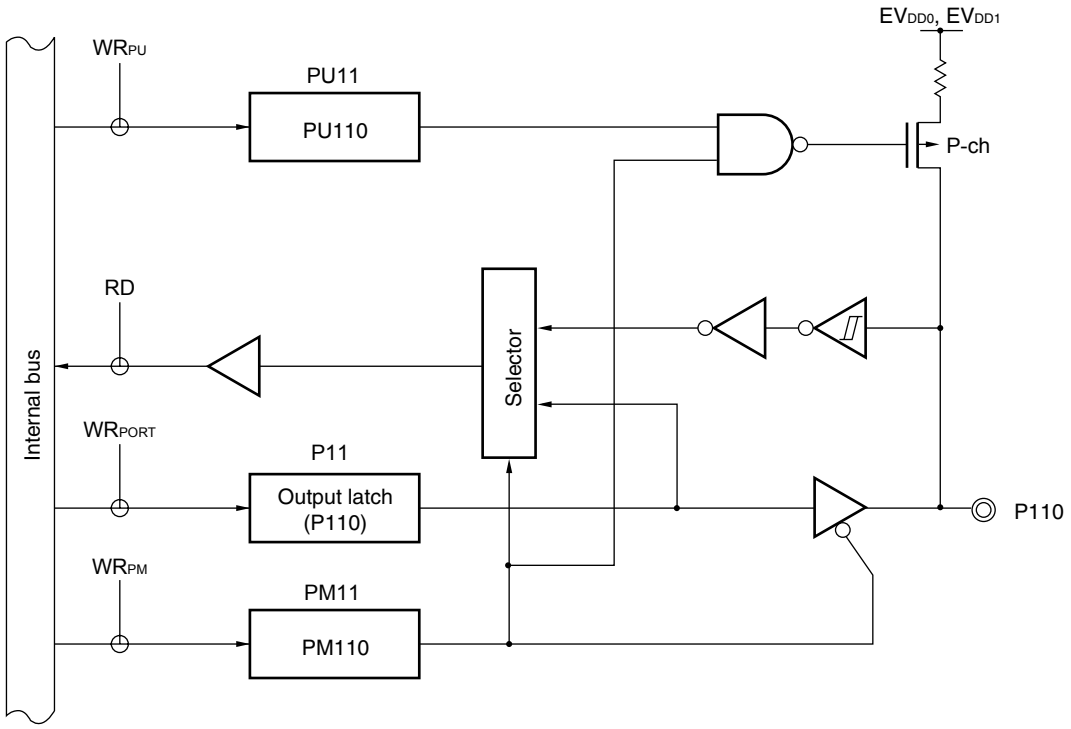
	78K0R/KF3-L (μPD78F10xx: xx = 10 to 12, 27,28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P110	√	√
P111	√	√

Port 11 is an I/O port with an output latch. Port 11 can be set to the input mode or output mode in 1-bit units using port mode register 11 (PM11). When the P110 and P111 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 11 (PU11).

Reset signal generation sets port 11 to input mode.

Figures 6-40 and 6-41 show a block diagram of port 11.

Figure 6-40. Block Diagram of P110



P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
RD: Read signal
WR××: Write signal

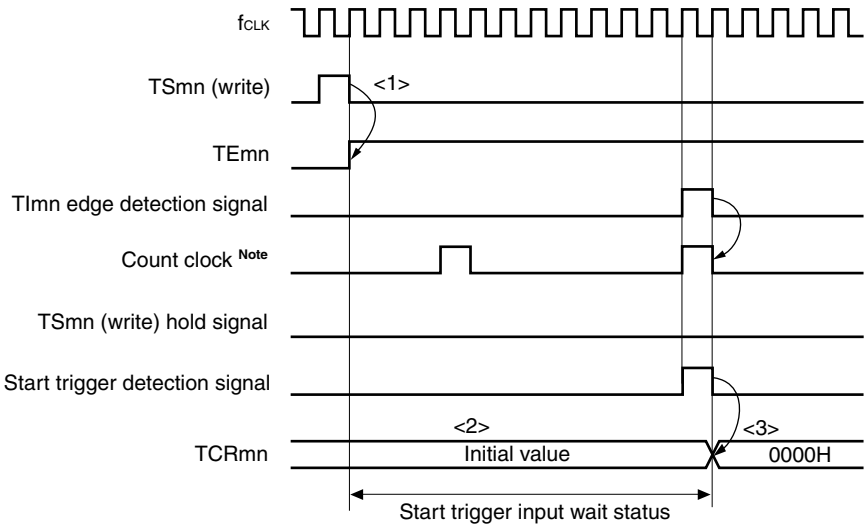
(e) Start timing in capture & one-count mode

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

<2> Enters the start trigger input wait status, and timer/counter register mn (TCRmn) holds the initial value.

<3> On start trigger detection, 0000H is loaded to the TCRmn register and count starts.

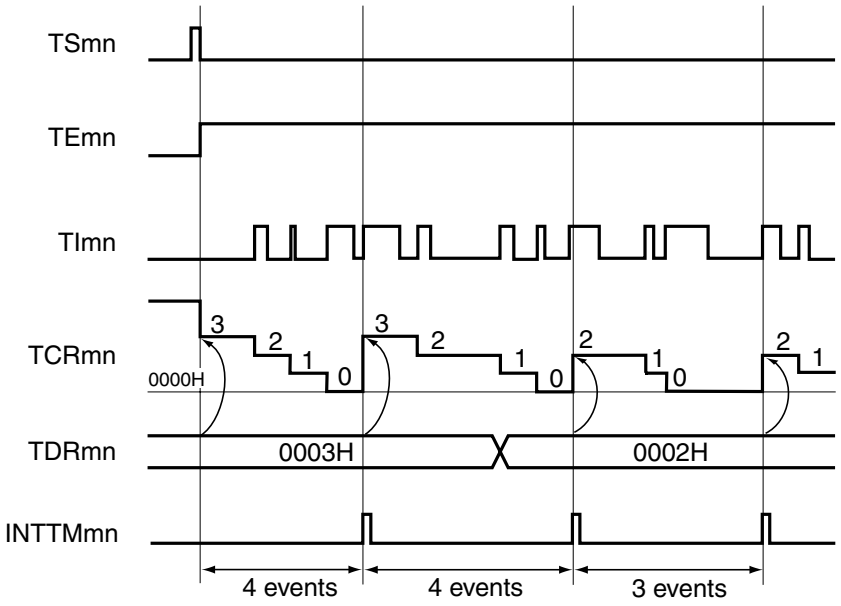
Figure 8-19. Start Timing (In Capture & One-count Mode)



Note When the capture & one-count mode is set, the operation clock (f_{MCK}) is selected as count clock (CCSmn = 0).

Caution An input signal sampling error is generated since operation starts upon start trigger detection (If the TImn pin input signal is used as a start trigger, an error of one count clock occurs.)

Figure 8-46. Example of Basic Timing of Operation as External Event Counter



Remarks 1. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

78K0R/KC3-L (40-pin): mn = 02 to 07

78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07

78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07

78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

2. TSmn: Bit n of timer channel start register m (TSm)

TEmn: Bit n of timer channel enable status register m (TEm)

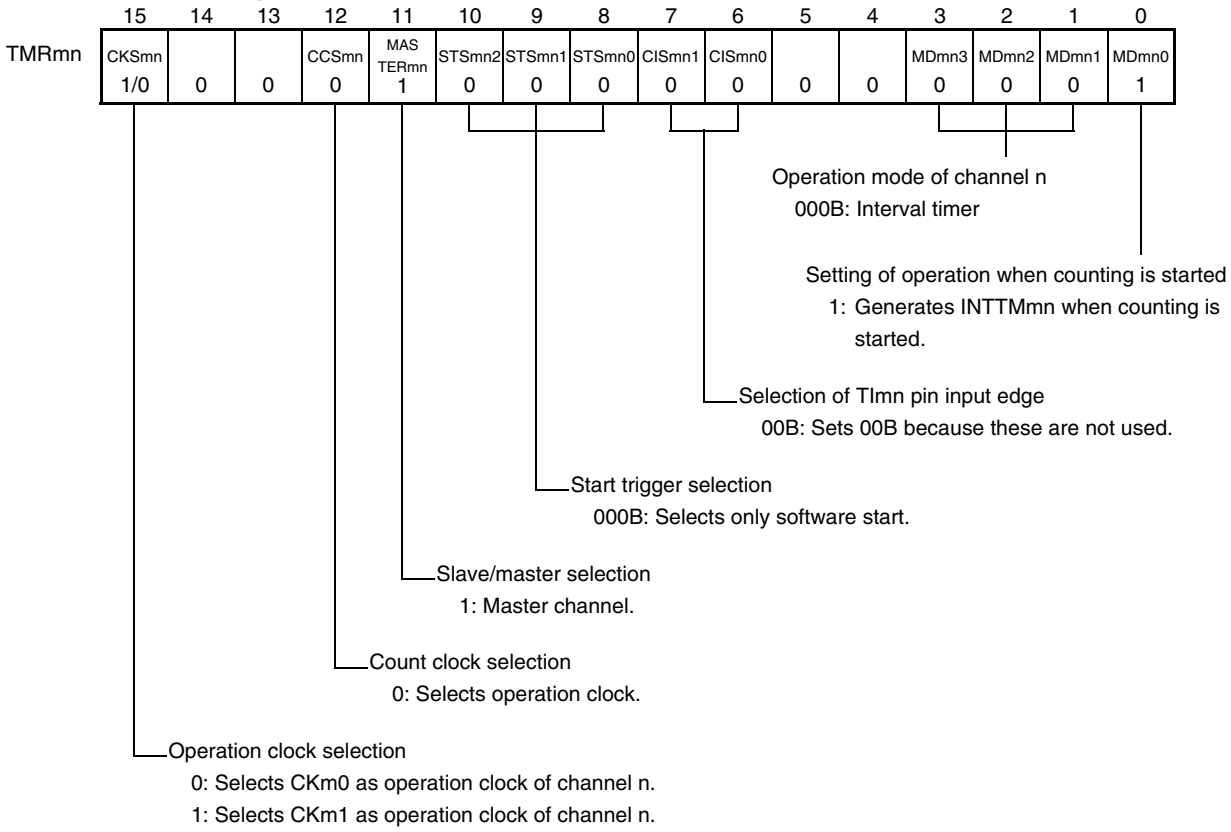
TImn: TImn pin input signal

TCRmn: Timer/counter register mn (TCRmn)

TDRmn: Timer data register mn (TDRmn)

Figure 8-68. Example of Set Contents of Registers When PWM Function (Master Channel) Is Used

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn 0	0: Outputs 0 from TOmn.

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn 0	0: Stops the TOmn output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn 0	0: Cleared to 0 when TOMmn = 0 (master channel output mode).

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn 0	0: Sets master channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12

(2) Scan mode

The four analog input channels of scans 0 to 3, which are specified by the analog input channel specification register (ADS), while the ADMD bit of the A/D converter mode register (ADM) is 1, are A/D converted successively. A/D conversion is performed in sequence, starting from the analog input channel specified by scan 0.

When A/D conversion of one analog input is complete, the conversion result is stored in the A/D conversion result register (ADCR) and the A/D conversion end interrupt request signal (INTAD) is generated.

The A/D conversion results of all the analog input channels are stored in the ADCR register. It is therefore recommended to save the contents of the ADCR register to RAM, once A/D conversion of one analog input channel has been completed.

After A/D conversion has been completed, A/D conversion is repeated successively, unless the ADCS bit is set to 0.

If anything is written to the ADM or ADS register during conversion, A/D conversion is aborted. In this case, A/D conversion is started again from the analog input channel of scan 0.

Figure 13-15. Example of Scan Mode Operation Timing

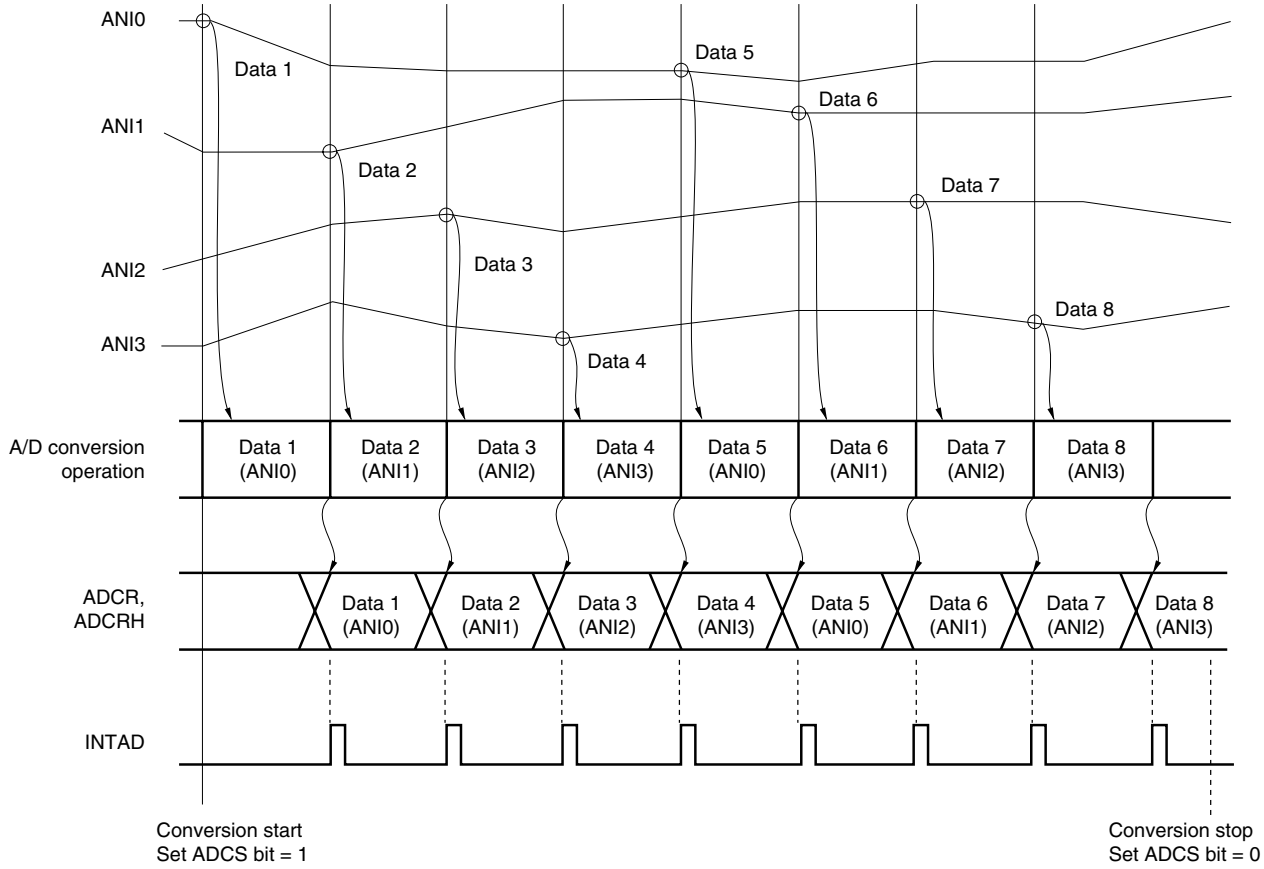


Table 14-1. Configuration of Serial Array Unit (2/2) (78K0R/KF3-L, 78K0R/KG3-L)

Item	Configuration	
	μPD78F1010, 78F1011, 78F1012, 78F1013, 78F1014	μPD78F1027, 78F1028, 78F1029, 78F1030
Shift register	8 bits	
Buffer register	Lower 8 bits of serial data register mn (SDRmn)[Note]	
Serial clock I/O	$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$ pins (for 3-wire serial I/O), SCL10, SCL20 pins (for simplified I^2C)	$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$, $\overline{SCK40}$, $\overline{SCK41}$ pins (for 3-wire serial I/O), SCL10, SCL20 pins (for simplified I^2C)
Serial data input	SI00, SI01, SI10, SI20 pins (for 3-wire serial I/O), RxD0 to RxD2 pins (for UART), RxD3 pin (for UART supporting LIN-bus)	SI00, SI01, SI10, SI20, SI40, SI41 pins (for 3-wire serial I/O), RxD0 to RxD2, RxD4 pins (for UART), RxD3 pin (for UART supporting LIN-bus)
Serial data output	SO00, SO01, SO10, SO20 pins (for 3-wire serial I/O), TxD0 to TxD2 pins (for UART), TxD3 pin (for UART supporting LIN-bus), output controller	SO00, SO01, SO10, SO20, SO40, SO41 pins (for 3-wire serial I/O), TxD0 to TxD2, TxD4 pins (for UART), TxD3 pin (for UART supporting LIN-bus), output controller
Serial data I/O	SDA10, SDA20 pins (for simplified I^2C)	
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)	<Registers of unit setting block> • Peripheral enable registers 0, 1 (PER0, PER1) • Serial clock select register m (SPSm) • Serial channel enable status register m (SEm) • Serial channel start register m (SSm) • Serial channel stop register m (STm) • Serial output enable register m (SOEm) • Serial output register m (SOm) • Serial output level register m (SOLm) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register mn (SDRmn) • Serial mode register mn (SMRmn) • Serial communication operation setting register mn (SCRmn) • Serial status register mn (SSRmn) • Serial flag clear trigger register mn (SIRmn)	
	• Port input mode registers 0, 1, 14 (PIM0, PIM1, PIM14) • Port output mode registers 0, 1, 14 (POM0, POM1, POM14) • Port mode registers 0, 1, 4, 14 (PM0, PM1, PM4, PM14) • Port registers 0, 1, 4, 14 (P0, P1, P4, P14	

Note The lower 8 bits of serial data register mn (SDRmn) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IICr communication … SIOr (IICr data register)

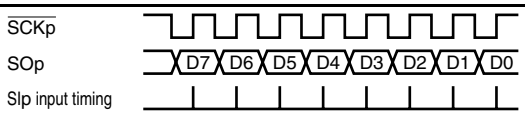
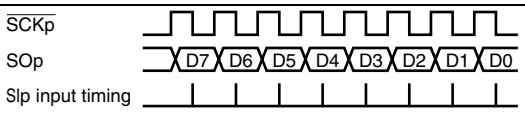
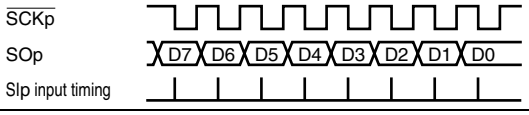
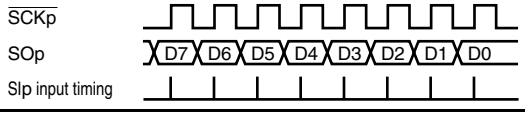
Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10, 20, 40, 41), q: UART number (q = 0 to 4), r: IIC number (r = 10, 20)

Figure 14-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (1/4)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), F0158H, F0159H (SCR10) to F015EH, F015FH (SCR13), F020CH, F020DH (SCR20), F020EH, F020FH (SCR21) After reset: 0087H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

TXE mn	RXE mn	Setting of operation mode of channel n
0	0	Disable communication.
0	1	Reception only
1	0	Transmission only
1	1	Transmission/reception

DAP mn	CKP mn	Selection of data and clock phase in CSI mode	Type
0	0		1
0	1		2
1	0		3
1	1		4
Be sure to set DAPmn, CKPmn = 0, 0 in the UART mode and simplified I^2C mode.			

EOC mn	Selection of masking of error interrupt signal (INTSREx (x = 0 to 3))
0	Masks error interrupt INTSREx (INTSRx is not masked).
1	Enables generation of error interrupt INTSREx (INTSRx is masked if an error occurs).
Set EOCmn = 0 in the CSI mode, simplified I^2C mode, and during UART transmission Note. Set EOCmn = 1 during UART reception.	

Note When using CSI01 not with EOC01 = 0, error interrupt INTSRE0 may be generated.

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

(**Remark** is listed on the next page.)

(10) Serial channel enable status register m (SEm)

The SEm register indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register m (SSm), the corresponding bit of this register is set to 1.

When 1 is written a bit of serial channel stop register m (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of the CKOmn bit (serial clock output of channel n) of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of the CKOmn bit of the SOm register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

The SEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SEm register can be set with an 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears the SEm register to 0000H.

Figure 14-14. Format of Serial Channel Enable Status Register m (SEm)

Address: F0120H, F0121H (SE0), F0160H, F0161H (SE1), F0210H, F0211H (SE2) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEm	0	0	0	0	0	0	0	0	0	0	0	0	SEm 3 Note	SEm 2 Note	SEm 1	SEm 0

SEm n	Indication of operation enable/stop status of channel n
0	Operation stops
1	Operation is enabled.

Note Those bits are invalid while operating serial allay unit 2.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03

78K0R/KF3-L□μ PD78F1010, 78F1011, 78F1012□: mn = 00 to 03, 10 to 13

78K0R/KF3-L□μ PD78F1027, 78F1028□: mn = 00 to 03, 10 to 13, 20, 21

78K0R/KG3-L□μ PD78F1013, 78F1014□: mn = 00 to 03, 10 to 13

78K0R/KG3-L□μ PD78F1029, 78F1030□: mn = 00 to 03, 10 to 13, 20, 21

Table 14-2. Selection of Operation Clock For 3-Wire Serial I/O

SMRmn Register	SPSm Register								Operation Clock (f_{MCK}) Note 1	
CKSmn	PRS m13	PRS m12	PRS m11	PRS m10	PRS m03	PRS m02	PRS m01	PRS m00		f_{CLK} = 20 MHz
0	X	X	X	X	0	0	0	0	f_{CLK}	20 MHz
	X	X	X	X	0	0	0	1	$f_{CLK}/2$	10 MHz
	X	X	X	X	0	0	1	0	$f_{CLK}/2^2$	5 MHz
	X	X	X	X	0	0	1	1	$f_{CLK}/2^3$	2.5 MHz
	X	X	X	X	0	1	0	0	$f_{CLK}/2^4$	1.25 MHz
	X	X	X	X	0	1	0	1	$f_{CLK}/2^5$	625 kHz
	X	X	X	X	0	1	1	0	$f_{CLK}/2^6$	313 kHz
	X	X	X	X	0	1	1	1	$f_{CLK}/2^7$	156 kHz
	X	X	X	X	1	0	0	0	$f_{CLK}/2^8$	78.1 kHz
	X	X	X	X	1	0	0	1	$f_{CLK}/2^9$	39.1 kHz
	X	X	X	X	1	0	1	0	$f_{CLK}/2^{10}$	19.5 kHz
	X	X	X	X	1	0	1	1	$f_{CLK}/2^{11}$	9.77 kHz
	X	X	X	X	1	1	1	1	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
1	0	0	0	0	X	X	X	X	f_{CLK}	20 MHz
	0	0	0	1	X	X	X	X	$f_{CLK}/2$	10 MHz
	0	0	1	0	X	X	X	X	$f_{CLK}/2^2$	5 MHz
	0	0	1	1	X	X	X	X	$f_{CLK}/2^3$	2.5 MHz
	0	1	0	0	X	X	X	X	$f_{CLK}/2^4$	1.25 MHz
	0	1	0	1	X	X	X	X	$f_{CLK}/2^5$	625 kHz
	0	1	1	0	X	X	X	X	$f_{CLK}/2^6$	313 kHz
	0	1	1	1	X	X	X	X	$f_{CLK}/2^7$	156 kHz
	1	0	0	0	X	X	X	X	$f_{CLK}/2^8$	78.1 kHz
	1	0	0	1	X	X	X	X	$f_{CLK}/2^9$	39.1 kHz
	1	0	1	0	X	X	X	X	$f_{CLK}/2^{10}$	19.5 kHz
	1	0	1	1	X	X	X	X	$f_{CLK}/2^{11}$	9.77 kHz
	1	1	1	1	X	X	X	X	INTTM02 if m = 0 Note 2, setting prohibited if m = 1	
Other than above									Setting prohibited	

Notes 1. When changing the clock selected for f_{CLK} (by changing the system clock control register (CKC) value), do so after having stopped (serial channel stop register m (STm) = 000FH) the operation of the serial array unit (SAU). When selecting INTTM02 for the operation clock, also stop the timer array unit 0 (timer channel stop register 0 (TT0) = 00FFH).

2. SAU0 can be operated at a fixed division ratio of the subsystem clock, regardless of the f_{CLK} frequency (main system clock, sub system clock), by operating the interval timer for which $f_{SUB}/4$ Note 3 has been selected as the count clock (setting the TIS02 bit of timer input select register 0 (TIS0) to 1) and selecting INTTM02 by using the SPS0 register in channel 2 of TAU0. When changing f_{CLK}, however, SAU0 and TAU0 must be stopped as described in Note 1 above.

3. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

Remarks 1. X: Don't care

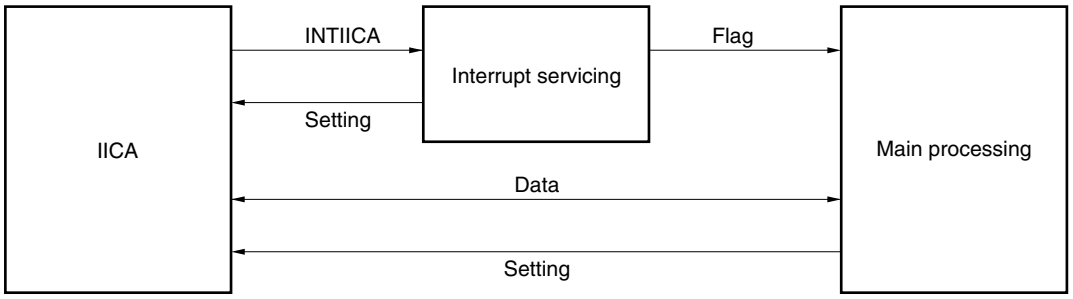
2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

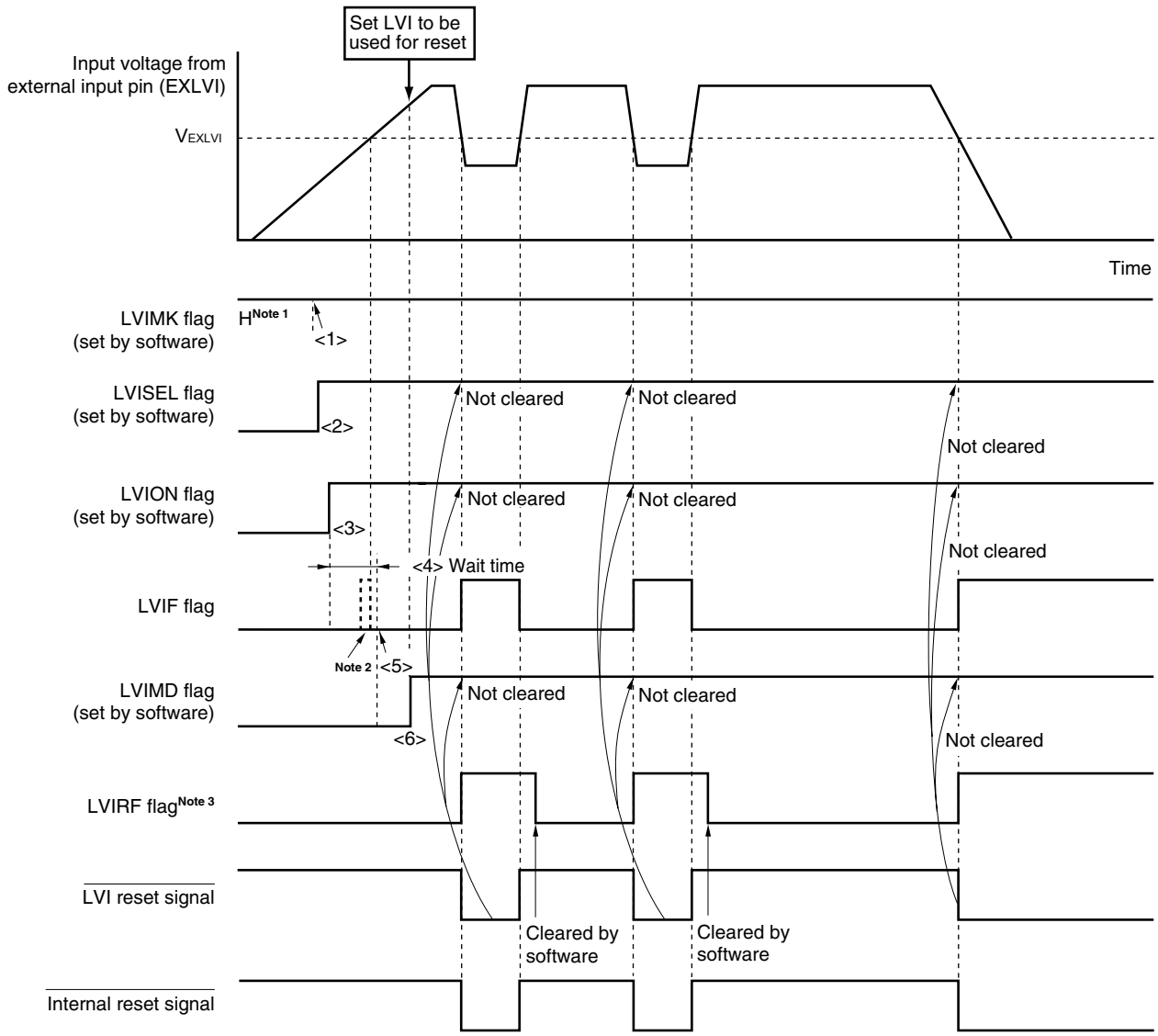
<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICA interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC bit.

Figure 23-7. Timing of Low-Voltage Detector Internal Reset Signal Generation (Bit: LVISEL = 1)



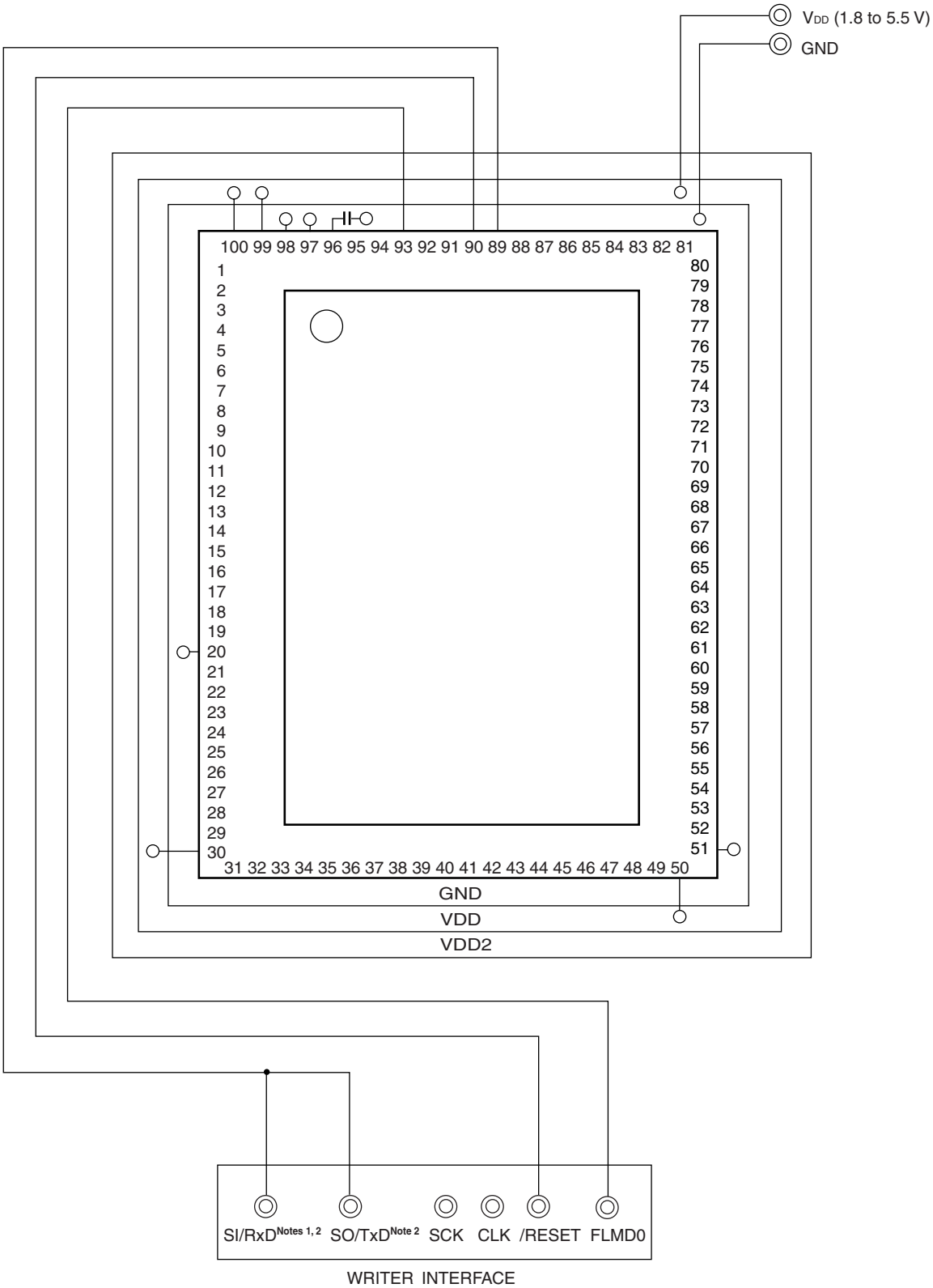
Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The LVIIF flag of the interrupt request flag registers and the LVIF flag may be set (1).

3. LVIRF flag is bit 0 of the reset control flag register (RESF). For details of the RESF register, see **CHAPTER 21 RESET FUNCTION**.

Remark <1> to <6> in Figure 23-7 above correspond to <1> to <6> in the description of "When starting operation" in **23.4.1 (2) When detecting level of input voltage from external input pin (EXLVI)**.

Figure 26-7. Example of Wiring Adapter for Flash Memory Writing (78K0R/KG3-L, LQFP (14x20))



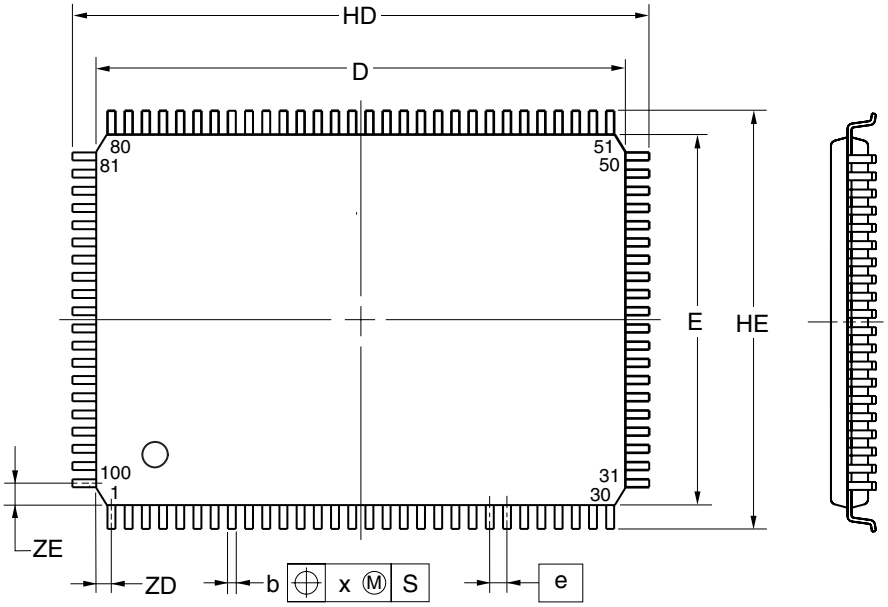
Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

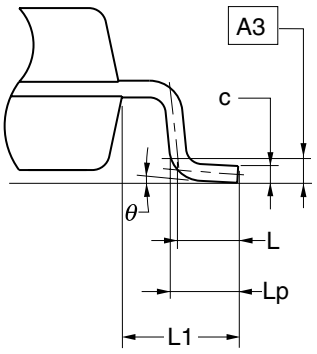
32.7 78K0R/KG3-L

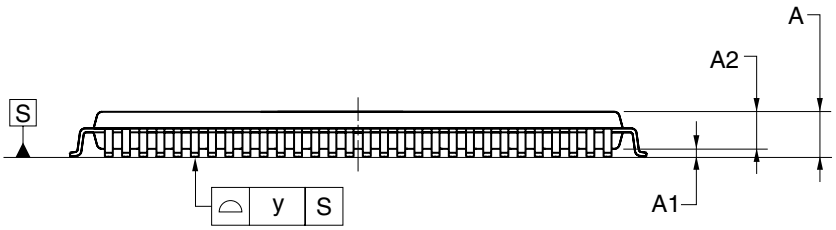
μPD78F1013GF-GAS-AX, 78F1014GF-GAS-AX, 78F1029GF-GAS-AX, 78F1030GF-GAS-AX

100-PIN PLASTIC LQFP (14x20)



detail of lead end





NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.30^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825

P100GF-65-GAS

A.5 Debugging Tools (Hardware)

A.5.1 When using in-circuit emulator

(1) QB-78K0RIX3 (compatible with 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)

QB-78K0RIX3 In-circuit emulator	This in-circuit emulator serves to debug hardware and software when developing application systems using the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L microcontrollers. It supports to the integrated debugger (ID78K0R-QB). This emulator should be used in combination with a power supply unit and emulation probe, and the USB is used to connect this emulator to the host machine.
QB-COMMON-PW-××Note 1	This power supply unit can be used in common with the all products of in-circuit emulator IECUBE and the flash memory programmer PG-FP5.
QB-144-CA-01 Check pin adapter	This check pin adapter is used in waveform monitoring using the oscilloscope, etc.
QB-80-EP-01T Emulation probe	This emulation probe is flexible type and used to connect the in-circuit emulator and target system.
QB-xxxx-EA-xxxNote 2 Exchange adapter	This exchange adapter is used to perform pin conversion from the in-circuit emulator to target connector.
QB-xxxx-YS-xxxxNote 2 Space adapter	This space adapter is used to adjust the height between the target system and in-circuit emulator.
QB-xxxx-YQ-xxxNote 2 YQ connector	This YQ connector is used to connect the target connector and exchange adapter.
QB-xxxx-HQ-XxxNote 2 Mount adapter	This mount adapter is used to mount the target device with socket.
QB-xxxx-NQ-xxxNote 2 Target connector	This target connector is used to mount on the target system.

Notes 1. ×× differs depending on the target area of each product.

2. The part numbers of the exchange adapter, space adapter, YQ connector, mount adapter, and target connector and the packages of the target device are described below.

	Package		Exchange Adapter	Space Adapter	YQ Connector	Mount Adapter	Target Connector
<R>	78K0R/KC3-L	40-pin plastic WQFN (K8-4B4 type)	QB-40K8-EA-02T	None	None	None	QB-40K8-NQ-01T
		44-pin plastic LQFP (GB-GAF type)	QB-44GB-EA-04T	QB-44GB-YS-01T	QB-44GB-YQ-01T	QB-44GB-HQ-01T	QB-44GB-NQ-01T
		48-pin plastic LQFP (GA-HAA type)	QB-48GA-EA-04T	QB-48GA-YS-01T	QB-48GA-YQ-01T	QB-48GA-HQ-01T	QB-48GA-NQ-01T
<R>		48-pin plastic WQFN (K8-5B4 type)	QB-48K8-EA-02T	None	None	None	QB-48K8-NQ-01T
	78K0R/KD3-L	52-pin plastic LQFP (GB-GAG type)	QB-52GB-EA-04T	QB-52GB-YS-01T	QB-52GB-YQ-01T	QB-52GB-HQ-01T	QB-52GB-NQ-01T
	78K0R/KE3-L	64-pin plastic LQFP (GB-GAH type)	QB-64GB-EA-04T	QB-64GB-YS-01T	QB-64GB-YQ-01T	QB-64GB-HQ-01T	QB-64GB-NQ-01T
		64-pin plastic LQFP (GK-GAJ type)	QB-64GK-EA-04T	QB-64GK-YS-01T	QB-64GK-YQ-01T	QB-64GK-HQ-01T	QB-64GK-NQ-01T
		64-pin plastic TQFP (GA-HAB type)	QB-64GA-EA-01T	QB-64GA-YS-01T	QB-64GA-YQ-01T	QB-64GA-HQ-01T	QB-64GA-NQ-01T
		64-pin plastic FBGA (F1-AN1 type)	QB-64FC-EA-01T	None	None	None	QB-64FC-NQ-01T
		64-pin plastic FBGA (F1-AA2 type)	QB-64F1-EA-03T	None	None	None	QB-64F1-NQ-01T

(Remarks are listed on the next page or later.)