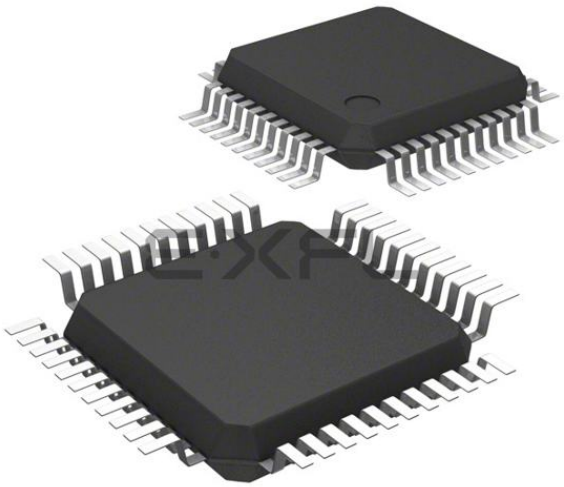
Renesas Electronics America Inc - UPD78F1002GB-GAF-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1002gb-gaf-ax

Input to the P71, P72, P74, and P75 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 7 (PIM7).

Output from the P70, P72, P73, and P75 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 7 (POM7).

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P70/KR0/SO01/INTP4	√		√	√	√
P71/KR1/SI01/INTP5	√		√	√	√
P72/KR2/$\overline{\text{SCK01}}$/INTP6	√		√	√	√
P73/KR3/SO00/TxD0	√		√	√	√
P74/KR4/SI00/RxD0	√		√	√	√
P75/KR5/$\overline{\text{SCK00}}$	√		√	√	√
P76/KR6	–		–	√	√
P77/KR7	–		–	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P70 to P77 function as an I/O port. P70 to P77 can be set to input or output port in 1-bit units using port mode register 7 (PM7). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 7 (PU7).

(2) Control mode

P70 to P77 function as key interrupt input, serial interface data I/O, clock I/O, and external interrupt request input.

(a) KR0 to KR7

These are the key interrupt input pins.

(b) SI00, SI01

These are the serial data input pin of serial interface CSI00 and CSI01.

(c) SO00, SO01

These are the serial data output pin of serial interface CSI00 and CSI01.

(d) $\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$

These are the serial clock I/O pins of serial interface CSI00 and CSI01.

(e) RxD0

This is a serial data input pin of serial interface UART0.

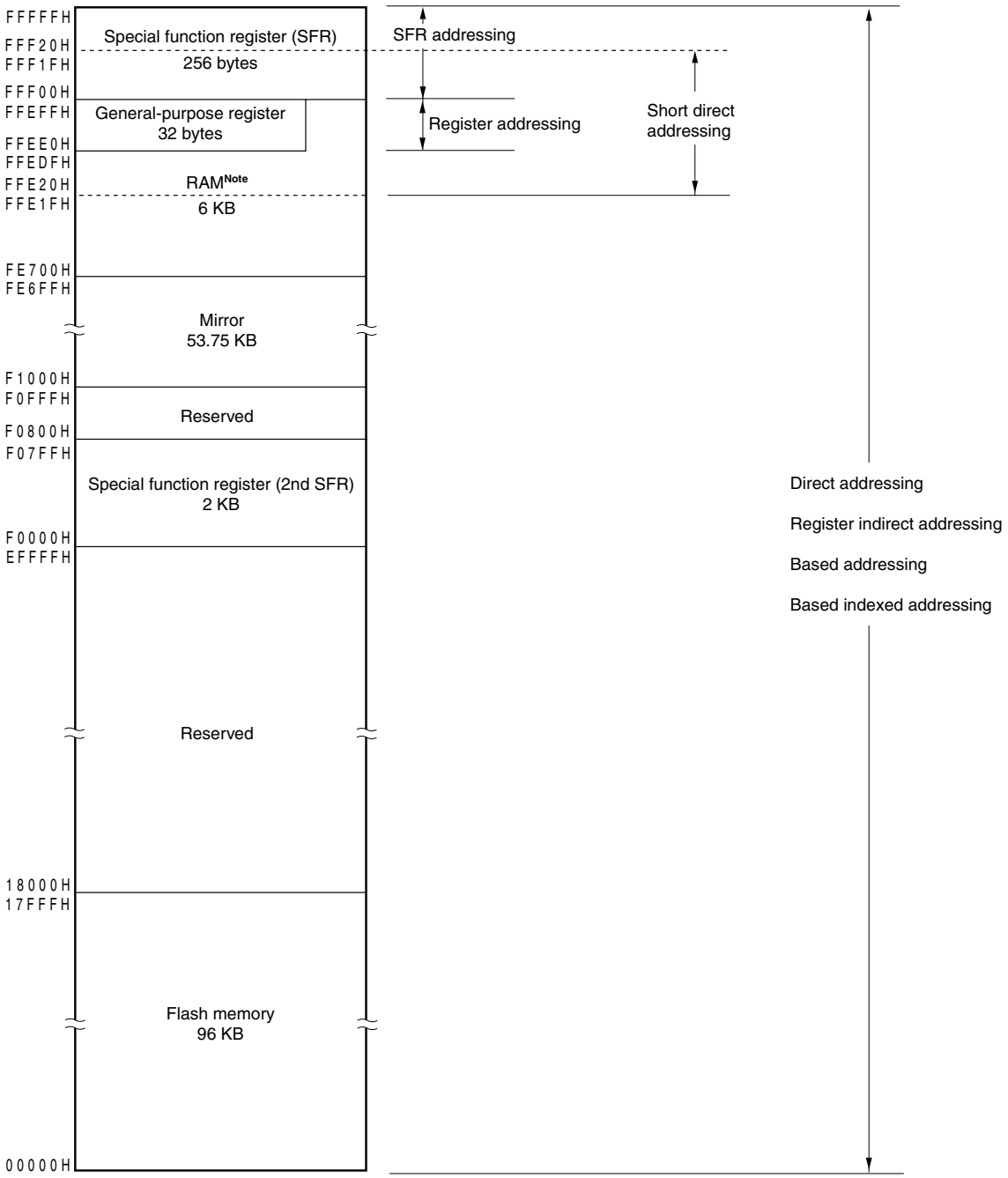
Table 3-4. Connection of Unused Pins (3/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P80 to P87	5-AG	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P91			
P110	8-R		
P111	5-AG		
P120/INTP0/EXLVI	8-R		
P121/X1[Note 1]	37-C	Input	Independently connect to V_{DD} or V_{SS} via a resistor.
P122/X2/EXCLK[Note 1]			
P123/XT1[Note 1]	37-B		
P124/XT2[Note 1]			
P130	3-C	Output	Leave open.
P131/TI06/TO06	8-R	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P140/PCLBUZ0/ITNP6			
P141/PCLBUZ1/INTP7			
P142/$\overline{SCK20}$/SCL20	5-AN		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P143/SI20/RxD2/SDA20			
P144/SO20/TxD2	5-AG		<When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P145/TI07/TO07	8-R		Input: Independently connect to EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} via a resistor. Output: Leave open.
P150/ANI8 to P157/ANI15[Note 2]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
AV_{REF}	–	–	<When one or more of P20 to P27 and P150 to P157 are set as a digital port> Make this pin the same potential as EV_{DD0}, EV_{DD1}, or V_{DD}. <When all of P20 to P27 and P150 to P157 are set as analog ports> Make this pin to have a potential where 1.8 V ≤ AV_{REF} ≤ V_{DD}.
AV_{SS}	–	–	Make this pin the same potential as EV_{SS0}, EV_{SS1}, or V_{SS}.
FLMD0	2-W	–	Leave open or connect to V_{SS} via a resistor of 100 kΩ or more.
$\overline{RESET}$	2	Input	Connect directly or via a resistor to EV_{DD0} or EV_{DD1}.
REGC	–	–	Connect to V_{SS} via capacitor (0.47 to 1 μF: target).

Notes 1. Use recommended connection above in input port mode (see **Figure 7-3 Format of Clock Operation Mode Control Register (CMC)**) when these pins are not used.

2. P150/ANI8 to P157/ANI15 are set in the digital input port mode after release of reset.

Figure 4-16. Correspondence Between Data Memory and Addressing (μPD78F1011, 78F1013)

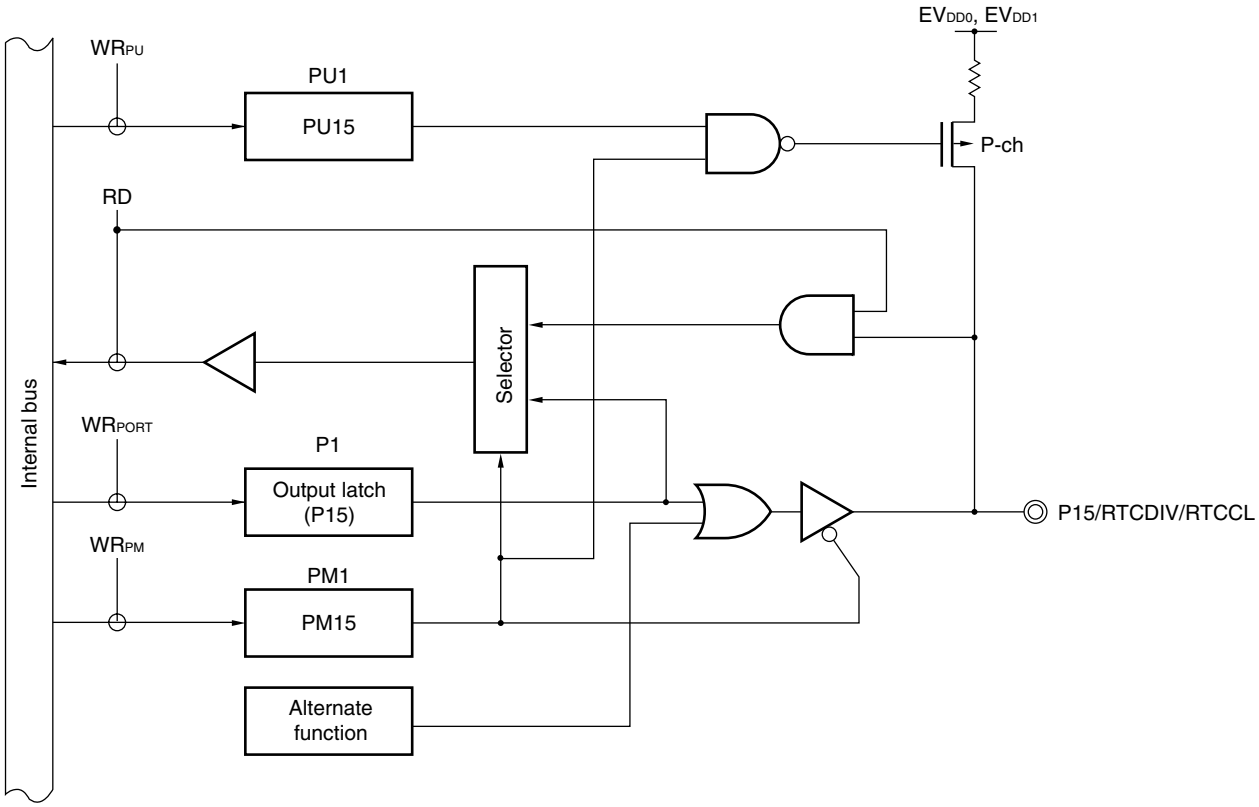


Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

Table 4-6. Extended SFR (2nd SFR) List (4/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0158H	Serial communication operation setting register 10	SCR10		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F0159H															
F015AH	Serial communication operation setting register 11	SCR11		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015BH															
F015CH	Serial communication operation setting register 12	SCR12		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015DH															
F015EH	Serial communication operation setting register 13	SCR13		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015FH															
F0160H	Serial channel enable status register 1	SE1L	SE1	R	√	√	√	0000H	–	–	–	–	–	√	√
F0161H		–			–	–			–	–	–	–	–	√	√
F0162H	Serial channel start register 1	SS1L	SS1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F0163H		–			–	–			–	–	–	–	–	√	√
F0164H	Serial channel stop register 1	ST1L	ST1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F0165H		–			–	–			–	–	–	–	–	√	√
F0166H	Serial clock select register 1	SPS1L	SPS1	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0167H		–			–	–			–	–	–	–	–	√	√
F0168H	Serial output register 1	SO1		R/W	–	–	√	0F0FH	–	–	–	–	–	√	√
F0169H															
F016AH	Serial output enable register 1	SOE1L	SOE1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F016BH		–			–	–			–	–	–	–	–	√	√
F0174H	Serial output level register 1	SOL1L	SOL1	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0175H		–			–	–			–	–	–	–	–	√	√
F0180H	Timer counter register 00	TCR00		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0181H															
F0182H	Timer counter register 01	TCR01		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0183H															
F0184H	Timer counter register 02	TCR02		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0185H															
F0186H	Timer counter register 03	TCR03		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0187H															
F0188H	Timer counter register 04	TCR04		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0189H															
F018AH	Timer counter register 05	TCR05		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018BH															
F018CH	Timer counter register 06	TCR06		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018DH															
F018EH	Timer counter register 07	TCR07		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018FH															

Figure 6-11. Block Diagram of P15



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (5/6)

(11) CPU clock changing from subsystem clock (D) to high-speed system clock (C) (products other than 78K0R/KC3-L (40-pin))

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	OSTS Register	CSC Register	OSMC Register	OSTC Register	CKC Register	
		MSTOP	FSEL		MCM0	CSS
(D) → (C) (X1 clock: 2 MHz ≤ fx ≤ 10 MHz)	**Note 1**	0	0	Must be checked	1	0
(D) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	**Note 1**	0	1 Note 2	Must be checked	1	0
(D) → (C) (external main clock)	**Note 1**	0	0/1	Must not be checked	1	0

Unnecessary if the CPU is operating with the high-speed system clock

Unnecessary if these registers are already set

Notes 1. Set the oscillation stabilization time as follows.

- Desired the oscillation stabilization time counter status register (OSTC) oscillation stabilization time ≤ Oscillation stabilization time set by the oscillation stabilization time select register (OSTS)

2. FSEL = 1 when f_{CLK} > 10 MHz

If a divided clock is selected and f_{CLK} ≤ 10 MHz, use with FSEL = 0 is possible even if fx > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)).

(12) CPU clock changing from 20 MHz internal high-speed oscillation clock (J) to internal high-speed oscillation clock (B)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	DSCCTL Register	
	SELDSC	DSCON
(J) → (B)	0	0

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Figure 8-11. Format of Timer Mode Register mn (TMRmn) (2/3)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKSmn	0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

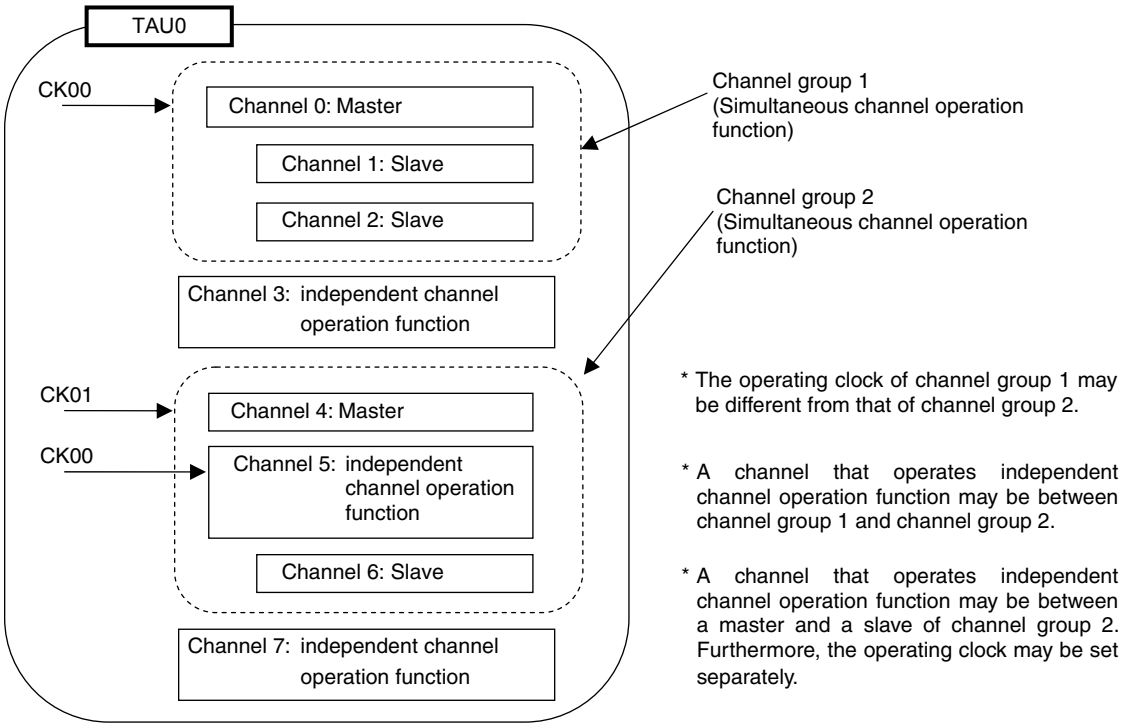
MASTERmn	Selection between using channel n independently or simultaneously with another channel(as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the even channel can be set as a master channel (MASTERmn = 1). Be sure to use odd-numbered channels as slave channels (MASTERmn = 0). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

STSmn2	STSmn1	STSmn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

CISmn1	CISmn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Example


TAU0
CK00
Channel 0: Master
Channel 1: Slave
Channel 2: Slave
Channel 3: independent channel operation function
CK01
CK00
Channel 4: Master
Channel 5: independent channel operation function
Channel 6: Slave
Channel 7: independent channel operation function
Channel group 1 (Simultaneous channel operation function)
Channel group 2 (Simultaneous channel operation function)
* The operating clock of channel group 1 may be different from that of channel group 2.
* A channel that operates independent channel operation function may be between channel group 1 and channel group 2.
* A channel that operates independent channel operation function may be between a master and a slave of channel group 2. Furthermore, the operating clock may be set separately.

8.8.3 Operation as multiple PWM output function

By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

For example, when using two slave channels, the period and duty factor of an output pulse can be calculated by the following expressions.

Pulse period = {Set value of TDRmn (master) + 1} × Count clock period
Duty factor 1 [%] = {Set value of TDRmp (slave 1)}/{Set value of TDRmn (master) + 1} × 100
Duty factor 2 [%] = {Set value of TDRmq (slave 2)}/{Set value of TDRmn (master) + 1} × 100

Remark Although the duty factor exceeds 100% if the set value of TDRmp (slave 1) > {set value of TDRmn (master) + 1} or if the {set value of TDRmq (slave 2)} > {set value of TDRmn (master) + 1}, it is summarized into 100% output.

Timer/counter register mn (TCRmn) of the master channel operates in the interval timer mode and counts the periods.

The TCRmp register of the slave channel 1 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmp pin. The TCRmp register loads the value of timer data register mp (TDRmp), using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmp = 0000H, TCRmp outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmp becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmp = 0000H.

In the same way as the TCRmp register of the slave channel 1, the TCRmq register of the slave channel 2 operates in one-count mode, counts the duty factor, and outputs a PWM waveform from the TOmq pin. The TCRmq register loads the value of the TDRmq register, using INTTMmn of the master channel as a start trigger, and starts counting down. When TCRmq = 0000H, the TCRmq register outputs INTTMmq and stops counting until the next start trigger (INTTMmn of the master channel) has been input. The output level of TOmq becomes active one count clock after generation of INTTMmn from the master channel, and inactive when TCRmq = 0000H.

When channel 0 is used as the master channel as above, up to seven types of PWM signals can be output at the same time.

Caution To rewrite both timer data register mn (TDRmn) of the master channel and the TDRmp register of the slave channel 1, write access is necessary at least twice. Since the values of the TDRmn and TDRmp registers are loaded to the TCRmn and TCRmp registers after INTTMmn is generated from the master channel, if rewriting is performed separately before and after generation of INTTMmn from the master channel, the TOmp pin cannot output the expected waveform. To rewrite both the TDRmn register of the master and the TDRmp register of the slave, be sure to rewrite both the registers immediately after INTTMmn is generated from the master channel (This applies also to the TDRmq register of the slave channel 2).

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 10
p: Slave channel number 1, q: Slave channel number 2[Note]
When m = 0: $n < p < q \leq 7$
When m = 1: $n < p < q \leq 3$
(Where p and q are consecutive integers greater than n)

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

(1) Peripheral enable registers 0, 1 (PER0, PER1)

PER0 and PER1 register are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When serial array unit 0 is used, be sure to set bit 2 (SAU0EN) of PER0 register to 1.

In the 78K0R/KF3-L and 78K0R/KG3-L, be sure to set bit 3 (SAU1EN) of PER0 register to 1 when using serial array unit 1, in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030), be sure to set bit 0 (SAU2EN) of PER1 register to 1 when using serial array unit 2.

The PER0 and PER1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears the PER0 and PER1 register to 00H.

Figure 14-5. Format of Peripheral Enable Register 0, 1 (PER0, PER1)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PER1 Note	0	0	0	0	0	0	0	SAU2EN Note 4

SAUmEN	Control of serial array unit m input clock supply
0	Stops supply of input clock. • SFR used by serial array unit m cannot be written. • Serial array unit m is in the reset status.
1	Enables input clock supply. • SFR used by serial array unit m can be read/written.

Notes 1. That is not provided in 40-pin product of the 78K0R/KC3-L.

2. That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

4. 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030) only.

Cautions 1. When setting serial array unit m, be sure to set the SAUmEN bit to 1 first. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read.
Note that this does not apply to the following registers.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:
ISC, NFEN0, PIM3, PIM7, POM3, POM7, PM3, PM7, P3, and P7 registers.
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012), 78K0R/KG3-L (μPD78F1013, 78F1014):
ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM14, P0, P1, P4, and P14 registers.
78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030):
ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM5, PM14, P0, P1, P4, P5, and P14 registers.

2. After setting the SAUmEN bit to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(**Caution 3** and **Remark** are listed on the next page.)

Figure 14-8. Format of Serial Communication Operation Setting Register mn (SCRmn) (4/4)

Address: F0118H, F0119H (SCR00) to F011EH, F011FH (SCR03), After reset: 0087H R/W
F0158H, F0159H (SCR10) to F015EH, F015FH (SCR13),
F020CH, F020DH (SCR20), F020EH, F020FH (SCR21)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCRmn	TXE mn	RXE mn	DAP mn	CKP mn	0	EOC mn	PTC mn1	PTC mn0	DIR mn	0	SLC mn1	SLC mn0	0	DLS mn2	DLS mn1	DLS mn0

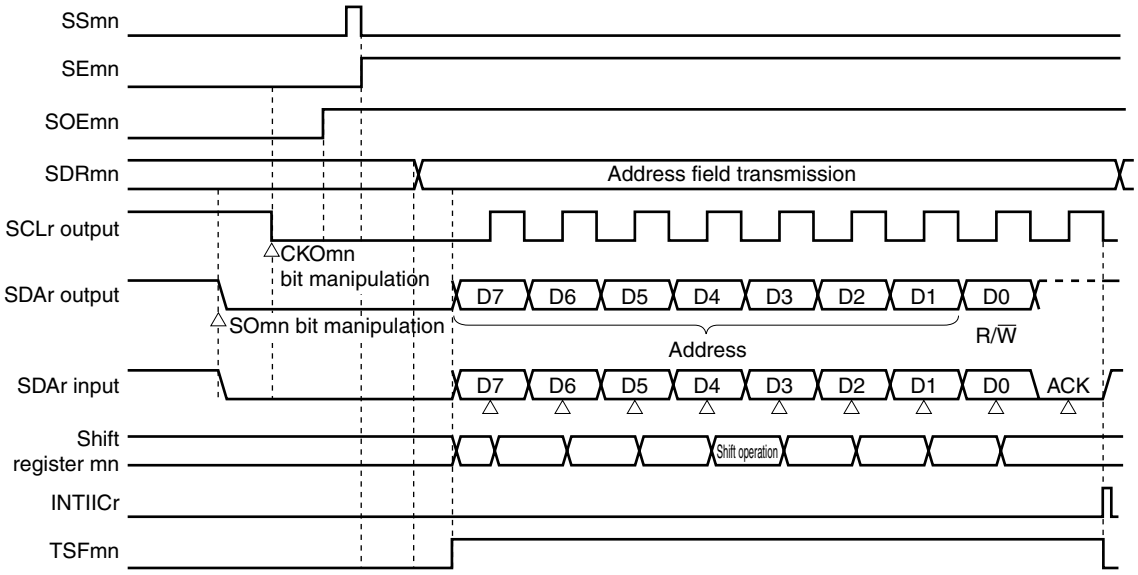
DLS mn2	DLS mn1	DLS mn0	Setting of data length in CSI and UART modes
1	0	0	5-bit data length (stored in bits 0 to 4 of the SDRmn register) (settable in UART mode only)
1	1	0	7-bit data length (stored in bits 0 to 6 of the SDRmn register)
1	1	1	8-bit data length (stored in bits 0 to 7 of the SDRmn register)
Other than above			Setting prohibited
Be sure to set DLSmn0 = 1 in the simplified I^2C mode.			

Caution Be sure to clear bits 3, 6, and 11 to "0". Be sure to set bit 2 to "1".

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L□μ PD78F1010, 78F1011, 78F1012□: mn = 00 to 03, 10 to 13
78K0R/KF3-L□μ PD78F1027, 78F1028□: mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L□μ PD78F1013, 78F1014□: mn = 00 to 03, 10 to 13
78K0R/KG3-L□μ PD78F1029, 78F1030□: mn = 00 to 03, 10 to 13, 20, 21

(3) Processing flow

Figure 14-100. Timing Chart of Address Field Transmission



Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10,r = 10, 20

Figure 14-101. Flowchart of Address Field Transmission

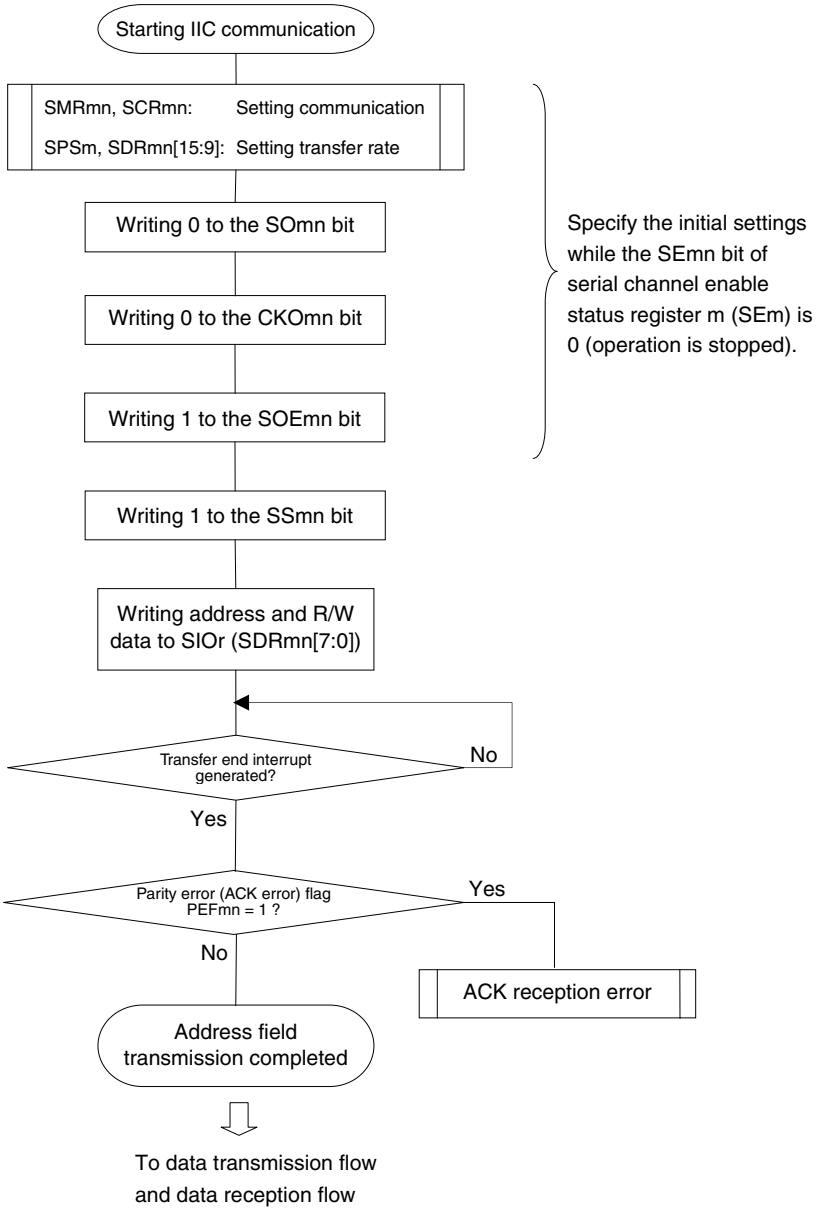


Table 14-11. Relationship between register settings and pins
(Channel 2 of unit 0: CSI10, UART1 transmission, IIC10)

SE 02 Note 1	MD 022	MD 021	SOE 02	SO 02	CKO 02	TXE 02	RXE 02	PM 04	P04	PM03 Note 2	P03 Note 2	PM02	P02	Operation mode	Pin Function		
															$\overline{\text{SCK10}}$/ SCL10/P04	SI10/SDA10/ RxD1/P03 Note 2	SO10/ TxD1/P02
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	P04	P03	P02
	0	1														P03/RxD1	
	1	0														P03	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI10 reception	$\overline{\text{SCK10}}$ (input)	SI10	P02
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI10 transmission	$\overline{\text{SCK10}}$ (input)	P03	SO10
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI10 transmission /reception	$\overline{\text{SCK10}}$ (input)	SI10	SO10
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI10 reception	$\overline{\text{SCK10}}$ (output)	SI10	P02
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI10 transmission	$\overline{\text{SCK10}}$ (output)	P03	SO10
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI10 transmission /reception	$\overline{\text{SCK10}}$ (output)	SI10	SO10
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART1 transmission Note 5	P04	P03/RxD1	TxD1
0	1	0	0	0/1 Note 6	0/1 Note 6	0	0	0	1	0	1	× Note 3	× Note 3	IIC10 start condition	SCL10	SDA10	P02
						1	0										
						0	1										
1			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC10 address field transmission	SCL10	SDA10	P02
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	0	1	× Note 3	× Note 3	IIC10 data transmission	SCL10	SDA10	P02
			1	0/1 Note 4	0/1 Note 4	0	1	0	1	0	1	× Note 3	× Note 3	IIC10 data reception	SCL10	SDA10	P02
0			0	0/1 Note 7	0/1 Note 7	0	0	0	1	0	1	× Note 3	× Note 3	IIC10 stop condition	SCL10	SDA10	P02
						1	0										
						0	1										

Notes 1. Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel statrt register 0 (SS0) and serial channel stop register 0 (ST0).

2. When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin (refer to **Table 14-12**). In this case, operation stop mode or UART1 transmission must be selected for channel 2 of unit 0.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART1 transmission and reception in a pair, set channel 3 of unit 0 to UART1 reception (refer to **Table 14-12**).

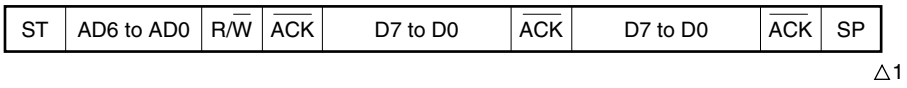
6. Set the CKO02 bit to 1 before a start condition is generated. Clear the SO02 bit from 1 to 0 when the start condition is generated.

7. Set the CKO02 bit to 1 before a stop condition is generated. Clear the SO02 bit from 0 to 1 when the stop condition is generated.

Remark X: Don't care

(4) Operation without communication

(a) Start ~ Code ~ Data ~ Data ~ Stop



△1: IICS = 00000001B

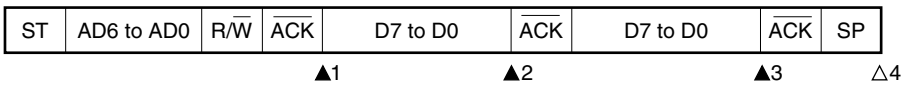
Remark △: Generated only when SPIE = 1

(5) Arbitration loss operation (operation as slave after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data

(i) When WTIM = 0



▲1: IICS = 0101×110B
▲2: IICS = 0001×000B
▲3: IICS = 0001×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

17.3 Registers Controlling DMA Controller

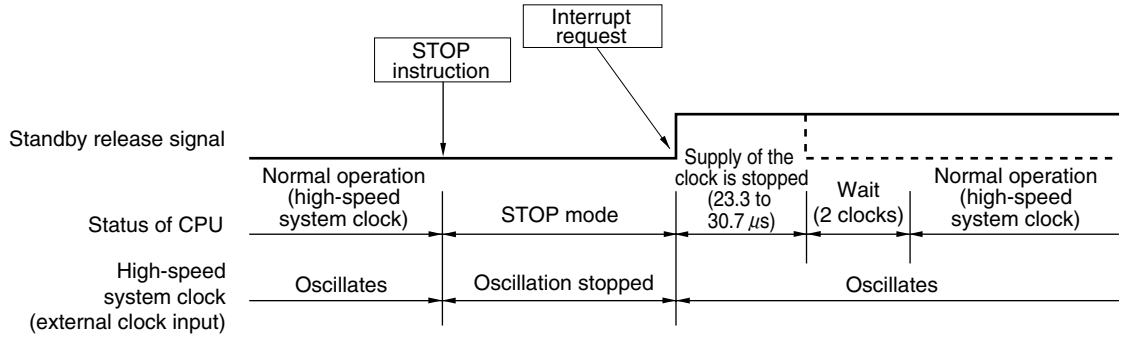
DMA controller is controlled by the following registers.

- DMA mode control register n (DMCn)
- DMA operation control register n (DRCn)

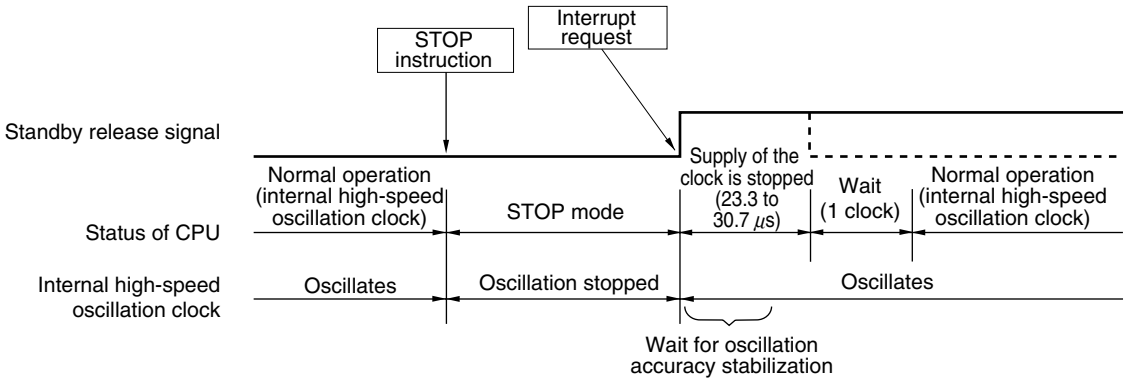
Remark n: DMA channel number (n = 0, 1)

Figure 20-5. STOP Mode Release by Interrupt Request Generation (2/2)

(2) When high-speed system clock (external clock input) is used as CPU clock

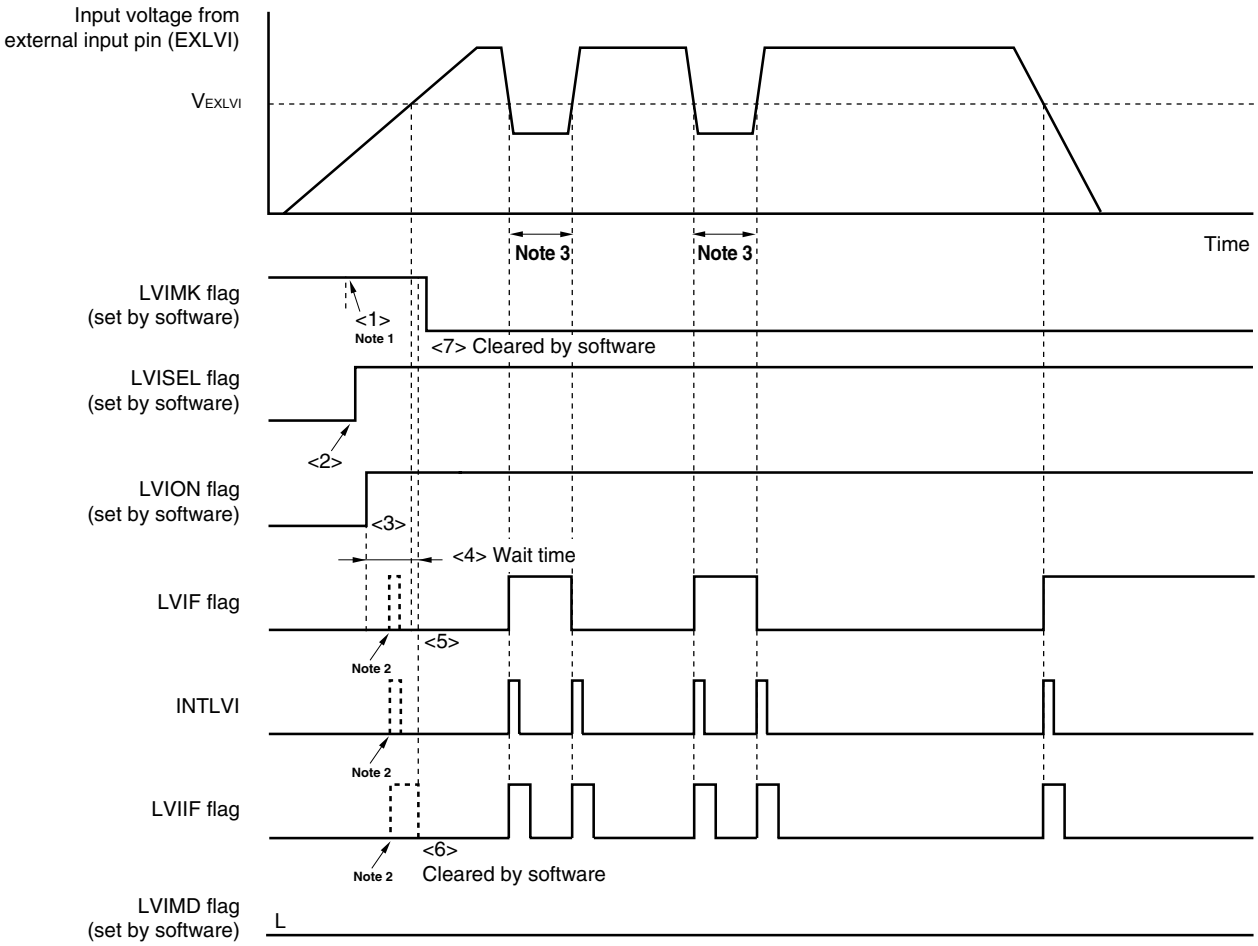


(3) When internal high-speed oscillation clock is used as CPU clock



Remark The broken lines indicate the case when the interrupt request that has released the standby mode is acknowledged.

Figure 23-10. Timing of Low-Voltage Detector Interrupt Signal Generation (Bit: LVISEL = 1)



Notes 1. The LVIMK flag is set to "1" by reset signal generation.

2. The interrupt request signal (INTLVI) is generated and the LVIF and LVIIF flags may be set (1).

3. If LVI operation is disabled (clears the LVION bit) when the input voltage of the external input pin (EXLVI) is less than or equal to the detection voltage (V_{EXLVI}), an interrupt request signal (INTLVI) is generated and the LVIIF flag may be set to 1.

Remark <1> to <7> in Figure 23-10 above correspond to <1> to <7> in the description of "When starting operation" in **23.4.2 (2) When detecting level of input voltage from external input pin (EXLVI)**.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

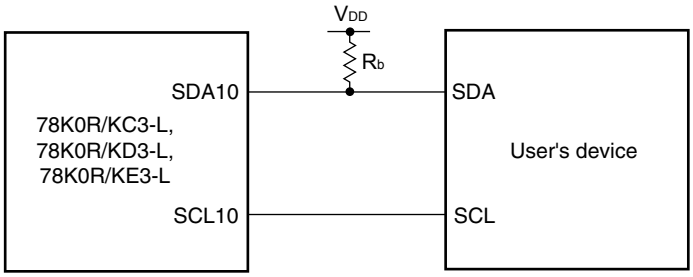
(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCL10 clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note	kHz
Hold time when SCL10 = “L”	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Hold time when SCL10 = “H”	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK}+120		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK}+230		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	660	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	710	ns

Note The value must also be f_{MCK}/4 or more.

Simplified I^2C mode connection diagram (during communication at same potential)

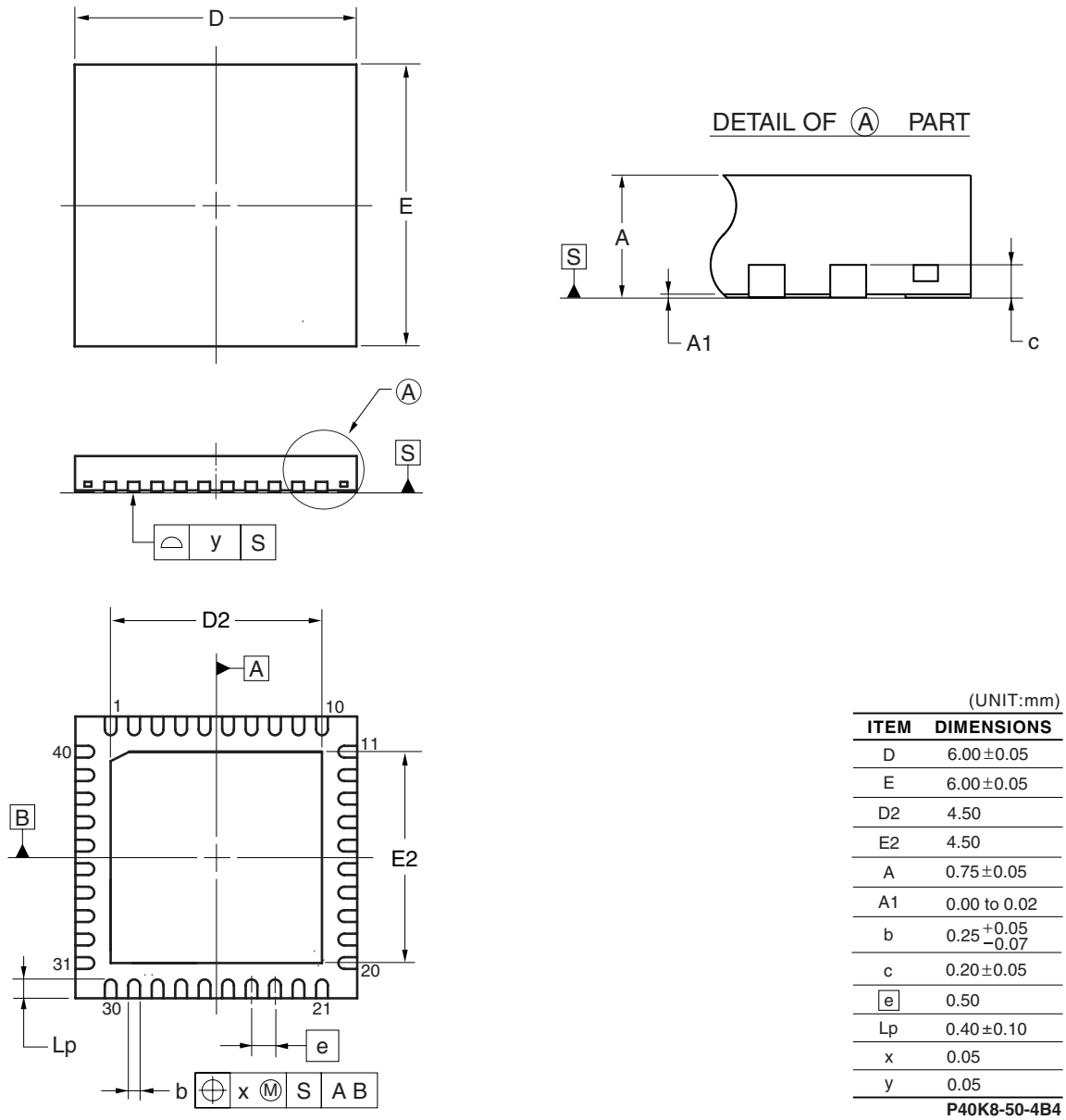


CHAPTER 32 PACKAGE DRAWINGS

32.1 78K0R/KC3-L (40-pin products)

μPD78F1000K8-4B4-AX, 78F1001K8-4B4-AX, 78F1002K8-4B4-AX, 78F1003K8-4B4-AX (Under development)

40-PIN PLASTIC WQFN(6x6)



(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.05
E	6.00±0.05
D2	4.50
E2	4.50
A	0.75±0.05
A1	0.00 to 0.02
b	$0.25^{+0.05}_{-0.07}$
c	0.20±0.05
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

P40K8-50-4B4