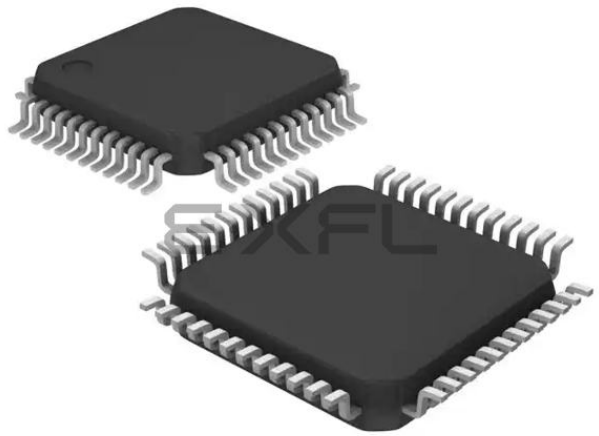
Renesas Electronics America Inc - UPD78F1003GA-HAA-AX Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1003ga-haa-ax

(2) AV_{SS}

This is the ground potential pin of A/D converter, programmable gain amplifier, comparator, P20 to P27, P150 to P153, and P80 to P83. Even when the A/D converter, programmable gain amplifier, and comparator are not used, always use this pin with the same potential as EV_{SS} or V_{SS}.

(3) V_{DD}, EV_{DD}

V_{DD} is the positive power supply pin for P121 to P124 and other than ports (other than the $\overline{\text{RESET}}$ pin and FLMD0 pin) Note.

EV_{DD} is the positive power supply pin for ports other than those of P20 to P27, P150 to P153, P80 to P83, and P121 to P124, as well as for the $\overline{\text{RESET}}$ pin and FLMD0 pin.

Note With products not provided with an EV_{DD} pin, use V_{DD} as the positive power supply pin for port pins other than P20 to P27, P150 to P153, and P80 to P83, as well as for pins other than those of ports.

(4) V_{SS}, EV_{SS}

V_{SS} is the ground potential pin for P121 to P124 and other than ports (other than the $\overline{\text{RESET}}$ pin and FLMD0 pin) Note.

EV_{SS} is the ground potential pin for ports other than those of P20 to P27, P150 to P153, P80 to P83, and P121 to P124, as well as for the $\overline{\text{RESET}}$ pin and FLMD0 pin.

Note With products not provided with an EV_{SS} pin, use V_{SS} as the ground potential pin for port pins other than P20 to P27, P150 to P153, P80 to P83, as well as for pins other than those of ports.

2.2.14 $\overline{\text{RESET}}$

This is the active-low system reset input pin.

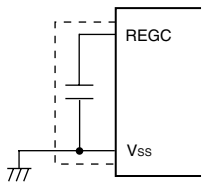
When the external reset pin is not used, connect this pin directly to EV_{DD} or via a resistor.

When the external reset pin is used, design the circuit based on V_{DD}.

2.2.15 REGC

This is the pin for connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect this pin to V_{SS} via a capacitor (0.47 to 1 μF).

Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.



Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

3.3.1 78K0R/KF3-L

Table 3-3 shows the types of pin I/O circuits and the recommended connections of unused pins. For I/O Circuit Type, see **Figure 3-1. Pin I/O Circuit List**.

Table 3-3. Connection of Unused Pins (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P02/SO10/TxD1	5-AG	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P03/SI10/RxD1/SDA10	5-AN		
P04/$\overline{SCK10}$/SCL10			
P05/TI05/TO05	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P06/TI06/TO06			
P10/$\overline{SCK00}$	5-AN		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P11/SI00/RxD0			Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P12/SO00/TxD0	5-AG		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P13/TxD3			Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P14/RxD3	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P15/RTCDIV/RTCCL	5-AG		
P16/TI01/TO01/INTP5	8-R		
P17/TI02/TO02			
P20/ANI0 to P27/ANI7[Note]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
P30/RTC1HZ/INTP3	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P31/TI03/TO03/INTP4			
P40/TOOL0			<When on-chip debugging is enabled> Pull this pin up (pulling it down is prohibited). <When on-chip debugging is disabled> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.

Note P20/ANI0 to P27/ANI7 are set in the digital input port mode after release of reset.

4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2nd SFR) has a special function.

Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (!addr16.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

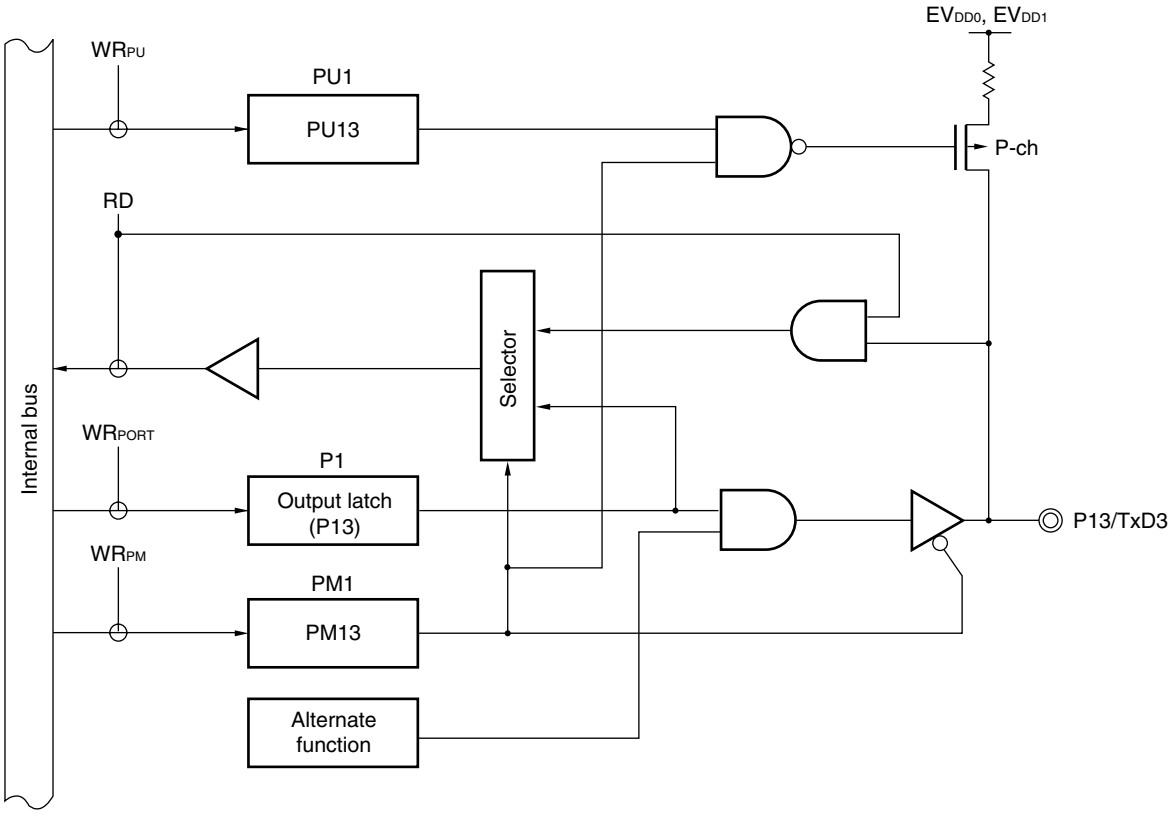
Table 4-6 gives a list of the extended SFRs. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of an extended SFR. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, ID78K0R-QB, and SM+ for 78K0R, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding extended SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

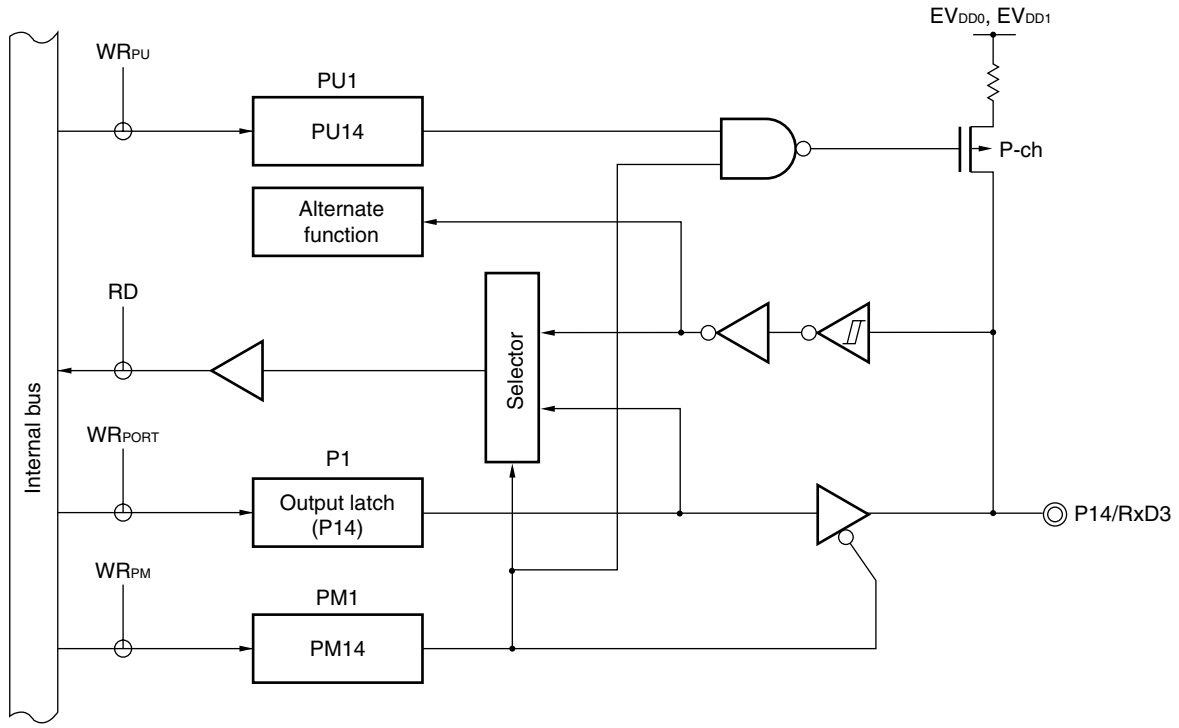
Remark For SFRs in the SFR area, see **4.2.4 Special function registers (SFRs)**.

Figure 6-9. Block Diagram of P13



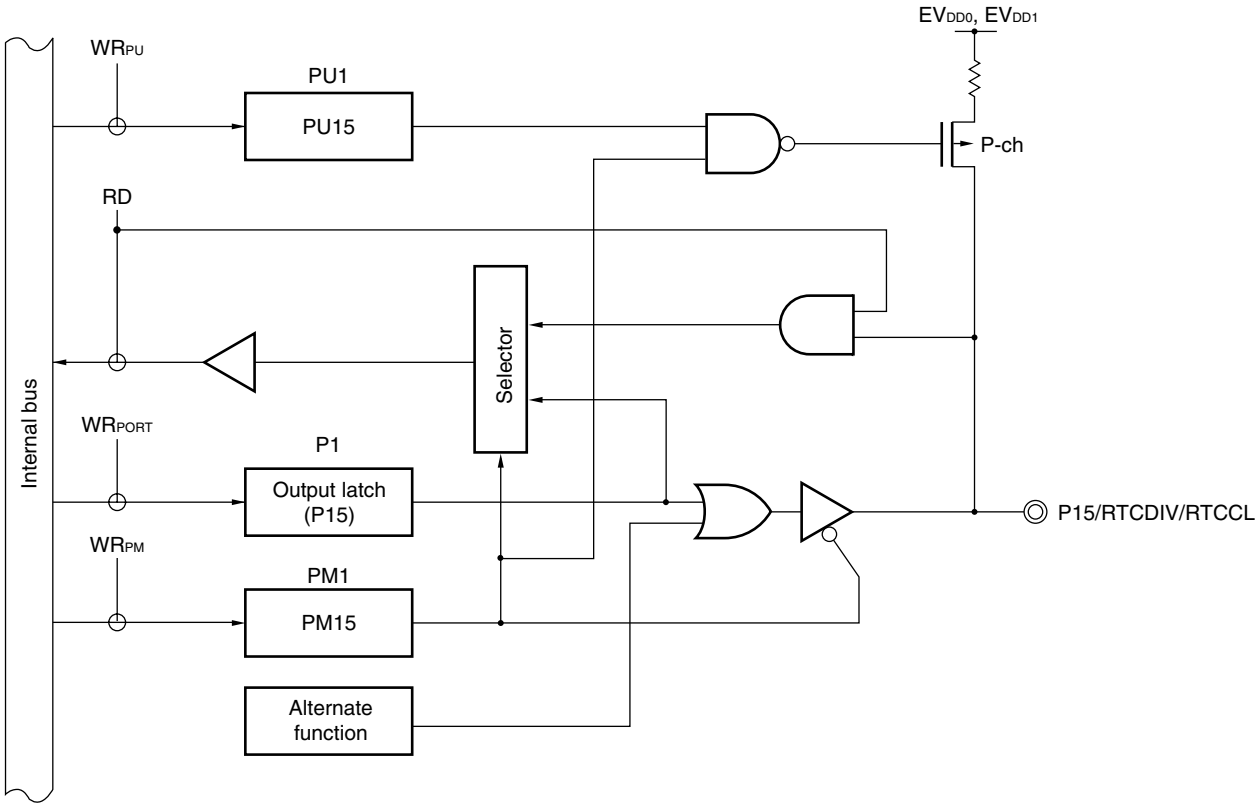
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 6-10. Block Diagram of P14



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

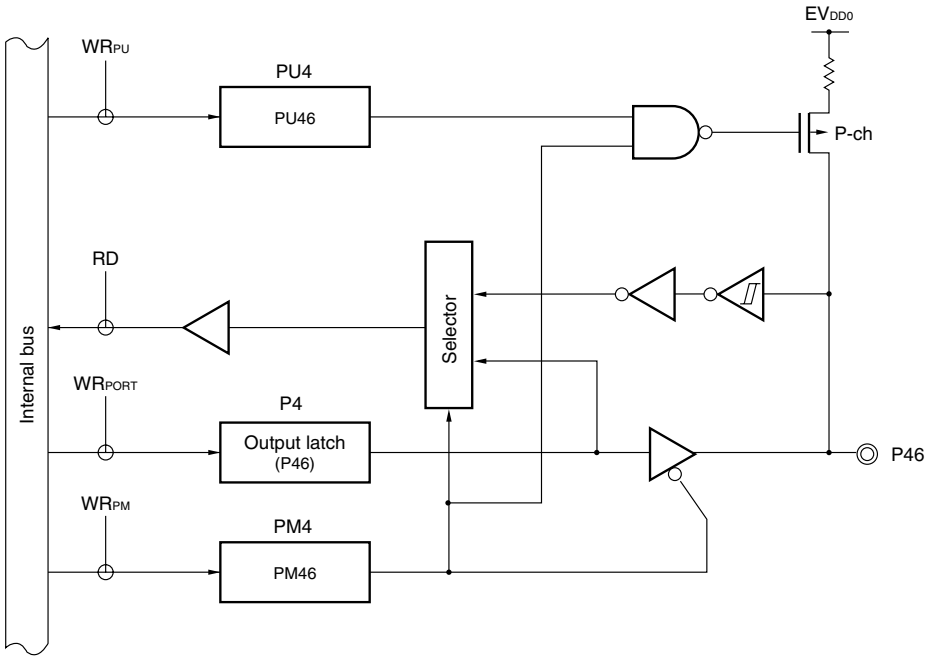
Figure 6-11. Block Diagram of P15



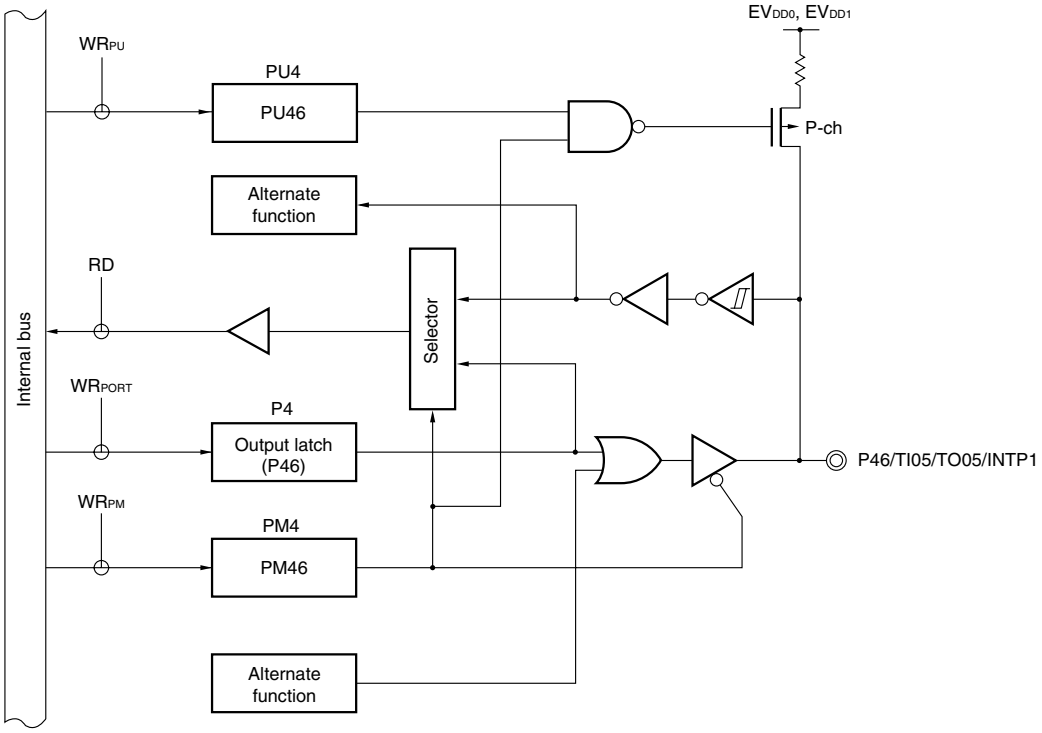
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 6-21. Block Diagram of P46

[78K0R/KF3-L]



[78K0R/KG3-L]



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

3. The microcontroller operates on the 8 MHz internal high-speed oscillation clock if 8 MHz or 20 MHz is selected for the internal high-speed oscillator by using the option byte or on the 1 MHz internal high-speed oscillation clock if 1 MHz is selected.

4. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

5. If the internal high-speed oscillator is set to 1 MHz by using the option byte, the 20 MHz internal high-speed oscillation clock cannot be used.

Cautions 1. A voltage stabilization time (about 2.12 to 5.84 ms) is required after the supply voltage reaches 1.61 V (TYP.). If the time for the supply voltage to rise from 1.61 V (TYP.) to 2.07 V (TYP.) is shorter than the voltage stabilization time, reset processing is entered after the voltage stabilization time elapses.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Table 7-4 shows transition of the CPU clock and examples of setting the SFR registers.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (1/6)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			CSC Register	OSMC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH	MSTOP	FSEL		MCM0
(A) → (B) → (C) (X1 clock: 2 MHz ≤ fx ≤ 10 MHz)	0	1	0	0	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	0	1	1	0	1 Note 2	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	0	0/1 Note 2	Must not be checked	1

Notes 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

2. FSEL = 1 when f_{CLK} > 10 MHz
If a divided clock is selected and f_{CLK} ≤ 10 MHz, use with FSEL = 0 is possible even if fx > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)).

Remark ×: don't care

(3) CPU operating with subsystem clock (D) after reset release (A) (products other than 78K0R/KC3-L (40-pin))

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note			CSC Register	Waiting for Oscillation Stabilization	CKC Register
	OSCSELS	AMPHS1	AMPHS0	XTSTOP		CSS
(A) → (B) → (D)	1	0/1	0/1	0	Necessary	1

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Caution While timer output is enabled (TOEmn = 1), even if the output by timer interrupt of each timer (INTTMmn) contends with writing to the TOmn bit, output is normally done to the TOmn pin.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.5.5 Timer Interrupt and TOmn Pin Output at Operation Start

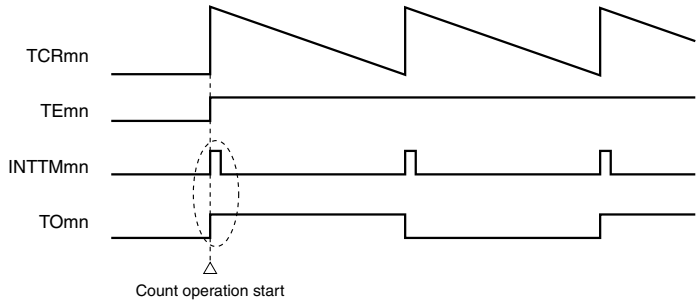
In the interval timer mode or capture mode, the MDmn0 bit in timer mode register mn (TMRmn) sets whether or not to generate a timer interrupt at count start.

When MDmn0 is set to 1, the count operation start timing can be known by the timer interrupt (INTTMmn) generation.

In the other modes, neither timer interrupt at count operation start nor TOmn output is controlled.

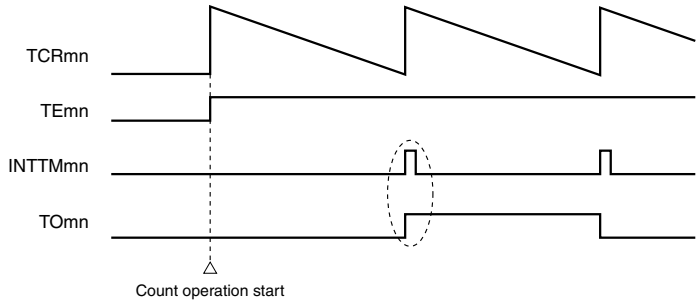
Figures 8-37 and 8-38 show operation examples when the interval timer mode (TOEmn = 1, TOMmn = 0) is set.

Figure 8-38. When MDmn0 is set to 1



When MDmn0 is set to 1, a timer interrupt (INTTMmn) is output at count operation start, and TOmn performs a toggle operation.

Figure 8-39. When MDmn0 is set to 0



When MDmn0 is set to 0, a timer interrupt (INTTMmn) is not output at count operation start, and TOmn does not change either. After counting one cycle, INTTMmn is output and TOmn performs a toggle operation.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-60. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Clears the TOEmn bit to 0 and stops operation of TOmn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the TImn pin start edge detection wait status is set.
	Detects the TImn pin input count start valid edge. →	Clears timer/counter register mn (TCRmn) to 0000H and starts counting up.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to timer data register mn (TDRmn) and INTTMmn is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. The TCRmn register stops the count operation until the next TImn pin start edge is detected.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0. Note →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

13.4.2 Input voltage and conversion results

The relationship between the analog input voltage input to the analog input pins (ANI0 to ANI15, PGAI) and the theoretical A/D conversion result (stored in the 10-bit A/D conversion result register (ADCR)) is shown by the following expression.

$$SAR = INT\left(\frac{V_{AIN}}{AV_{REF}} \times 1024 + 0.5\right)$$

$$ADCR = SAR \times 64$$

or

$$\left(\frac{ADCR}{64} - 0.5\right) \times \frac{AV_{REF}}{1024} \leq V_{AIN} < \left(\frac{ADCR}{64} + 0.5\right) \times \frac{AV_{REF}}{1024}$$

where, INT( ): Function which returns integer part of value in parentheses

V_{AIN}: Analog input voltage

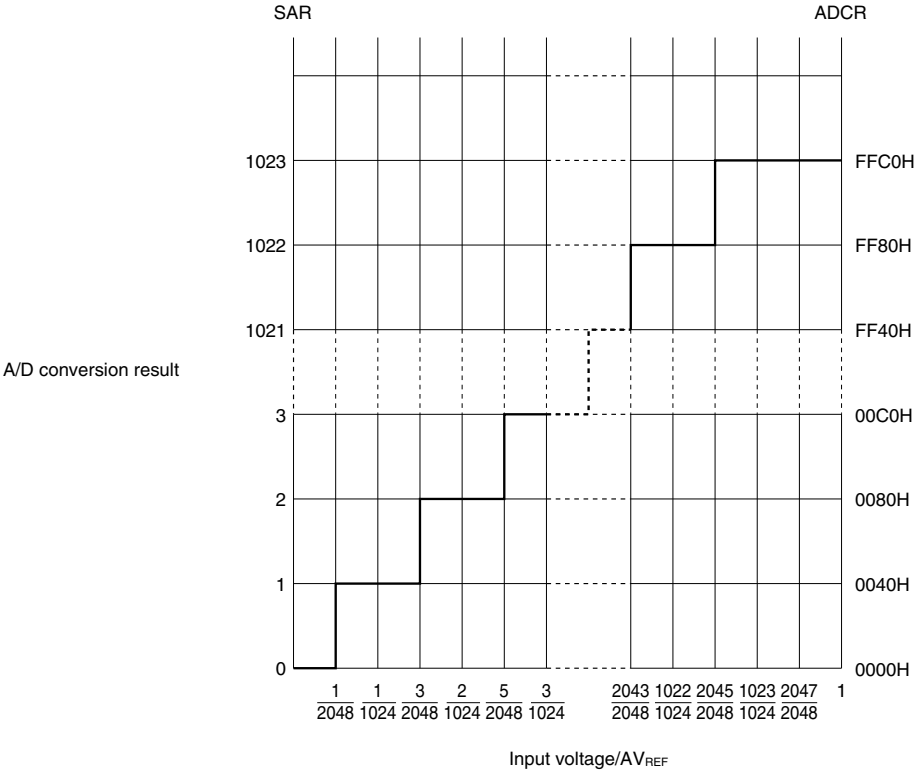
AV_{REF}: AV_{REF} pin voltage

ADCR: A/D conversion result register (ADCR) value

SAR: Successive approximation register

Figure 13-13 shows the relationship between the analog input voltage and the A/D conversion result.

Figure 13-13. Relationship Between Analog Input Voltage and A/D Conversion Result



Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

The channels supporting 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) are channels 0 to 2 of SAU0, channel 0 of SAU1 (78K0R/KF3-L, 78K0R/KG3-L only), and channel 0 and 1 of SAU2 (78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030) only).

- 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0 (supporting LIN-bus)	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–

- 78K0R/KF3-L, 78K0R/KG3-L

Unit	Channel	Used as CSI	Used as UART	Used as Simplified I^2C
0	0	CSI00	UART0	–
	1	CSI01		–
	2	CSI10	UART1	IIC10
	3	–		–
1	0	CSI20	UART2	IIC20
	1	–		–
	2	–	UART3 (supporting LIN-bus)	–
	3	–		–
2 Note	0	CSI40	UART4	–
	1	CSI41		–

Note Serial array unit 2 is only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) performs the following six types of communication operations.

- Master transmission (See **14.5.1**.)
- Master reception (See **14.5.2**.)
- Master transmission/reception (See **14.5.3**.)
- Slave transmission (See **14.5.4**.)
- Slave reception (See **14.5.5**.)
- Slave transmission/reception (See **14.5.6**.)

(8) Port mode register 6 (PM6)

This register sets the input/output of port 6 in 1-bit units.

When using the P60/SCL0 pin as clock I/O and the P61/SDA0 pin as serial data I/O, clear PM60 and PM61, and the output latches of P60 and P61 to 0.

Set the IICE bit (bit 7 of IICA control register 0 (IICCTL0)) to 1 before setting the output mode because the P60/SCL0 and P61/SDA0 pins output a low level (fixed) when the IICE bit is 0.

The PM6 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to FFH.

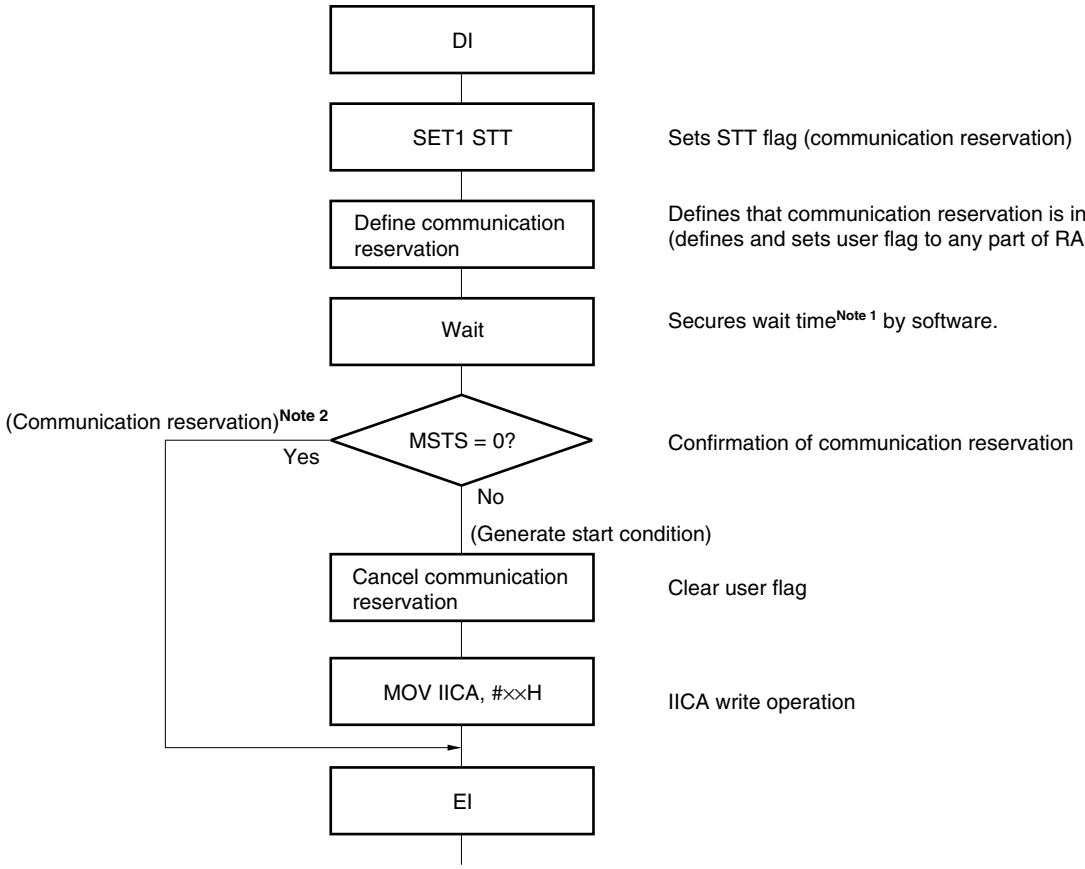
Figure 15-12. Format of Port Mode Register 6 (PM6)

Address: FFF26H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM6	1	1	1	1	1	1	PM61	PM60

PM6n	P6n pin I/O mode selection (n = 0, 1)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Figure 15-27. Communication Reservation Protocol



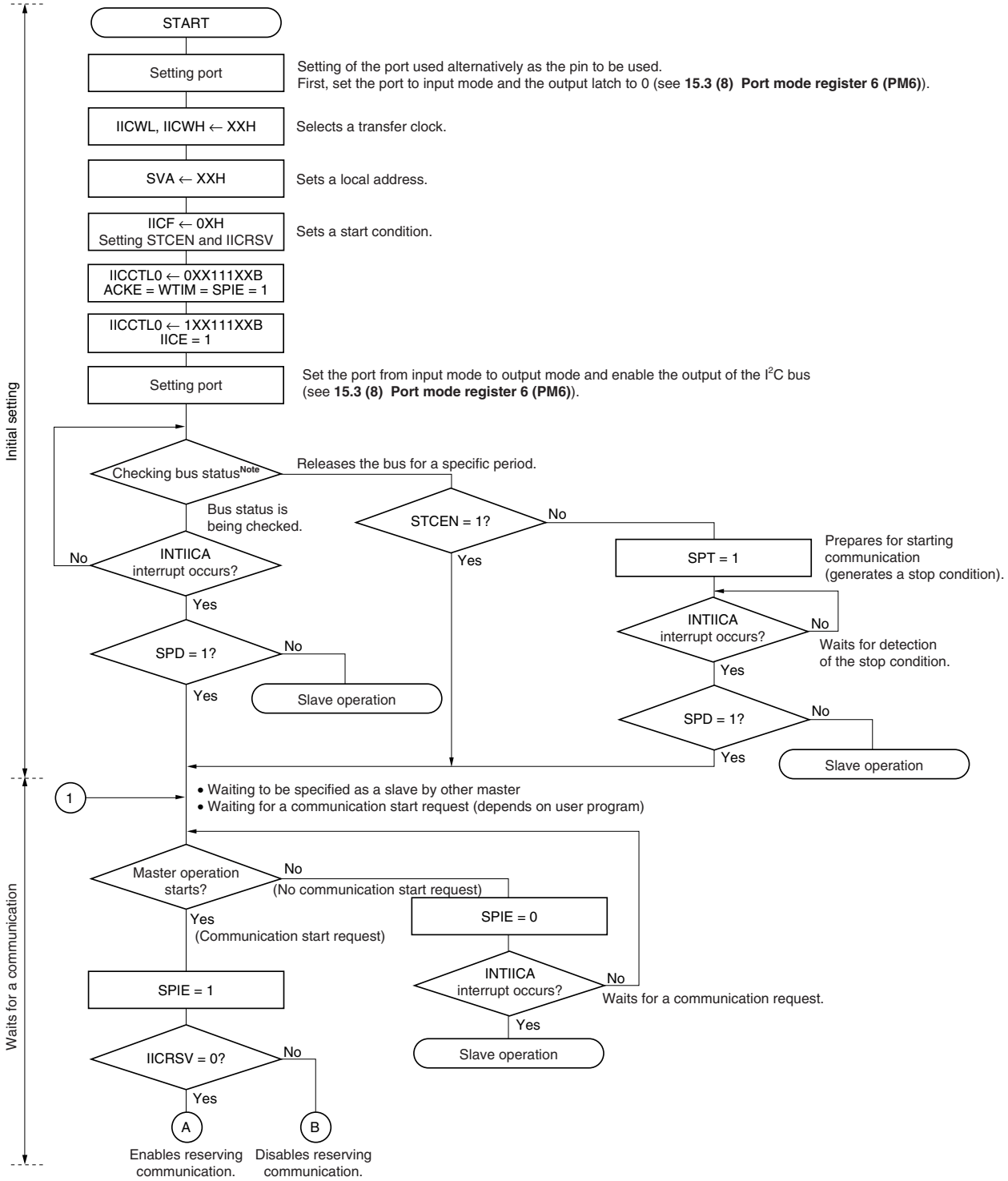
Notes 1. The wait time is calculated as follows.
(IICWL setting value + IICWH setting value + 4) + $t_F \times 2 \times f_{CLK}$ [clocks]

2. The communication reservation operation executes a write to the IICA shift register (IICA) when a stop condition interrupt request occurs.

Remark STT: Bit 1 of IICA control register 0 (IICCTL0)
MSTS: Bit 7 of IICA status register (IICS)
IICA: IICA shift register
IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

(2) Master operation in multi-master system

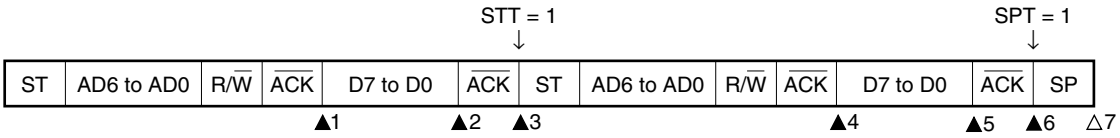
Figure 15-29. Master Operation in Multi-Master System (1/3)



Note Confirm that the bus is released (CLD bit = 1, DAD bit = 1) for a specific period (for example, for a period of one frame). If the SDA0 pin is constantly at low level, decide whether to release the I²C bus (SCL0 and SDA0 pins = high level) in conformance with the specifications of the product that is communicating.

(b) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

(i) When WTIM = 0

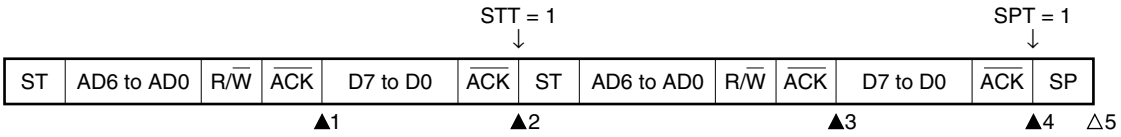


▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets the WTIM bit to 1)[Note 1]
▲3: IICS = 1000××00B (Clears the WTIM bit to 0[Note 2], sets the STT bit to 1)
▲4: IICS = 1000×110B
▲5: IICS = 1000×000B (Sets the WTIM bit to 1)[Note 3]
▲6: IICS = 1000××00B (Sets the SPT bit to 1)
△7: IICS = 00000001B

Notes 1. To generate a start condition, set the WTIM bit to 1 and change the timing for generating the INTIICA interrupt request signal.
2. Clear the WTIM bit to 0 to restore the original setting.
3. To generate a stop condition, set the WTIM bit to 1 and change the timing for generating the INTIICA interrupt request signal.

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

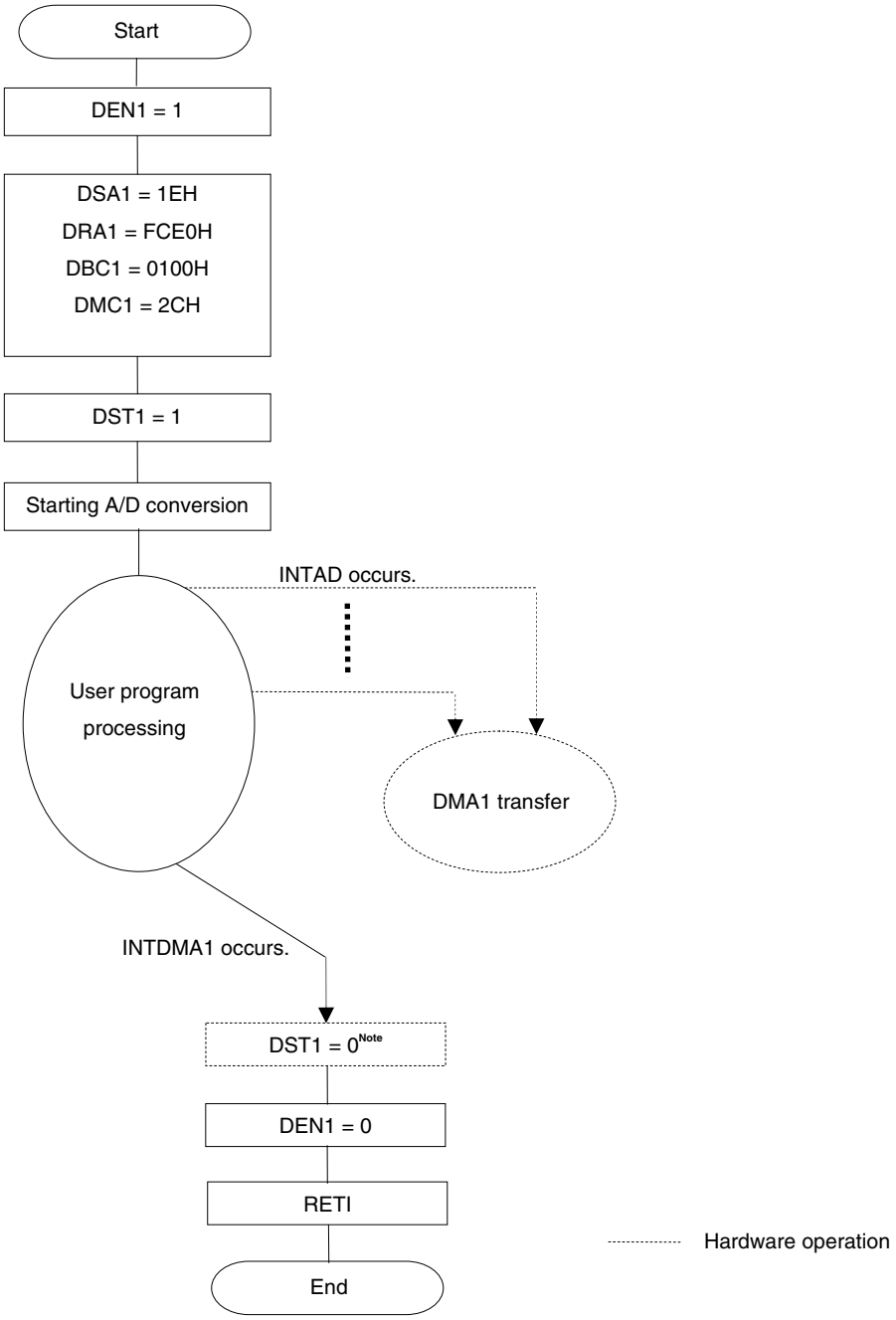
(ii) When WTIM = 1



▲1: IICS = 1000×110B
▲2: IICS = 1000××00B (Sets the STT bit to 1)
▲3: IICS = 1000×110B
▲4: IICS = 1000××00B (Sets the SPT bit to 1)
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

Figure 17-8. Example of Setting of Consecutively Capturing A/D Conversion Results



Note The DST1 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN1 flag is enabled only when DST1 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA1 (INTDMA1), set the DST1 bit to 0 and then the DEN1 bit to 0 (for details, refer to **17.5.5 Forced termination by software**).

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +50°C	V_{DD} = 5.0 V		0.9	2.9	μA
				V_{DD} = 3.0 V		0.9	2.9	μA
				V_{DD} = 2.0 V		0.9	2.9	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +70°C	V_{DD} = 5.0 V		0.9	4.8	μA
				V_{DD} = 3.0 V		0.9	4.8	μA
				V_{DD} = 2.0 V		0.9	4.8	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +85°C	V_{DD} = 5.0 V		0.9	7.1	μA
				V_{DD} = 3.0 V		0.9	7.1	μA
				V_{DD} = 2.0 V		0.9	7.1	μA
	I_{DD3} Note 3	STOP mode	T_A = –40 to +50°C			0.33	2.1	μA
			T_A = –40 to +70°C			0.33	4	μA
			T_A = –40 to +85°C			0.33	6.2	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current. However, not including the current flowing into the A/D converter, programmable gain amplifier, comparator, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution in flash memory.

2. When operating real-time counter (RTC) and setting ultra-low current consumption (AMPHS1 (bit2 of CMC register) = 1, OSMC = 82H).When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped. When watchdog timer is stopped. When RTCLPC = 1 (stops supply of subsystem clock to peripheral functions other than real-time counter). When output function of RTC is stopped.

3. Total current flowing into V_{DD}, EV_{DD}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current. However, not including the current flowing into the A/D converter, programmable gain amplifier, comparator, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. When subsystem clock is stopped. When watchdog timer is stopped.

Remarks 1. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. RTCLPC: bit 7 of the operation speed mode control register (OSMC)

3. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note	kHz
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1200		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1500		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK}+120		ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK}+230		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	660	ns
		1.8 V ≤ V_{DD} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	710	ns

Note The value must also be f_{MCK}/4 or more.

Simplified I^2C mode mode connection diagram (during communication at same potential)