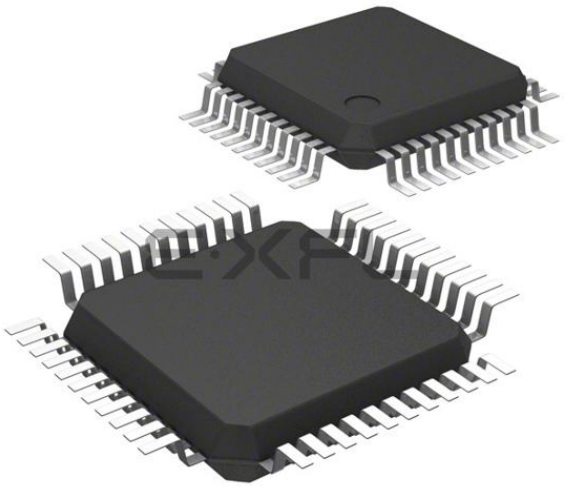
Renesas Electronics America Inc - UPD78F1003GB-GAF-AX Datasheet



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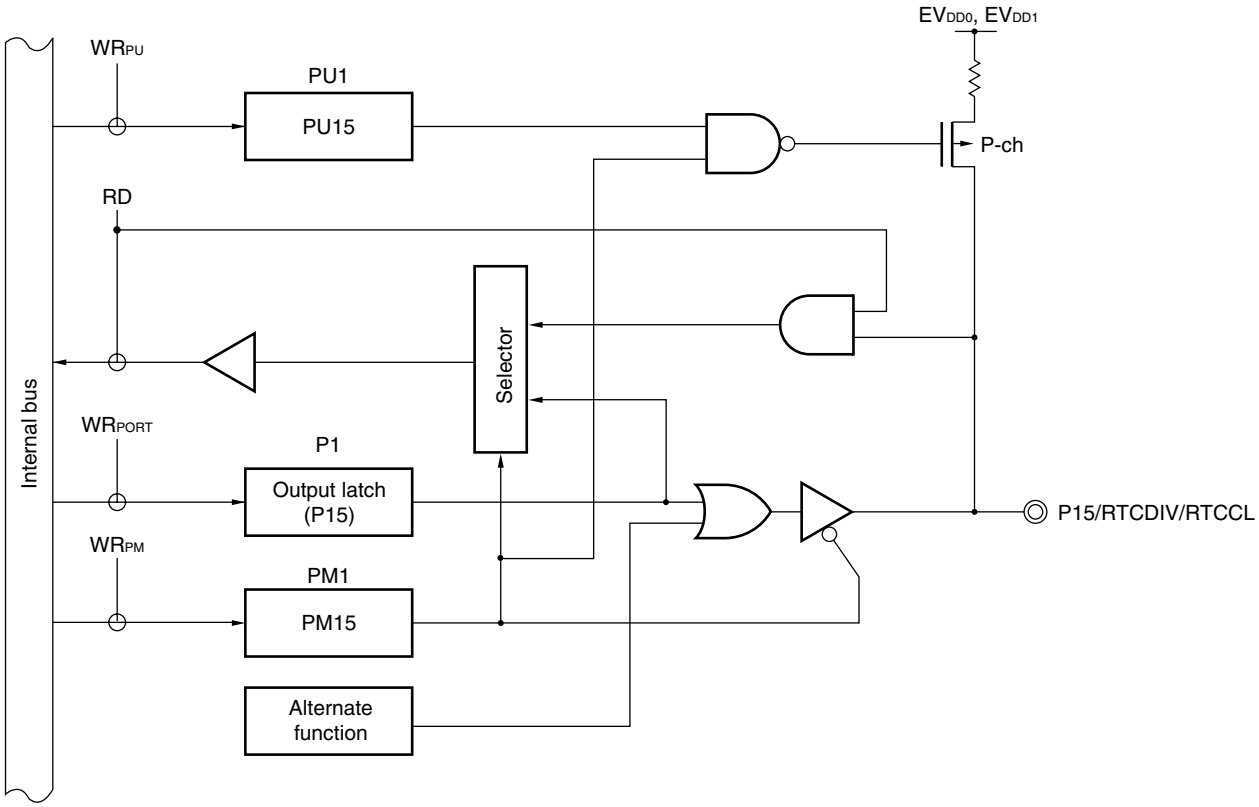
Applications of "Embedded - Microcontrollers"

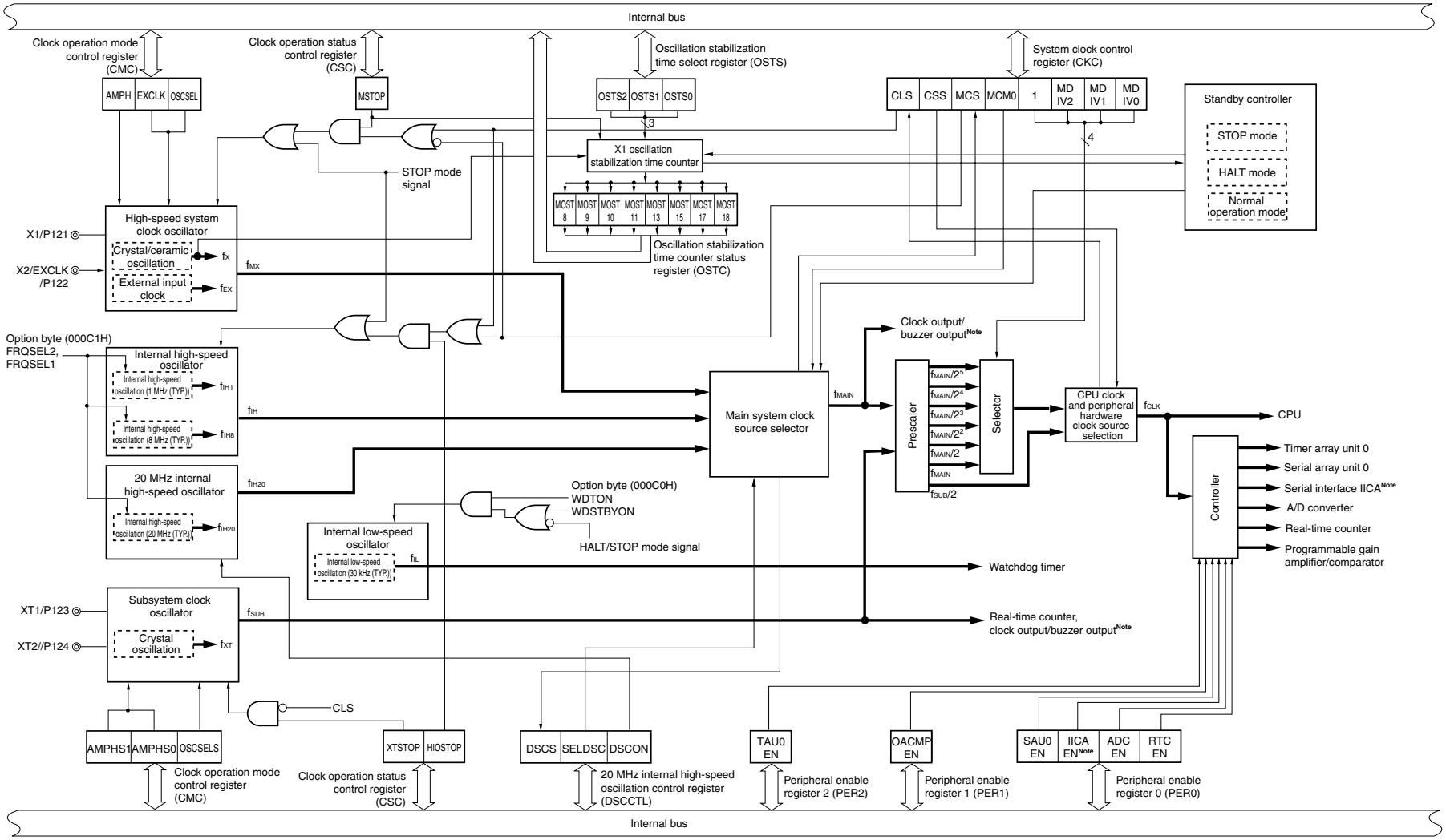
Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1003gb-gaf-ax

Figure 6-11. Block Diagram of P15



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 7-2. Block Diagram of Clock Generator (78K0R/KC3-L (44-pin and 48-pin), 78K0R/KD3-L, 78K0R/KE3-L)

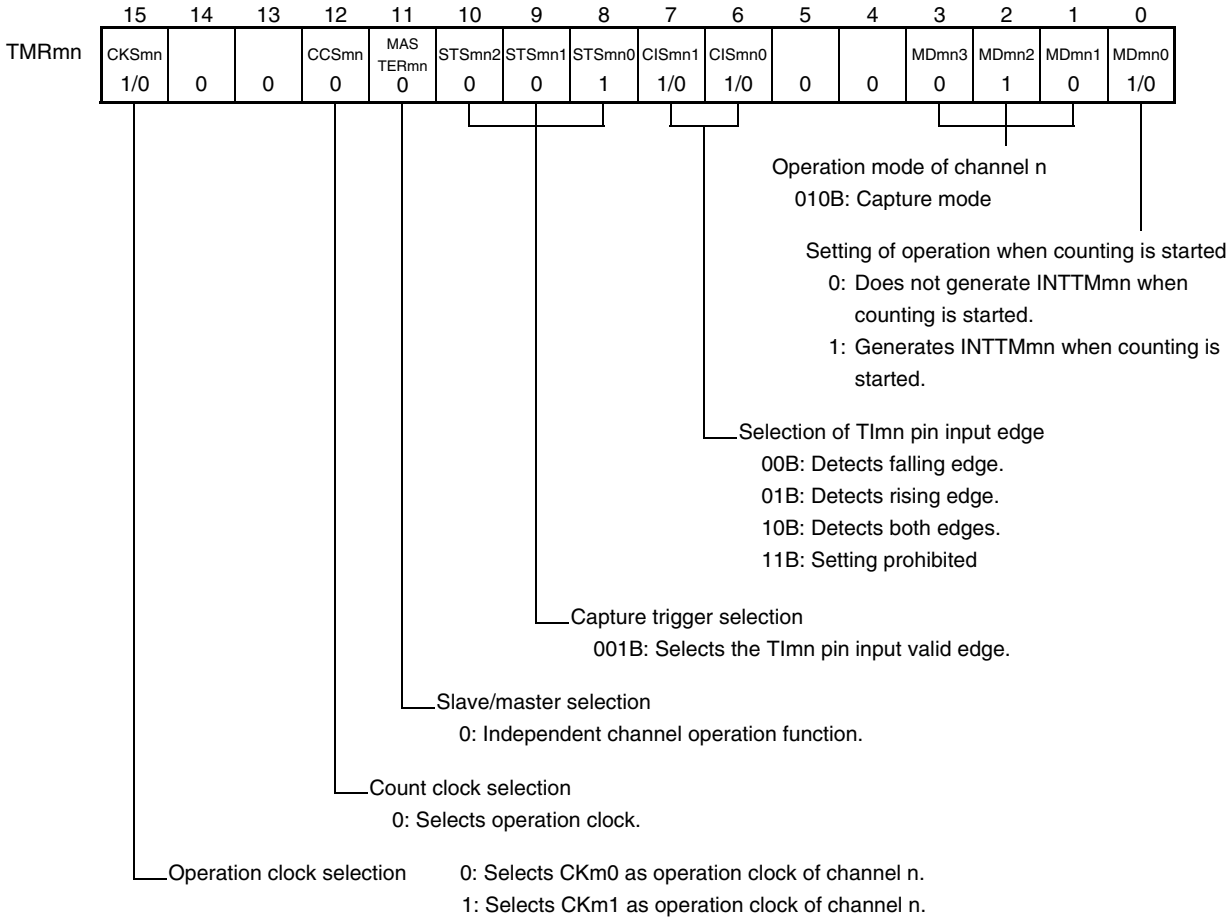


Note This is not mounted onto 44-pin product of the 78K0R/KC3-L.

(**Remark** is listed on the next page after next.)

Figure 8-55. Example of Set Contents of Registers to Measure Input Pulse Interval

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn	0: Outputs 0 from TOmn.
	0	

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn	0: Stops TOmn output operation by counting operation.
	0	

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (master channel output mode).
	0	

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets master channel output mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 9-3. Format of Real-Time Counter Control Register 0 (RTCC0)

Address: FFF9DH After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	2	1	0
RTCC0	RTCE	0	RCLOE1	RCLOE0	AMPM	CT2	CT1	CT0

RTCE	Real-time counter operation control
0	Stops counter operation.
1	Starts counter operation.

RCLOE1	RTC1HZ pin output control
0	Disables output of the RTC1HZ pin (1 Hz).
1	Enables output of the RTC1HZ pin (1 Hz).

RCLOE0[Note]	RTCCL pin output control
0	Disables output of the RTCCL pin (32.768 kHz).
1	Enables output of the RTCCL pin (32.768 kHz).

AMPM	Selection of 12-/24-hour system
0	12-hour system (a.m. and p.m. are displayed.)
1	24-hour system
• Rewrite the AMPM bit value after setting the RWAIT bit (bit 0 of real-time counter control register 1 (RTCC1)) to 1. If the AMPM bit value is changed, the values of the hour count register (HOUR) change according to the specified time system. • Table 9-2 shows the displayed time digits that are displayed.	

CT2	CT1	CT0	Constant-period interrupt (INTRTC) selection
0	0	0	Does not use constant-period interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
0	1	0	Once per 1 s (same time as second count up)
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	×	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)
When changing the values of the CT2 to CT0 bits while the counter operates (RTCE = 1), rewrite the values of the CT2 to CT0 bits after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, after rewriting the values of the CT2 to CT0 bits, enable interrupt servicing after clearing the RIFG and RTCIF flags.			

Note The RCLOE0 and RCLOE2 bits must not be enabled at the same time.

Caution If the RCLOE0 and RCLOE1 bits are changed when RTCE = 1, the last waveform of the 32.768 kHz and 1 Hz output signals may become short.

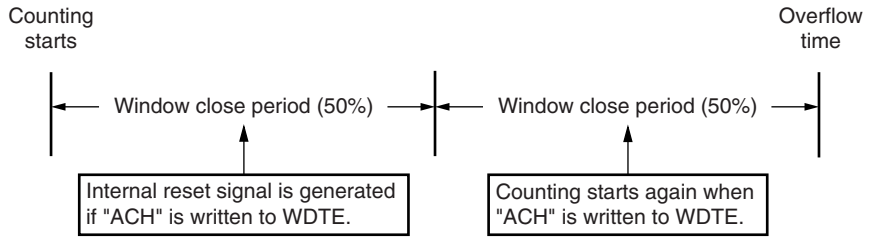
Remark ×: don't care

12.4.3 Setting window open period of watchdog timer

Set the window open period of the watchdog timer by using bits 6 and 5 (WINDOW1, WINDOW0) of the option byte (000C0H). The outline of the window is as follows.

- If “ACH” is written to the watchdog timer enable register (WDTE) during the window open period, the watchdog timer is cleared and starts counting again.
- Even if “ACH” is written to the WDTE register during the window close period, an abnormality is detected and an internal reset signal is generated.

Example: If the window open period is 50%



Caution When data is written to the WDTE register for the first time after reset release, the watchdog timer is cleared in any timing regardless of the window open time, as long as the register is written before the overflow time, and the watchdog timer starts counting again.

The window open period can be set is as follows.

Table 12-4. Setting Window Open Period of Watchdog Timer

WINDOW1	WINDOW0	Window Open Period of Watchdog Timer
0	0	Setting prohibited
0	1	50%
1	0	75%
1	1	100%

Cautions 1. The watchdog timer continues its operation during self-programming of the flash memory and EEPROM emulation. During processing, the interrupt acknowledge time is delayed. Set the overflow time and window size taking this delay into consideration.

2. When bit 0 (WDSTBYON) of the option byte (000C0H) = 0, the window open period is 100% regardless of the values of the WINDOW1 and WINDOW0 bits.

(11) Internal equivalent circuit

The equivalent circuit of the analog input block is shown below.

Figure 13-24. Internal Equivalent Circuit of ANIn Pin

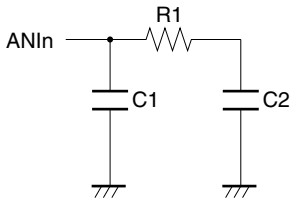


Table 13-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

AV_{REF}	Mode	R1	C1	C2
4.0 V ≤ V_{DD} ≤ 5.5 V	Normal	5.2 kΩ	8 pF	6.3 pF
	High speed 1	5.2 kΩ		
	High speed 2	7.8 kΩ		
2.7 V ≤ V_{DD} < 4.0 V	Normal	18.6 kΩ		
	High speed 2	7.8 kΩ		
1.8 V ≤ V_{DD} < 4.0 V	Low-voltage	169.8 kΩ		

Remarks 1. The resistance and capacitance values shown in Table 13-4 are not guaranteed values.

2. 78K0R/KC3-L (40-pin, 44-pin): n = 0 to 9
78K0R/KC3-L (48-pin), 78K0R/KD3-L: n = 0 to 10
78K0R/KE3-L, 78K0R/KF3-L: n = 0 to 11
78K0R/KG3-L: n = 0 to 15

(12) Starting the A/D converter

Start the A/D converter after the AV_{REF} voltage stabilize.

(9) Serial channel stop register m (STm)

The STm register is a trigger register that is used to enable stopping communication/count by each channel.

When 1 is written a bit of this register (STmn), the corresponding bit (SEmn) of serial channel enable status register m (SEm) is cleared to 0 (operation is stopped). Because the STmn bit is a trigger bit, it is cleared immediately when SEmn = 0.

The STm register can set written by a 16-bit memory manipulation instruction.

The lower 8 bits of the STm register can be set with an 1-bit or 8-bit memory manipulation instruction with STmL.

Reset signal generation clears the STm register to 0000H.

Figure 14-13. Format of Serial Channel Stop Register m (STm)

Address: F0124H, F0125H (ST0), F0164H, F0165H (ST1) After reset: 0000H R/W
F0214H, F0215H (ST2)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STm	0	0	0	0	0	0	0	0	0	0	0	0	STm3 Note 1	STm2 Note 1	STm1	STm0

STmn	Operation stop trigger of channel n
0	No trigger operation
1	Clears the SEmn bit to 0 and stops the communication operation Note 2.

Notes 1. Those bits are invalid while operating serial allay unit 2.

2. Communication stops while holding the value of the control register and shift register, and the status of the serial clock I/O pin, serial data output pin, and each error flag (FEFmn: framing error flag, PEFmn: parity error flag, OVFmn: overrun error flag).

Caution Be sure to clear bits 15 to 4 to "0".

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03
78K0R/KF3-L□μPD78F1010, 78F1011, 78F1012□: mn = 00 to 03, 10 to 13
78K0R/KF3-L□μPD78F1027, 78F1028□: mn = 00 to 03, 10 to 13, 20, 21
78K0R/KG3-L□μPD78F1013, 78F1014□: mn = 00 to 03, 10 to 13
78K0R/KG3-L□μPD78F1029, 78F1030□: mn = 00 to 03, 10 to 13, 20, 21

2. When the STm register is read, 0000H is always read.

Figure 14-60. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)

(e) Serial output enable register m (SOEm) …The Register that not used in this mode.

<R>

SOEm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	SOEm2 ×	SOEm1 ×	SOEm0 ×

(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.

<R>

SSm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	SSm3 ×	SSm2 0/1 Note 2	SSm1 0/1	SSm0 0/1

Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

Remarks 1. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

2. □ : Setting is fixed in the CSI master transmission mode, ■ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

(3) IICA status register (IICS)

This register indicates the status of I^2C.

The IICS register is read by a 1-bit or 8-bit memory manipulation instruction only when STT = 1 and during the wait period.

Reset signal generation clears this register to 00H.

Caution Reading the IICS register while the address match wakeup function is enabled (WUP = 1) in STOP mode is prohibited. When the WUP bit is changed from 1 to 0 (wakeup operation is stopped), regardless of the INTIICA interrupt request, the change in status is not reflected until the next start condition or stop condition is detected. To use the wakeup function, therefore, enable (SPIE = 1) the interrupt generated by detecting a stop condition and read the IICS register after the interrupt has been detected.

Remark STT: bit 1 of IICA control register 0 (IICCTL0)
WUP: bit 7 of IICA control register 1 (IICCTL1)

Figure 15-7. Format of IICA Status Register (IICS) (1/3)

Address: FFF51H After reset: 00H R

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICS	MSTS	ALD	EXC	COI	TRC	ACKD	STD	SPD

MSTS	Master status check flag
0	Slave device status or communication standby status
1	Master device communication status

Condition for clearing (MSTS = 0)	Condition for setting (MSTS = 1)
• When a stop condition is detected • When ALD = 1 (arbitration loss) • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is generated

ALD	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win”.
1	This status indicates the arbitration result was a “loss”. The MSTS bit is cleared.

Condition for clearing (ALD = 0)	Condition for setting (ALD = 1)
• Automatically cleared after the IICS register is read[Note] • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When the arbitration result is a “loss”.

Note This register is also cleared when a 1-bit memory manipulation instruction is executed for bits other than the IICS register. Therefore, when using the ALD bit, read the data of this bit before the data of the other bits.

Remark LREL: Bit 6 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

15.5.14 Communication reservation

(1) When communication reservation function is enabled (bit 0 (IICRSV) of IICA flag register (IICF) = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ is not returned and the bus was released by setting bit 6 (LREL) of IICA control register 0 (IICCTL0) to 1 and saving communication).

If bit 1 (STT) of the IICCTL0 register is set to 1 while the bus is not used (after a stop condition is detected), a start condition is automatically generated and wait state is set.
If an address is written to the IICA shift register (IICA) after bit 4 (SPIE) of the IICCTL0 register was set to 1, and it was detected by generation of an interrupt request signal (INTIICA) that the bus was released (detection of the stop condition), then the device automatically starts communication as the master. Data written to the IICA register before the stop condition is detected is invalid.
When the STT bit has been set to 1, the operation mode (as start condition or as communication reservation) is determined according to the bus status.

- If the bus has been released ..... a start condition is generated
- If the bus has not been released (standby mode)..... communication reservation

Check whether the communication reservation operates or not by using the MSTS bit (bit 7 of the IICA status register (IICS)) after the STT bit is set to 1 and the wait time elapses.
Use software to secure the wait time calculated by the following expression.

Wait time from setting STT = 1 to checking the MSTS flag: (IICWL setting value + IICWH setting value + 4) + $t_F \times 2 \times f_{CLK}$ [clocks]

Remark IICWL: IICA low-level width setting register
IICWH: IICA high-level width setting register
t_F: SDA0 and SCL0 signal falling times
f_{CLK}: CPU/peripheral hardware clock frequency

CHAPTER 16 MULTIPLIER/DIVIDER

16.1 Functions of Multiplier/Divider

The multiplier/divider has the following functions.

- 16 bits × 16 bits = 32 bits (multiplication)
- 32 bits ÷ 32 bits = 32 bits, 32-bit remainder (division)

16.2 Configuration of Multiplier/Divider

The multiplier/divider consists of the following hardware.

Table 16-1. Configuration of Multiplier/Divider

Item	Configuration
Registers	Multiplication/division data register A (L) (MDAL) Multiplication/division data register A (H) (MDAH) Multiplication/division data register B (L) (MDBL) Multiplication/division data register B (H) (MDBH) Multiplication/division data register C (L) (MDCL) Multiplication/division data register C (H) (MDCH)
Control register	Multiplication/division control register (MDUC)

Figure 16-1 shows a block diagram of the multiplier/divider.

16.4.2 Division operation

- Initial setting
  - <1> Set bit 7 (DIVMODE) of the multiplication/division control register (MDUC) to 1.
  - <2> Set the dividend (higher 16 bits) to multiplication/division data register A (H) (MDAH).
  - <3> Set the dividend (lower 16 bits) to multiplication/division data register A (L) (MDAL).
  - <4> Set the divisor (higher 16 bits) to multiplication/division data register B (H) (MDBH).
  - <5> Set the divisor (lower 16 bits) to multiplication/division data register B (L) (MDBL).
  - <6> Set bit 0 (DIVST) of the MDUC register to 1.

    (There is no preference in the order of executing steps <2> to <5>.)
- During operation processing
  - <7> The operation will end when one of the following processing is completed.
    - A wait of at least 16 clocks (The operation will end when 16 clocks have been issued.)
    - A check whether the DIVST bit has been cleared
    - Generation of a division completion interrupt (INTMD)

    (The read values of the MDBL, MDBH, MDCL, and MDCH registers during operation processing are not guaranteed.)
- Operation end
  - <8> The DIVST bit is cleared (0) and an interrupt request signal (INTMD) is generated (end of operation).
  - <9> Read the quotient (lower 16 bits) from the MDAL register.
  - <10> Read the quotient (higher 16 bits) from the MDAH register.
  - <11> Read the remainder (lower 16 bits) from multiplication/division data register C (L) (MDCL).
  - <12> Read the remainder (higher 16 bits) from multiplication/division data register C (H) (MDCH).

    (There is no preference in the order of executing steps <9> to <12>.)
- Next operation
  - <13> To execute multiplication operation next, start from the “Initial setting” in **16.4.1 Multiplication operation**.
  - <14> To execute division operation next, start from the “Initial setting” for division operation.

Remark Steps <1> to <12> correspond to <1> to <12> in Figure 16-7.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(3) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V		6/f_{MCK}			ns
		1.8 V ≤ V_{DD} < 4.0 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}			t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			80			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK}+50			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	C = 30 pF[Note 4]	4.0 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK}+45	ns
			2.7 V ≤ V_{DD} < 4.0 V			2/f_{MCK}+57	ns
			1.8 V ≤ V_{DD} < 2.7 V			2/f_{MCK}+125	ns

Notes 1. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

2. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

3. When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0.

4. C is the load capacitance of the SOp output lines.

Caution Select the normal input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10), g: PIM and POM number (g = 3, 7)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of the SMR0n register. n: Channel number (n = 0 to 2))

CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)

Cautions 1. The 78K0R/KF3-L, 78K0R/KG3-L have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. The pins mounted are as follows according to product.

31.1 Pins Mounted According to Product

31.1.1 Port functions

Port	78K0R/KF3-L		78K0R/KG3-L	
	μPD78F10xx : xx = 10, 11, 12	μPD78F10xx : xx = 27, 28	μPD78F10xx : xx = 13, 14	μPD78F10xx : xx = 29, 30
Port 0	P02 to P06		P00 to P06	
Port 1	P10 to P17			
Port 2	P20 to P27			
Port 3	P30, P31			
Port 4	P40 to P47			
Port 5	P50 to P55		P50 to P57	
Port 6	P60 to P67			
Port 7	P70 to P77			
Port 8	–		P80 to P87	
Port 9	P90, P91		P91	
Port 11	P110, P111			
Port 12	P120 to P124			
Port 13	P130		P130, P131	
Port 14	P140, P142 to P144		P140 to P145	
Port 15	P150 to P153		P150 to P157	

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Square wave input		1.2	3.6	mA
				Resonator connection		1.5	3.9	mA
			f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Square wave input		1.2	3.6	mA
				Resonator connection		1.5	3.9	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 5.0 V	Square wave input		0.55	2.1	mA
				Resonator connection		0.65	2.2	mA
			f_{MX} = 10 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		0.55	2.1	mA
				Resonator connection		0.65	2.2	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 3.0 V	Square wave input		0.40	1.8	mA
				Resonator connection		0.45	1.8	mA
			f_{MX} = 5 MHz Notes 2, 3, V_{DD} = 2.0 V	Square wave input		0.28	1.3	mA
				Resonator connection		0.33	1.4	mA
			f_{IH20} = 20 MHz Note 4	V_{DD} = 5.0 V		1.4	3.9	mA
				V_{DD} = 3.0 V		1.4	3.9	mA
			f_{IH} = 8 MHz Note 4	V_{DD} = 5.0 V		0.48	1.8	mA
				V_{DD} = 3.0 V		0.48	1.8	mA
			f_{IH} = 1 MHz Note 4, 5	V_{DD} = 3.0 V		50	168	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value include the peripheral operation current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When internal high-speed oscillator, 20 MHz internal high-speed oscillator, and subsystem clock are stopped.

3. When AMPH (bit 0 of clock operation mode control register (CMC)) = 0, FLPC and FSEL (bits 1 and 0 of operation speed mode control register (OSMC)) = 0 and 0.

4. When high-speed system clock and subsystem clock are stopped.

5. When low consumption current mode is set (RMC = 5AH, OSMC = 02H).

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH20}: 20 MHz internal high-speed oscillation clock frequency

3. f_{IH}: Internal high-speed oscillation clock frequency

4. RMC: Regulator mode control register (RMC)

5. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Real-time counter operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz		V_{DD} = 3.0 V		0.2	1.0	μA
				V_{DD} = 2.0 V		0.2	1.0	
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 30 kHz				0.31	0.35	μA
A/D converter operating current	I_{ADC} Note 4	During conversion at maximum speed	High speed mode 1	AV_{REF} = V_{DD} = 5.0 V		1.72	3.2	mA
			High speed mode 2	AV_{REF} = V_{DD} = 3.0 V		0.72	1.6	mA
			Normal mode	AV_{REF} = V_{DD} = 5.0 V		0.86	1.9	mA
			Low voltage mode	AV_{REF} = V_{DD} = 3.0 V		0.37	0.8	mA
LVI operating current	I_{LVI} Note 5					9	18	μA

Notes 1. Current flowing only to the real-time counter (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time counter operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time counter operating current. When the real-time counter operates during f_{CLK} = f_{SUB}/2, the TYP. value of I_{DD2} includes the real-time counter operating current.

2. When internal high-speed oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 30 kHz internal oscillator). The current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates during f_{CLK} = f_{SUB}/2 or STOP mode.

4. Current flowing only to the A/D converter (AV_{REF} pin). The current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the LVI circuit. The current value of the 78K0R/KF3-L, 78K0R/KG3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the Operating, HALT or STOP mode.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.6.7 LVI circuit characteristics

(T_A = –40 to +85°C, $V_{PDR} \le V_{DD} = EV_{DD0} = EV_{DD1} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

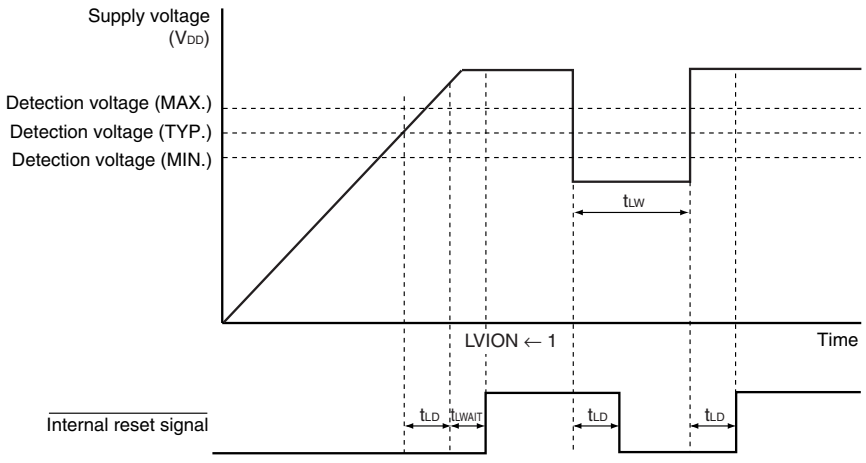
Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVI0}		4.12	4.22	4.32	V
		V_{LVI1}		3.97	4.07	4.17	V
		V_{LVI2}		3.82	3.92	4.02	V
		V_{LVI3}		3.66	3.76	3.86	V
		V_{LVI4}		3.51	3.61	3.71	V
		V_{LVI5}		3.35	3.45	3.55	V
		V_{LVI6}		3.20	3.30	3.40	V
		V_{LVI7}		3.05	3.15	3.25	V
		V_{LVI8}		2.89	2.99	3.09	V
		V_{LVI9}		2.74	2.84	2.94	V
		V_{LVI10}		2.58	2.68	2.78	V
		V_{LVI11}		2.43	2.53	2.63	V
		V_{LVI12}		2.28	2.38	2.48	V
		V_{LVI13}		2.12	2.22	2.32	V
		V_{LVI14}		1.97	2.07	2.17	V
		V_{LVI15}		1.81	1.91	2.01	V
	External input pin[Note 1]	V_{EXLVI}	EXLVI < V_{DD}, 1.8 V ≤ V_{DD} ≤ 5.5 V	1.11	1.21	1.31	V
	Power supply voltage on power application	V_{PUPLVI}	When LVI default start function enabled is set	1.87	2.07	2.27	V
Minimum pulse width		t_{LW}		200			μs
Detection delay time		t_{LD}				200	μs
Operation stabilization wait time[Note 2]		t_{LWAIT}				10	μs

Notes 1. The EXLVI/P120/INTP0 pin is used.

2. Time required from setting bit 7 (LVION) of the low-voltage detection register (LVIM) to 1 to operation stabilization

Remark $V_{LVI(n-1)} > V_{LVIn}$: n = 1 to 15

LVI Circuit Timing



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Edition	Description	Chapter
Current Version (U20024E) 1st edition	Change of **Figure 21-2. Timing of Reset by $\overline{\text{RESET}}$ Input**	CHAPTER 21 RESET FUNCTION
	Change of **Figure 21-4. Timing of Reset in STOP Mode by $\overline{\text{RESET}}$ Input**	
	Change of **Figure 22-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (1/2)**	CHAPTER 22 POWER-ON-CLEAR CIRCUIT
	Change of **Note 4** in **Figure 22-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector (2/2)**	
	Change of **Figure 22-3. Example of Software Processing After Reset Release (1/2)**	
	Change of **Figure 23-11. Example of Software Processing After Reset Release (1/2)**	CHAPTER 23 LOW-VOLTAGE DETECTOR
	Change of **26.3 Communication Mode**, and addition of **Note**	CHAPTER 26 FLASH MEMORY
	Addition of **Note** to **Table 26-5. Communication Modes**	
	Addition of **Remark** to **26.8 Flash Memory Programming by Self-Programming**	
	Change of **Figure 26-16. Flow of Self Programming (Rewriting Flash Memory)**	
	Change of **Table 27-1. Lists the Differences Between 1-line Mode and 2-line Mode.**	CHAPTER 27 ON-CHIP DEBUG FUNCTION
	Change of description in **29.1.4 PREFIX instruction**	CHAPTER 29 INSTRUCTION SET
	Change of **Table 29-5. Operation List**	
	Change of high-level output current conditions, low-level output current conditions, high-level input voltage conditions, low-level input voltage conditions, high-level output voltage conditions, low-level output voltage conditions, high-level input leakage current conditions, and low-level input leakage current conditions in **30.4 DC Characteristics**	CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)
	Change of **30.6.1 (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**	
	Change of **30.6.1 (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**	
	Change of **30.6.1 (4) During communication at same potential (simplified I^2C mode)**	
	Change of **30.6.1 (6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock**	
	Change of **30.6.1 (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**	
	Change of **30.6.1 (8) Communication at different potential (2.5 V, 3 V) (simplified I^2C mode)**	
	Change of **30.6.2 Serial interface IICA**	
	Change of **POC Circuit Timing** in **30.6.7 POC circuit characteristics**	
	Change of **LVI Circuit Timing** in **30.6.9 LVI circuit characteristics**	
	Addition of chapter	CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)