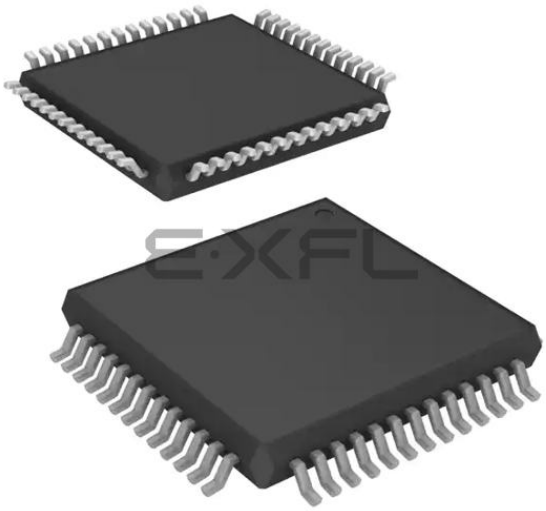
Renesas Electronics America Inc - UPD78F1004GB-GAG-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1004gb-gag-ax

(f) SDA10

This is a serial data I/O pin of serial interface for simplified I^2C.

(g) SCL10

This is a serial clock I/O pin of serial interface for simplified I^2C.

(h) INTP1, INTP2

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

Caution To use P30/SO10/TxD1 and P32/$\overline{\text{SCK10}}$/SCL10/INTP2 as general-purpose ports, set serial communication operation setting register 02 (SCR02) to the default status (0087H). In addition, clear port output mode register 3 (POM3) to 00H.

2.2.5 P40 to P43 (port 4)

P40 to P43 function as an I/O port. These pins also function as data I/O for a flash memory programmer/debugger and clock output.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P40/TOOL0	√		√	√	√
P41/TOOL1	√		√	√	√
P42	–		–	–	√
P43	–		–	–	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P43 function as an I/O port. P40 to P43 can be set to input or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

Be sure to connect an external pull-up resistor to P40 when on-chip debugging is enabled (by using an option byte).

(2) Control mode

P40 to P43 function as data I/O for a flash memory programmer/debugger and clock output.

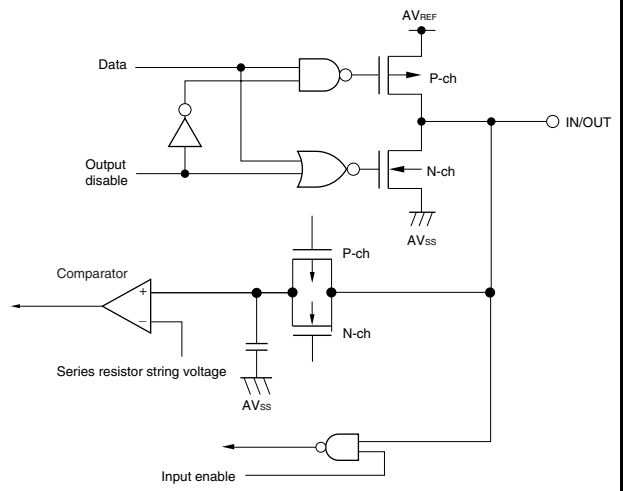
(a) TOOL0

This is a data I/O pin for a flash memory programmer/debugger.

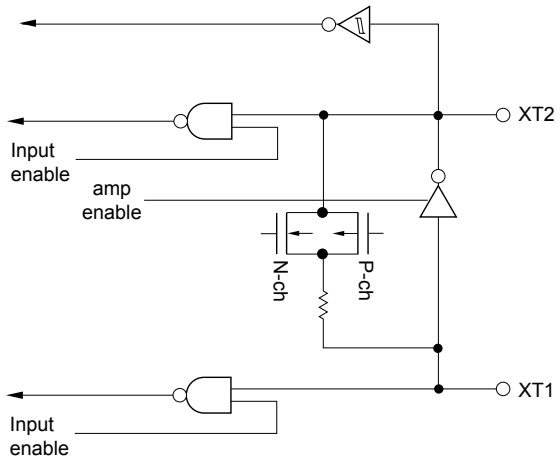
Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).

Figure 3-1. Pin I/O Circuit List (2/2)

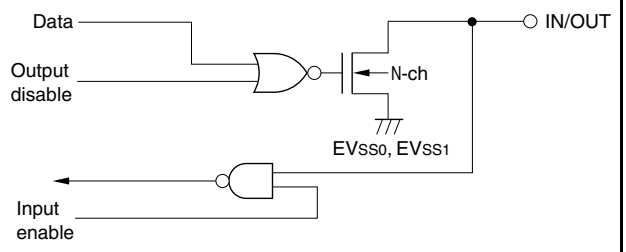
Type 11-G



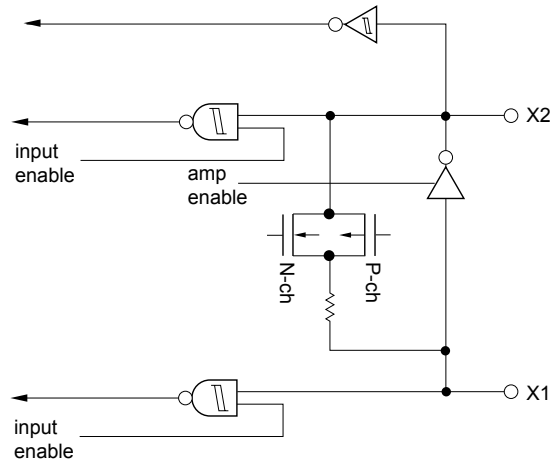
Type 37-B



Type 13-P



Type 37-C



Type 13-R

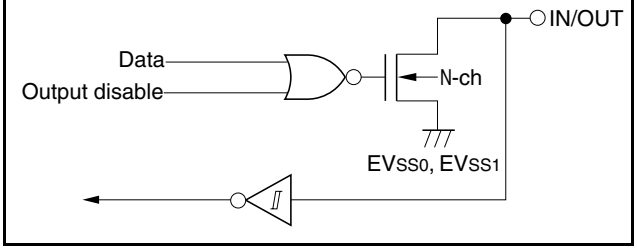


Table 4-3. Vector Table (2/2)

Vector Table Address	Interrupt Source	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
00034H	INTAD	√	√	√	√	√	√	√
00036H	INTRTC	–	√	√	√	√	√	√
00038H	INTRTCI	–	√	√	√	√	√	√
0003AH	INTKR	√	√	√	√	√	√	√
0003CH	INTST2/INTCSI20/INTIIC20	–	–	–	–	–	√	√
0003EH	INTP6	–	–	–	–	–	√	√
00040H	INTTM13	–	–	–	–	–	√	√
	INTMD	√	√	√	√	√	–	–
00042H	INTTM04	√	√	√	√	√	√	√
00044H	INTTM05	√	√	√	√	√	√	√
00046H	INTTM06	√	√	√	√	√	√	√
00048H	INTTM07	√	√	√	√	√	√	√
0004AH	INTSR2	–	–	–	–	–	√	√
	INTP6	√	√	√	√	√	–	–
0004CH	INTP7	–	√	√	√	√	√	√
0004EH	INTP8	–	–	–	–	–	√	√
00050H	INTP9	–	–	–	–	–	√	√
00052H	INTP10	–	–	–	–	–	√	√
00054H	INTP11	–	–	–	–	–	√	√
	INTSRE4	–	–	–	–	–	Note	Note
00056H	INTTM10	–	–	–	–	–	√	√
00058H	INTTM11	–	–	–	–	–	√	√
0005AH	INTTM12	–	–	–	–	–	√	√
0005CH	INTSRE2	–	–	–	–	–	√	√
0005EH	INTMD	–	–	–	–	–	√	√
00060H	INTST4	–	–	–	–	–	Note	Note
	INTCSI40	–	–	–	–	–	Note	Note
00062H	INTSR4	–	–	–	–	–	Note	Note
	INTCSI41	–	–	–	–	–	Note	Note
0007EH	BRK	√	√	√	√	√	√	√

Note Those are only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

Table 4-5. SFR List (1/6)

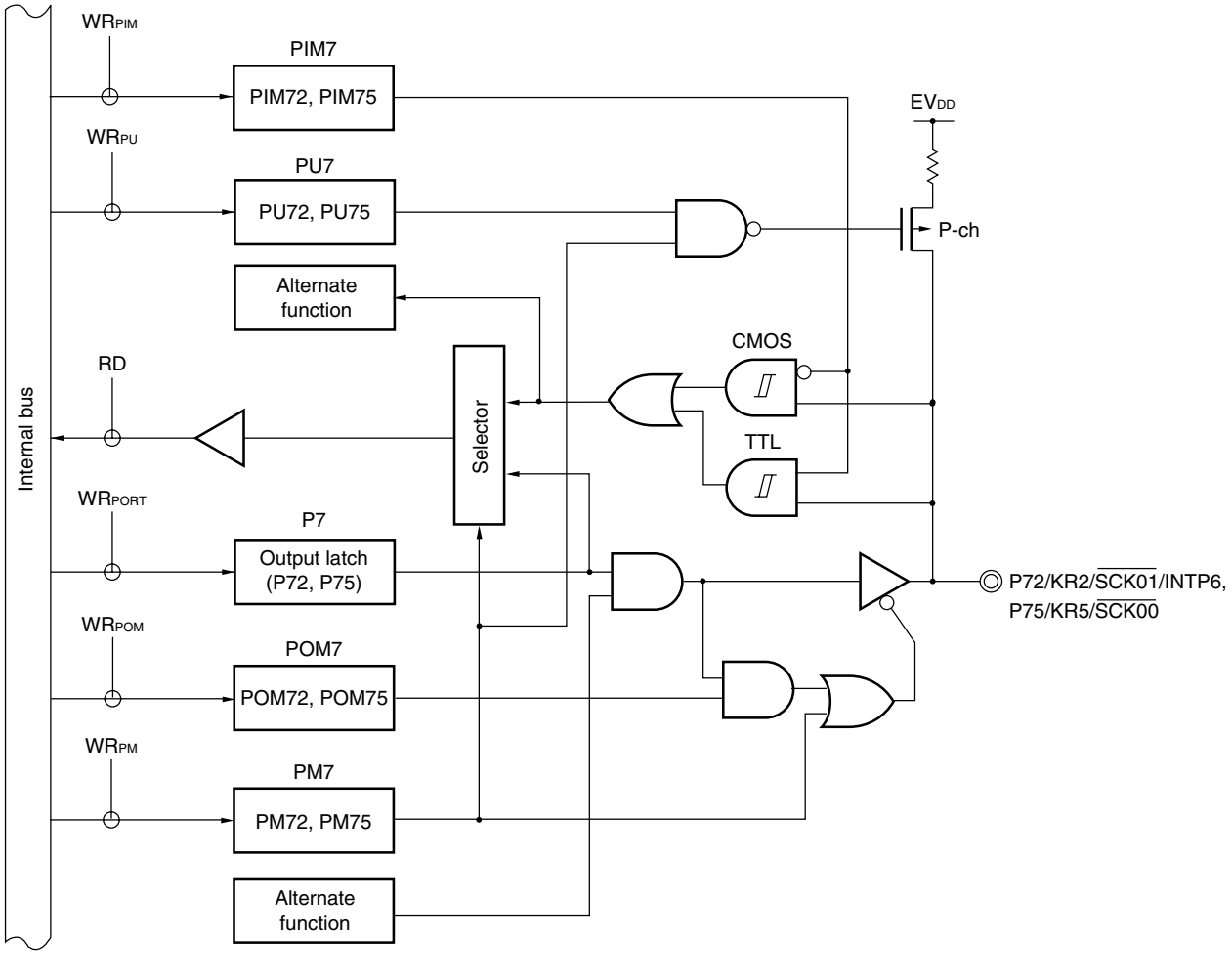
Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
FFF00H	Port register 0	P0	R/W	√	√	–	00H	–	–	–	√	√	√	√
FFF01H	Port register 1	P1	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF02H	Port register 2	P2	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF03H	Port register 3	P3	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF04H	Port register 4	P4	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF05H	Port register 5	P5	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF06H	Port register 6	P6	R/W	√	√	–	00H	–	–	√	√	√	√	√
FFF07H	Port register 7	P7	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF08H	Port register 8	P8	R/W	√	√	–	00H	√	√	√	√	√	–	√
FFF09H	Port register 9	P9	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF0BH	Port register 11	P11	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF0CH	Port register 12	P12	R/W	√	√	–	Undefined	√	√	√	√	√	√	√
FFF0DH	Port register 13	P13	R/W	√	√	–	00H	–	–	–	–	–	√	√
FFF0EH	Port register 14	P14	R/W	√	√	–	00H	–	–	√	√	√	√	√
FFF0FH	Port register 15	P15	R/W	√	√	–	00H	√	√	√	√	√	√	√
FFF10H	Serial data register 00	TXD0/SIO00 SDR00	R/W	–	√	√	0000H	√	√	√	√	√	√	√
FFF11H		–		–	–			√	√	√	√	√	√	√
FFF12H	Serial data register 01	RXD0/SIO01 SDR01	R/W	–	√	√	0000H	√	√	√	√	√	√	√
FFF13H		–		–	–			√	√	√	√	√	√	√
FFF14H	Serial data register 12	TXD3 SDR12	R/W	–	√	√	0000H	–	–	–	–	–	√	√
FFF15H		–		–	–			–	–	–	–	–	√	√
FFF16H	Serial data register 13	RXD3 SDR13	R/W	–	√	√	0000H	–	–	–	–	–	√	√
FFF17H		–		–	–			–	–	–	–	–	√	√
FFF18H	Timer data register 00	TDR00	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF19H														
FFF1AH	Timer data register 01	TDR01	R/W	–	–	√	0000H	√	√	√	√	√	√	√
FFF1BH														
FFF1EH	10-bit A/D conversion result register	ADCR	R	–	–	√	0000H	√	√	√	√	√	√	√
FFF1FH	8-bit A/D conversion result register	ADCRH	R	–	√	–	00H	√	√	√	√	√	√	√
FFF20H	Port mode register 0	PM0	R/W	√	√	–	FFH	–	–	–	√	√	√	√
FFF21H	Port mode register 1	PM1	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF22H	Port mode register 2	PM2	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF23H	Port mode register 3	PM3	R/W	√	√	–	FFH	√	√	√	√	√	√	√
FFF24H	Port mode register 4	PM4	R/W	√	√	–	FFH	√	√	√	√	√	√	√

Table 4-6. Extended SFR (2nd SFR) List (1/8)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
				1-bit	8-bit	16-bit								
F0017H	A/D port configuration register	ADPC	R/W	–	√	–	10H	√	√	√	√	√	√	√
F0030H	Pull-up resistor option register 0	PU0	R/W	√	√	–	00H	–	–	–	√	√	√	√
F0031H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0033H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0034H	Pull-up resistor option register 4	PU4	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0035H	Pull-up resistor option register 5	PU5	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0036H	Pull-up resistor option register 6	PU6	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0037H	Pull-up resistor option register 7	PU7	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0038H	Pull-up resistor option register 8	PU8	R/W	√	√	–	00H	–	–	–	–	–	–	√
F0039H	Pull-up resistor option register 9	PU9	R/W	√	√	–	00H	–	–	–	–	–	√	√
F003BH	Pull-up resistor option register 11	PU11	R/W	√	√	–	00H	–	–	–	–	–	√	√
F003CH	Pull-up resistor option register 12	PU12	R/W	√	√	–	00H	√	√	√	√	√	√	√
F003DH	Pull-up resistor option register 13	PU13	R/W	√	√	–	00H	–	–	–	–	–	–	√
F003EH	Pull-up resistor option register 14	PU14	R/W	√	√	–	00H	–	–	–	–	√	√	√
F0040H	Port input mode register 0	PIM0	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0041H	Port input mode register 1	PIM1	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0043H	Port input mode register 3	PIM3	R/W	√	√	–	00H	√	√	√	√	√	–	–
F0047H	Port input mode register 7	PIM7	R/W	√	√	–	00H	√	√	√	√	√	–	–
F0048H	Port input mode register 8	PIM8	R/W	√	√	–	00H	√	√	√	√	√	–	–
F004EH	Port input mode register 14	PIM14	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0050H	Port output mode register 0	POM0	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0051H	Port output mode register 1	POM1	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0053H	Port output mode register 0	POM3	R/W	√	√	–	00H	√	√	√	√	√	–	–
F0057H	Port output mode register 1	POM7	R/W	√	√	–	00H	√	√	√	√	√	–	–
F005EH	Port output mode register 14	POM14	R/W	√	√	–	00H	–	–	–	–	–	√	√
F0060H	Noise filter enable register 0	NFEN0	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0061H	Noise filter enable register 1	NFEN1	R/W	√	√	–	00H	√	√	√	√	√	√	√
F0062H	Noise filter enable register 2	NFEN2	R/W	√	√	–	00H	√	√	√	√	√	√	√
F00E0H	Multiplication/division data register C (L)	MDCL	R	–	–	√	0000H	√	√	√	√	√	√	√
F00E2H	Multiplication/division data register C (H)	MDCH	R	–	–	√	0000H	√	√	√	√	√	√	√
F00E8H	Multiplication/division control register	MDUC	R/W	√	√	–	00H	√	√	√	√	√	√	√
F00F0H	Peripheral enable register 0	PER0	R/W	√	√	–	00H	√	√	√	√	√	√	√
F00F1H	Peripheral enable register 1	PER1	R/W	√	√	–	00H	√	√	√	√	√	Note	Note
F00F2H	Peripheral enable register 2	PER2	R/W	√	√	–	00H	√	√	√	√	√	–	–

Note Those are only mounted in the 78K0R/KF3-L (μPD78F1027 and 78F1028) and the 78K0R/KG3-L (μPD78F1029 and 78F1030).

Figure 5-17. Block Diagram of P72 and P75



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
PIM7: Port input mode register 7
POM7: Port output mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Notes 1. The internal reset processing time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC).

3. The microcontroller operates on the 8 MHz internal high-speed oscillation clock if 8 MHz or 20 MHz is selected for the internal high-speed oscillator by using the option byte or on the 1 MHz internal high-speed oscillation clock if 1 MHz is selected.

4. The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

5. If the internal high-speed oscillator is set to 1 MHz by using the option byte, the 20 MHz internal high-speed oscillation clock cannot be used.

Cautions 1. A voltage stabilization time (about 2.12 to 5.84 ms) is required after the supply voltage reaches 1.61 V (TYP.). If the time for the supply voltage to rise from 1.61 V (TYP.) to 2.07 V (TYP.) is shorter than the voltage stabilization time, reset processing is entered after the voltage stabilization time elapses.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

Figure 8-11. Format of Timer Mode Register mn (TMRmn) (3/3)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKS mn	0	0	CCS mn	MAST ERmn	STS mn2	STS mn1	STS mn0	CIS mn1	CIS mn0	0	0	MD mn3	MD mn2	MD mn1	MD mn0

MD mn3	MD mn2	MD mn1	MD mn0	Operation mode of channel n	Count operation of TCR	Independent operation
0	0	0	1/0	Interval timer mode	Counting down	Possible
0	1	0	1/0	Capture mode	Counting up	Possible
0	1	1	0	Event counter mode	Counting down	Possible
1	0	0	1/0	One-count mode	Counting down	Impossible
1	1	0	0	Capture & one-count mode	Counting up	Possible
Other than above				Setting prohibited		
The operation of the MDmn0 bit varies depending on each operation mode (see table below).						

Operation mode (Value set by the MDmn3 to MDmn1 bits (see table above))	MD mn0	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode Note 1 (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation Note 2. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated, either.
Other than above		Setting prohibited

Notes 1. In one-count mode, interrupt output (INTTMmn) when starting a count operation and TOmn output are not controlled.

2. If the start trigger (TSmn = 1) is issued during operation, the counter is cleared, an interrupt is generated, and recounting is started.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-28. Format of Noise Filter Enable Registers 1, 2 (NFEN1, NFEN2) (78K0R/KF3-L, 78K0R/KG3-L) (1/2)

Address: F0061H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	TNFEN01	TNFEN00

Address: F0062H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN2	0	0	0	0	TNFEN13	TNFEN12	TNFEN11	TNFEN10

TNFEN07	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: SI41[Note 1]/TI07/TO07/P54 pin or RxD3/P14 pin[Note 2] 78K0R/KG3-L: TI07/TO07/P145 pin or RxD3/P14 pin[Note 2]
0	Noise filter OFF
1	Noise filter ON

TNFEN06	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: TI06/TO06/P06 pin 78K0R/KG3-L: TI06/TO06/P131 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN05	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: TI05/TO05/P05 pin 78K0R/KG3-L: TI05/TO05/P146 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/P42 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN03	Enable/disable using noise filter of TI03/TO03/INTP4/P31 pin input signal
0	Noise filter OFF
1	Noise filter ON

Notes 1. SI41 pin is only mounted in the μPD78F1027 and 78F1028.

2. The applicable pin can be switched by setting the ISC1 bit of the ISC register.

ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.

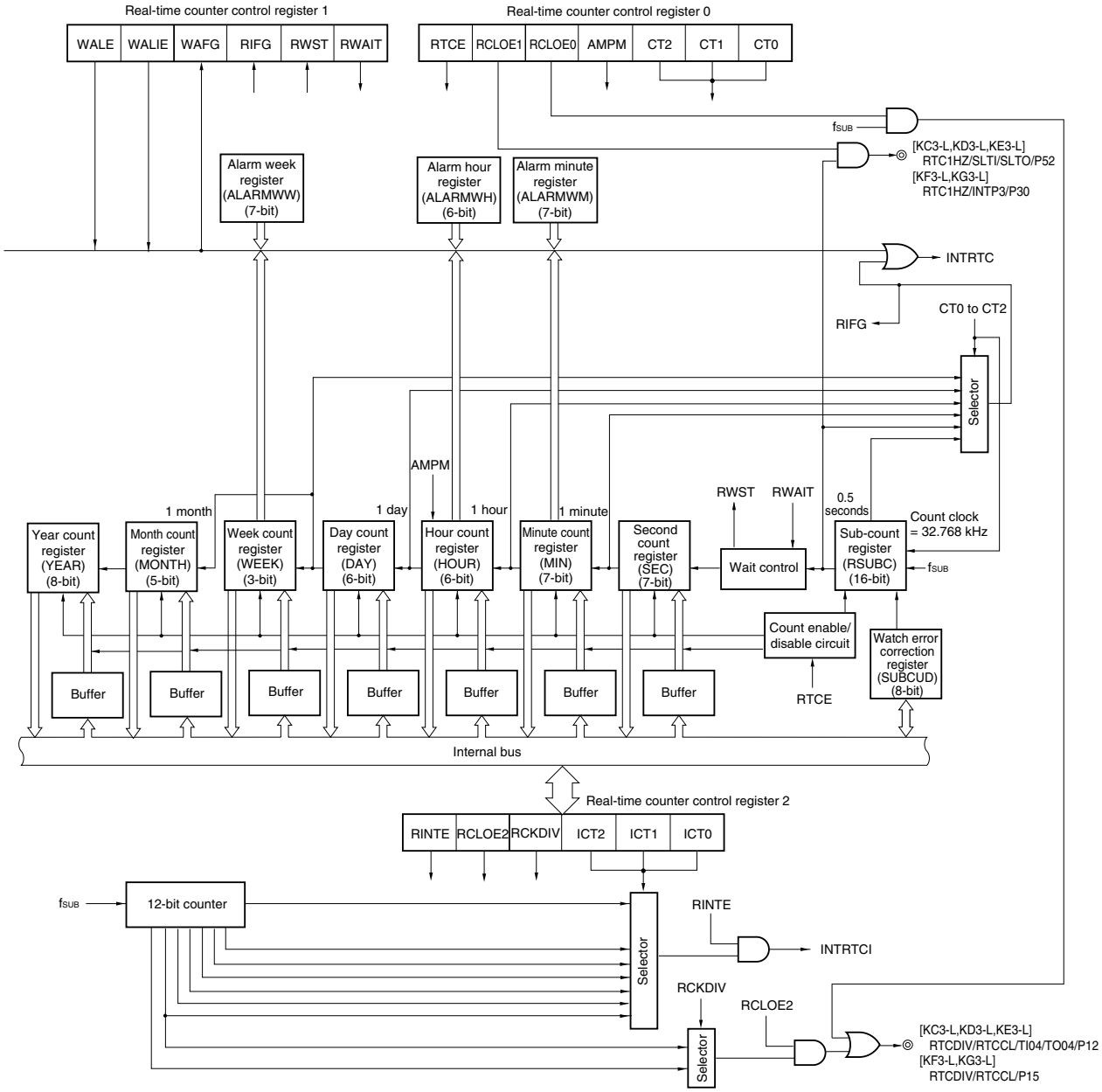
ISC1 = 1: Whether or not to use the noise filter of the RxD3 pin can be selected.

Figure 8-70. Operation Procedure When PWM Function Is Used (1/2)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp (TMRmn, TMRmp) of two channels to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp register of the slave channel.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channel. The TOMmp bit of timer output mode register m (TOMm) is set to 1 (slave channel output mode). Sets the TOLmp bit. Sets the TOmp bit and determines default level of the TOmp output. →	The TOmp pin goes into Hi-Z output state. The TOmp default setting level is output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp bit to 1 and enables operation of TOmp. →	TOmp does not change because channel stops operating.
	Clears the port register and port mode register to 0. →	The TOmp pin outputs the TOmp set level.

(**Note** and **Remark** are listed on the next page.)

Figure 9-1. Block Diagram of Real-Time Counter



(4) Real-time counter control register 2 (RTCC2)

The RTCC2 register is an 8-bit register that is used to control the interval interrupt function and the RTCDIV pin.

The RTCC2 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-5. Format of Real-Time Counter Control Register 2 (RTCC2)

Address: FFF9FH After reset: 00H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
RTCC2	RINTE	RCLOE2	RCKDIV	0	0	ICT2	ICT1	ICT0

RINTE	ICT2	ICT1	ICT0	Interval interrupt (INTRTCI) selection
0	×	×	×	Interval interrupt is not generated.
1	0	0	0	$2^6/f_{XT}$ (1.953125 ms)
1	0	0	1	$2^7/f_{XT}$ (3.90625 ms)
1	0	1	0	$2^8/f_{XT}$ (7.8125 ms)
1	0	1	1	$2^9/f_{XT}$ (15.625 ms)
1	1	0	0	$2^{10}/f_{XT}$ (31.25 ms)
1	1	0	1	$2^{11}/f_{XT}$ (62.5 ms)
1	1	1	×	$2^{12}/f_{XT}$ (125 ms)

RCLOE2[Note]	RTCDIV pin output control
0	Output of the RTCDIV pin is disabled.
1	Output of the RTCDIV pin is enabled.

RCKDIV	Selection of RTCDIV pin output frequency
0	The RTCDIV pin outputs 512 Hz. (1.95 ms)
1	The RTCDIV pin outputs 16.384 kHz. (0.061 ms)

Notes The RCLOE0 and RCLOE2 bits must not be enabled at the same time.

Cautions 1. Change the ICT2, ICT1, and ICT0 bits when RINTE = 0.

2. When the output from the RTCDIV pin is stopped, the output continues after a maximum of two clocks of f_{XT} and enters the low level. While 512 Hz is output, and when the output is stopped immediately after entering the high level, a pulse of at least one clock width of f_{XT} may be generated.

3. After the real-time counter starts operating, the output width of the RTCDIV pin may be shorter than as set during the first interval period.

(9) Day count register (DAY)

The DAY register is an 8-bit register that takes a value of 1 to 31 (decimal) and indicates the count value of days.
It counts up when the hour counter overflows.
This counter counts as follows.

- 01 to 31 (January, March, May, July, August, October, December)
- 01 to 30 (April, June, September, November)
- 01 to 29 (February, leap year)
- 01 to 28 (February, normal year)

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later. Even if the hour count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 01 to 31 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.
The DAY register can be set by an 8-bit memory manipulation instruction.
Reset signal generation clears this register to 01H.

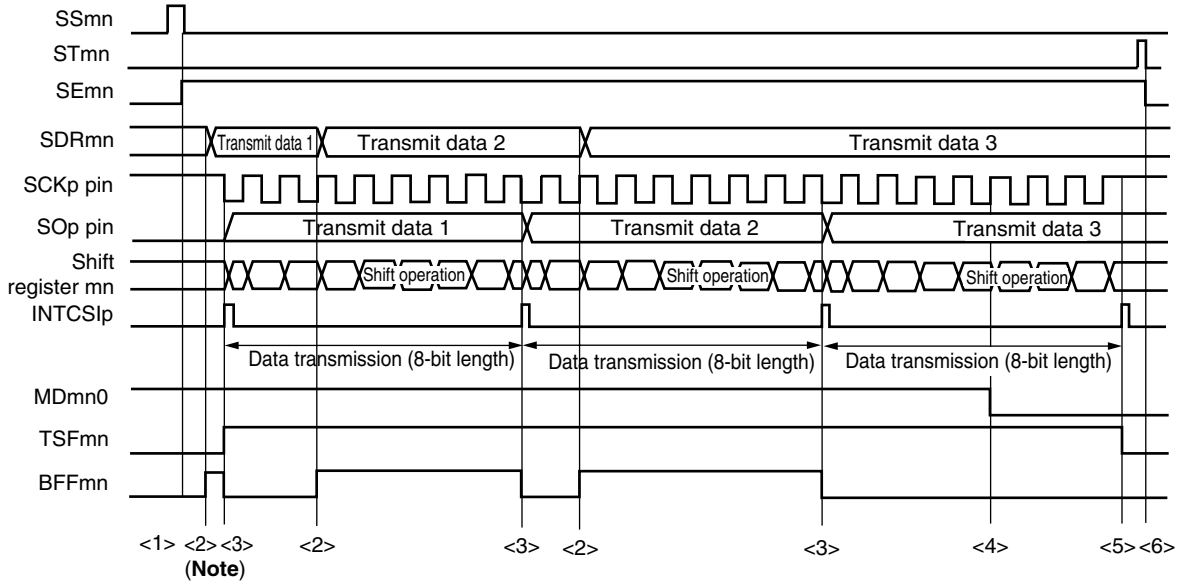
Figure 9-10. Format of Day Count Register (DAY)

Address: FFF96H After reset: 01H R/W

Symbol	7	6	5	4	3	2	1	0
DAY	0	0	DAY20	DAY10	DAY8	DAY4	DAY2	DAY1

(4) Processing flow (in continuous transmission mode)

Figure 14-34. Timing Chart of Master Transmission (in Continuous Transmission Mode)
(Type 1: DAPmn = 0, CKPmn = 0)



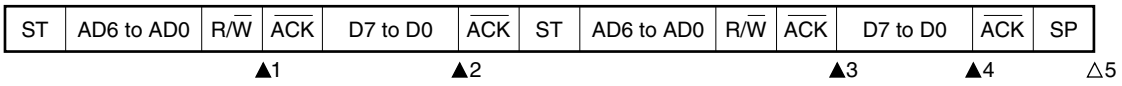
Note If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

(b) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

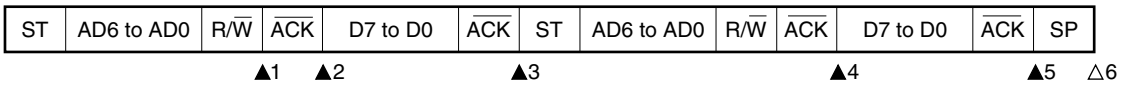
(i) When WTIM = 0 (after restart, matches SVA)



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0001×110B
▲4: IICS = 0001×000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, matches SVA)



▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010××00B
▲4: IICS = 0001×110B
▲5: IICS = 0001××00B
△6: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

18.4 Registers Controlling Interrupt Functions (78K0R/KF3-L, 78K0R/KG3-L)

The following 6 types of registers are used to control the interrupt functions.

- Interrupt request flag registers (IF0L, IF0H, IF1L, IF1H, IF2L, IF2H)
- Interrupt mask flag registers (MK0L, MK0H, MK1L, MK1H, MK2L, MK2H)
- Priority specification flag registers (PR00L, PR00H, PR01L, PR01H, PR02L, PR02H, PR10L, PR10H, PR11L, PR11H, PR12L, PR12H)
- External interrupt rising edge enable registers (EGP0, EGP1)
- External interrupt falling edge enable registers (EGN0, EGN1)
- Program status word (PSW)

Table 18-4 shows a list of interrupt request flags, interrupt mask flags, and priority specification flags corresponding to interrupt request sources.

Table 18-4. Flags Corresponding to Interrupt Request Sources (1/3)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTWDTI	WDTIIF	IF0L	WDTIMK	MK0L	WDTIPR0, WDTIPR1	PR00L, PR10L
INTLVI	LVIIF		LVIMK		LVIPR0, LVIPR1	
INTP0	PIF0		PMK0		PPR00, PPR10	
INTP1	PIF1		PMK1		PPR01, PPR11	
INTP2	PIF2		PMK2		PPR02, PPR12	
INTP3	PIF3		PMK3		PPR03, PPR13	
INTP4	PIF4		PMK4		PPR04, PPR14	
INTP5	PIF5		PMK5		PPR05, PPR15	
INTST3	STIF3	IF0H	STMK3	MK0H	STPR03, STPR13	PR00H, PR10H
INTSR3	SRIF3		SRMK3		SRPR03, SRPR13	
INTSRE3	SREIF3		SREMK3		SREPR03, SREPR13	
INTDMA0	DMAIF0		DMAMK0		DMAPR00, DMAPR10	
INTDMA1	DMAIF1		DMAMK1		DMAPR01, DMAPR11	
INTST0[Note 1]	STIF0[Note 1]		STMK0[Note 1]		STPR00, STPR10[Note 1]	
INTCSI00[Note 1]	CSIIF00[Note 1]		CSIMK00[Note 1]		CSIPR000, CSIPR100[Note 1]	
INTSR0[Note 2]	SRIF0[Note 2]		SRMK0[Note 2]		SRPR00, SRPR10[Note 2]	
INTCSI01[Note 2]	CSIIF01[Note 2]		CSIMK01[Note 2]		CSIPR001, CSIPR101[Note 2]	
INTSRE0	SREIF0		SREMK0		SREPR00, SREPR10	

Notes 1. Do not use UART0 and CSI00 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTST0 and INTCSI00 is generated, bit 5 of the IF0H register is set to 1. Bit 5 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

2. Do not use UART0 and CSI01 at the same time because they share flags for the interrupt request sources. If one of the interrupt sources INTSR0 and INTCSI01 is generated, bit 6 of the IF0H register is set to 1. Bit 6 of the MK0H, PR00H, and PR10H registers supports these three interrupt sources.

30.3.4 Recommended oscillator circuit constants

(1) X1 oscillation: Ceramic resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd..	CSTCC2M00G56-R0	SMD	2.0	Internal (47)	Internal (47)	0	1.8	5.5
	CSTCR4M00G55-R0	SMD	4.0	Internal (39)	Internal (39)	0		
	CSTLS4M00G56-B0	Lead		Internal (47)	Internal (47)	0		
	CSTLS4M19G56-B0	Lead	4.194	Internal (47)	Internal (47)	0		
	CSTCR4M19G55-R0	SMD		Internal (39)	Internal (39)	0		
	CSTCR4M91G55-R0	SMD	4.915	Internal (39)	Internal (39)	0		
	CSTLS4M91G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR5M00G55-R0	SMD	5.0	Internal (39)	Internal (39)	0		
	CSTLS5M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR6M00G53-R0	SMD	6.0	Internal (15)	Internal (15)	0		
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M00G52-R0	SMD	8.0	Internal (10)	Internal (10)	0		
	CSTLS8M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M38G52-R0	SMD	8.388	Internal (10)	Internal (10)	0		
	CSTLS8M38G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	0		
	CSTLS10M0G53-B0	Lead		Internal (15)	Internal (15)	0		
TDK Corporation	CCR4.0MUC8	SMD	4.0	Internal (27)	Internal (27)	0	1.8	5.5
	CCR4.19MUC8	SMD	4.19	Internal (27)	Internal (27)	0		
	CCR4.91MUC8	SMD	4.91	Internal (27)	Internal (27)	0		
	CCR5.0MUC8	SMD	5.0	Internal (27)	Internal (27)	0		
	CCR6.0MUC8	SMD	6.0	Internal (27)	Internal (27)	0		
	CCR8.0MXC8	SMD	8.0	Internal (18)	Internal (18)	0		
	CCR8.38MXC8	SMD	8.38	Internal (18)	Internal (18)	0		
	CCR10.0MXC8	SMD	10.0	Internal (18)	Internal (18)	0		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

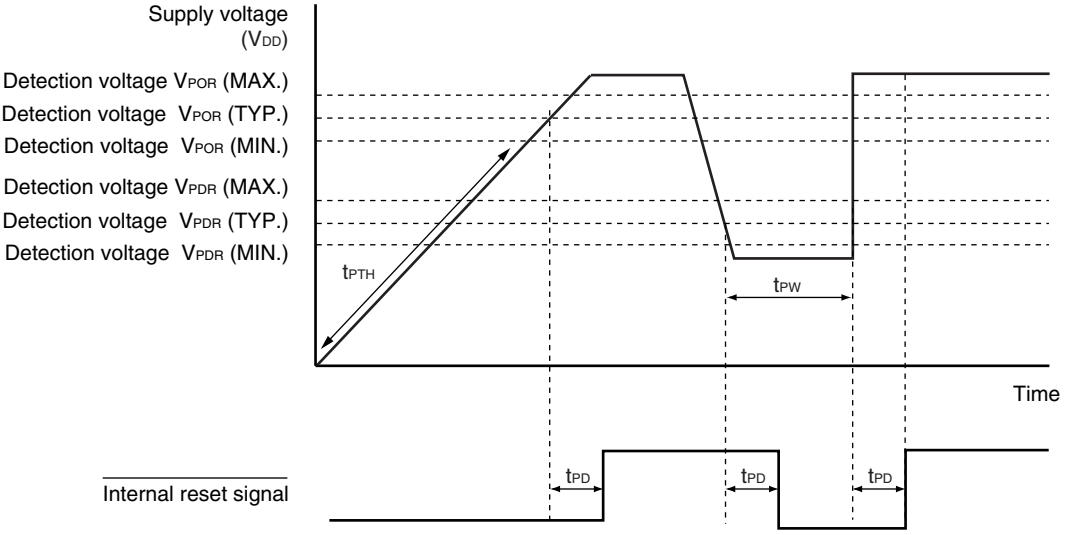
Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6.7 POC circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.52	1.61	1.70	V
	V_{PDR}	Power supply fall time	1.5	1.59	1.68	V
Power supply voltage rise inclination	t_{PTH}	Change inclination of V_{DD}: 0 V → V_{POR}	0.5			V/ms
Minimum pulse width	t_{PW}	When the voltage drops	200			μs
Detection delay time	t_{PD}				200	μs

POC Circuit Timing

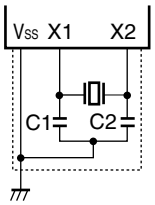
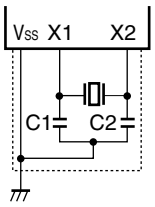


Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

31.3 Oscillator Characteristics

31.3.1 Main system clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} ≤ 2.7 V	2.0		5.0	MHz
Crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} ≤ 2.7 V	2.0		5.0	MHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

(4/7)

Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Change of **Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1))**	CHAPTER 5 CLOCK GENERATOR
	Change of **Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVIOFF = 0))**	
	Change of **5.6 Controlling Clock**	
	Addition of **Notes 3** and **4** to **5.6.6 CPU clock status transition diagram**	
	Change of **6.1.1 Independent channel operation function**	CHAPTER 6 TIMER ARRAY UNIT
	Change of **6.1.2 Simultaneous channel operation function**	
	Change of **Figure 6-1. Entire Configuration of Timer Array Unit TAUS**	
	Addition of **Figure 6-2. Internal Block Diagram of Channel of Timer Array Unit TAUS**	
	Change of **Figure 6-21. Format of Timer Output Mode Register 0 (TOM0)**	
	Change of **Figure 6-22. Format of Input Switch Control Register (ISC)**	
	Change of description of operation start in **Figure 6-39. Operation Procedure of Interval Timer/Square Wave Output Function**	
	Change of description in **6.7.2 Operation as external event counter**	
	Addition of **Caution** to **6.7.5 Operation as input signal high-/low-level width measurement**	
	Change of description in **6.8.2 Operation as PWM function**	
	Change of **Note** in **Figure 7-2. Format of Peripheral Enable Register 0 (PER0)**	CHAPTER 7 REAL-TIME COUNTER
	Addition of **Note** to **Figure 7-18. Procedure for Starting Operation of Real-Time Counter**	
	Change of **10.4.3 Setting window open period of watchdog timer** (deletion of window open period 25% setting)	CHAPTER 10 WATCHDOG TIMER
	Change of **Figure 11-5. A/D Converter Sampling and A/D Conversion Timing**	CHAPTER 11 A/D CONVERTER
	Change of description in **11.6 (9) Conversion results just after A/D conversion start**	
	Change of **Table 11-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**	
	Change of **Note 2** in **Figure 12-4. Format of Serial Clock Select Register 0 (SPS0)**	CHAPTER 12 SERIAL ARRAY UNIT
	Change of description of the MD0n0 bit in **Figure 12-5. Format of Serial Mode Register 0n (SMR0n) (2/2)**	
	Addition of **Note** to **Figure 12-6. Format of Serial Communication Operation Setting Register 0n (SCR0n) (2/3)**	
	Change of description in **12.3 (5) Higher 7 bits of the serial data register 0n (SDR0n)**	
	Change of **Figure 12-8. Format of Serial Flag Clear Trigger Register 0n (SIR0n)**	
	Change of **Figure 12-9. Format of Serial Status Register 0n (SSR0n)**	
	Change of **Figure 12-25. Procedure for Stopping Master Transmission**	
	Change of **Figure 12-27. Timing Chart of Master Transmission (in Single-Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-29. Timing Chart of Master Transmission (in Continuous Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	