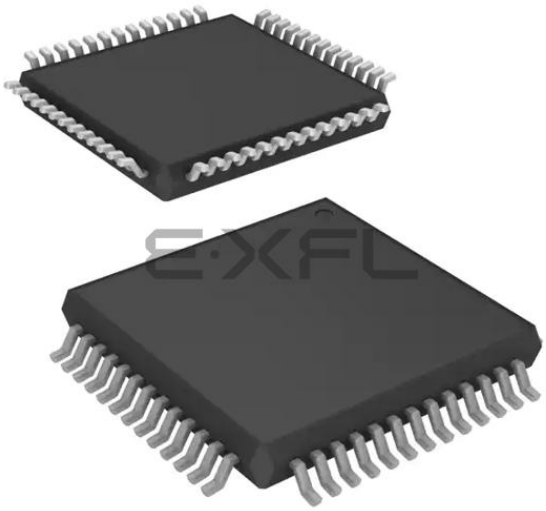
Renesas Electronics America Inc - UPD78F1005GB-GAG-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	40
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1005gb-gag-ax

(2) Non-port functions (1/3): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI10	Input			P150 to P152
CMP0M	Input	Input voltage on the (–) side of comparator 0	Analog input	P81
CMP0P	Input	Input voltage on the (+) side of comparator 0		P80/INTP3/PGAI
CMP1M	Input	Input voltage on the (–) side of comparator 1		P83
CMP1P	Input	Input voltage on the (+) side of comparator 1		P82/INTP7
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P31/SI10/RxD1/SDA10
INTP2				P32/$\overline{\text{SCK10}}$/SCL10
INTP3			Analog input	P80/CMP0P/PGAI
INTP4			Input port	P70/KR0/SO01
INTP5				P71/KR1/SI01
INTP6				P72/KR2/$\overline{\text{SCK01}}$
INTP7			Analog input	P82/CMP1P
KR0	Input	Key interrupt input	Input port	P70/SO01/INTP4
KR1				P71/SI01/INTP5
KR2				P72/$\overline{\text{SCK01}}$/INTP6
KR3				P73/SO00/TxD0
KR4				P74/SI00/RxD0
KR5				P75/$\overline{\text{SCK00}}$
KR6				P76
KR7				P77
PCLBUZ0	Output	Clock output/buzzer output	Output port	P140
PGAI	Input	Programmable gain amplifier input	Analog input	P80/CMP0P/INTP3
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz division) output	Input port	P12/TI04/TO04/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P12/TI04/TO04/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P52/SLTI/SLTO
$\overline{\text{RESET}}$	Input	System reset input	–	–

5.2.9 Port 8

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P80/CMP0P/ INTP3/PGAI	√		√	√	√
P81/CMP0M	√		√	√	√
P82/CMP1P/ INTP7	–	√	√	√	√
P83/CMP1M	√		√	√	√

Remark √: Mounted

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8).

Inputs to the P80 to P83 pins must be enabled or disabled in 1-bit units using port input mode register 8 (PIM8).

This port can also be used for an input voltage on the (+) sides of comparators 0 and 1, an input voltage on the (–) sides of comparators 0 and 1, an external interrupt request input, and a programmable gain amplifier input.

Reset signal generation sets port 8 to analog input mode.

Figures 5-19 to 5-21 show block diagrams of port 8.

Caution In the case of the 78K0R/KC3-L (40-pin), be sure to clear bit2 of the PM8 register to "0" after the reset release.

(5) Port output mode registers (POM3, POM7)

These registers set the output mode of P30 to P32, P70, P72, P73, or P75 in 1-bit units.

N-ch open drain output (V_{DD} tolerance) mode can be selected during serial communication with an external device of the different potential, and for the SDA10 pin during simplified I^2C communication with an external device of the same potential.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

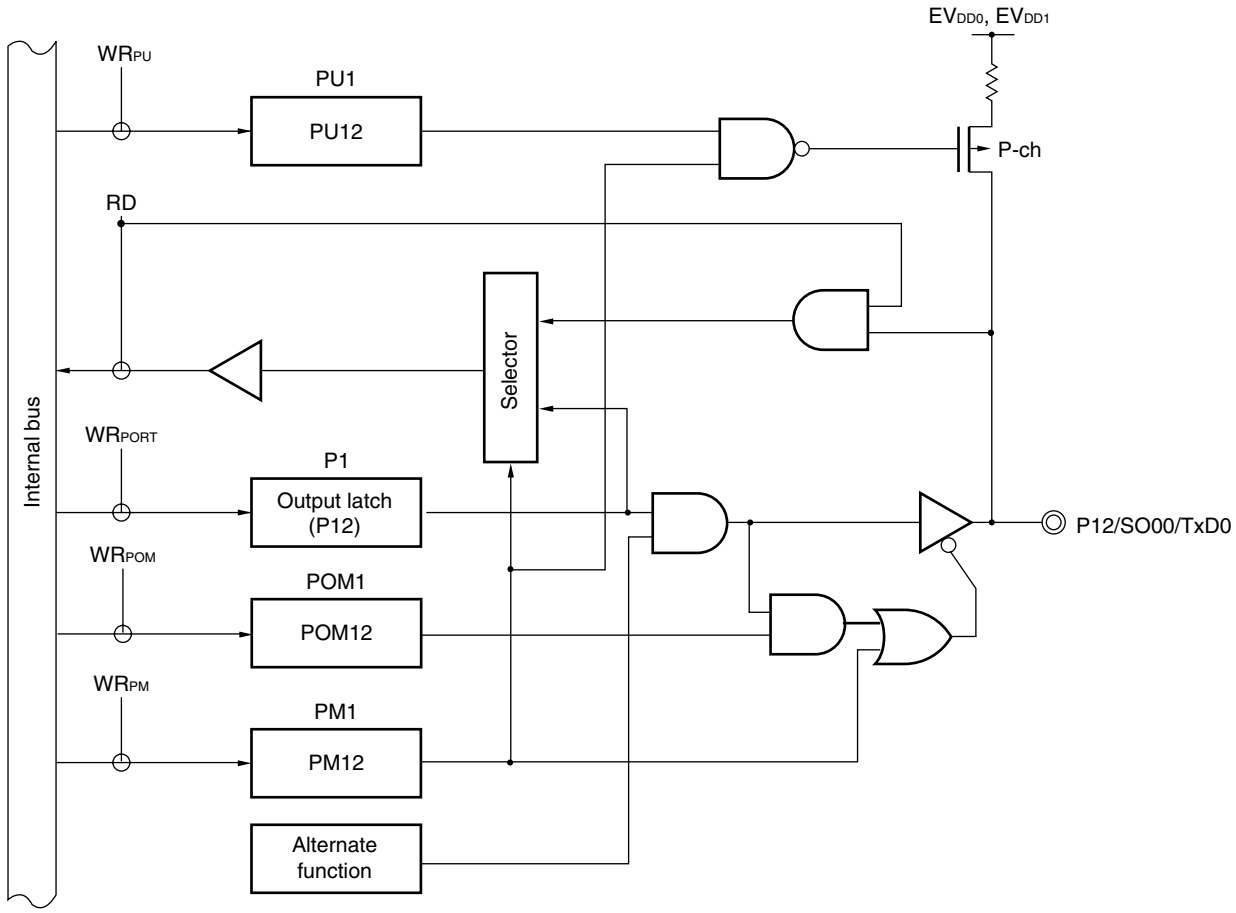
Reset signal generation clears these registers to 00H.

Figure 5-40. Format of Port Output Mode Register

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
POM3	0	0	0	0	0	POM32	POM31	POM30	F0053H	00H	R/W
POM7	0	0	POM75	0	POM73	POM72	0	POM70	F0057H	00H	R/W

POMmn	Pmn pin output mode selection (m = 3 and 7; n = 0 to 3 and 5)
0	Normal output mode
1	N-ch open-drain output (V_{DD} tolerance) mode

Figure 6-8. Block Diagram of P12



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
POM1: Port output mode register 1
RD: Read signal
WR××: Write signal

Caution While timer output is enabled (TOEmn = 1), even if the output by timer interrupt of each timer (INTTMmn) contends with writing to the TOmn bit, output is normally done to the TOmn pin.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.5.5 Timer Interrupt and TOmn Pin Output at Operation Start

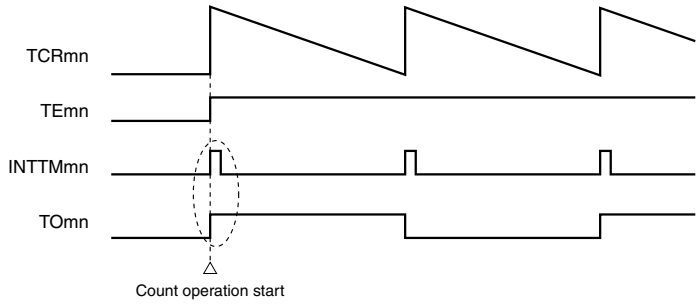
In the interval timer mode or capture mode, the MDmn0 bit in timer mode register mn (TMRmn) sets whether or not to generate a timer interrupt at count start.

When MDmn0 is set to 1, the count operation start timing can be known by the timer interrupt (INTTMmn) generation.

In the other modes, neither timer interrupt at count operation start nor TOmn output is controlled.

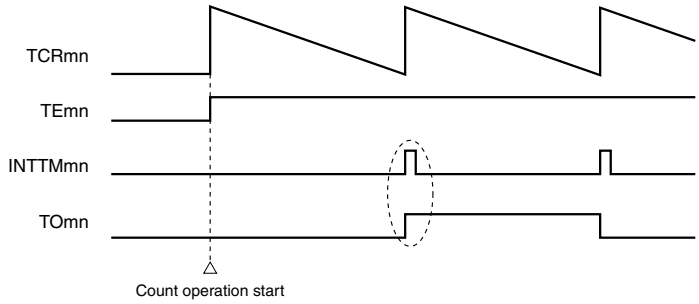
Figures 8-37 and 8-38 show operation examples when the interval timer mode (TOEmn = 1, TOMmn = 0) is set.

Figure 8-38. When MDmn0 is set to 1



When MDmn0 is set to 1, a timer interrupt (INTTMmn) is output at count operation start, and TOmn performs a toggle operation.

Figure 8-39. When MDmn0 is set to 0

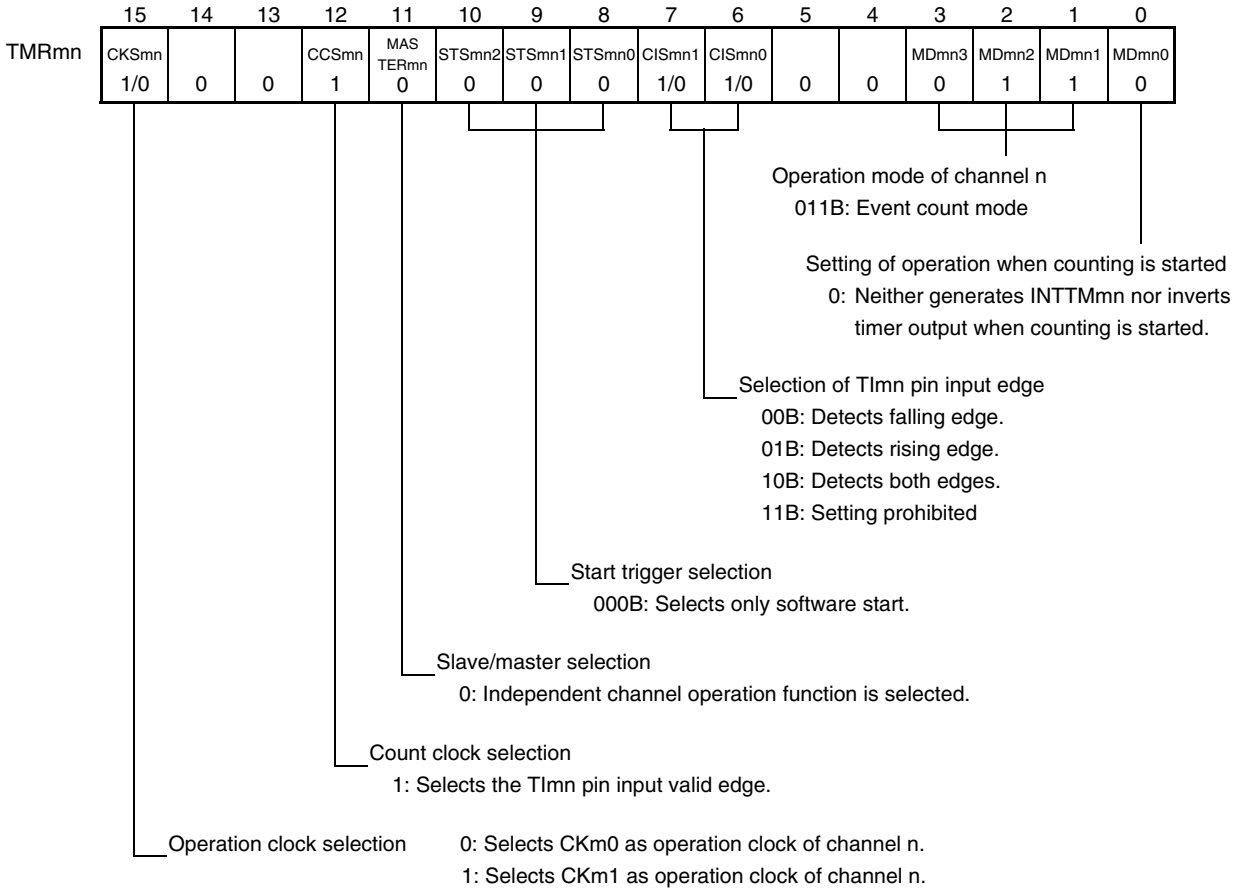


When MDmn0 is set to 0, a timer interrupt (INTTMmn) is not output at count operation start, and TOmn does not change either. After counting one cycle, INTTMmn is output and TOmn performs a toggle operation.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-47. Example of Set Contents of Registers in External Event Counter Mode

(a) Timer mode register mn (TMRmn)



(b) Timer output register m (TOm)

	Bit n	
TOm	TOmn	0: Outputs 0 from TOmn.
	0	

(c) Timer output enable register m (TOEm)

	Bit n	
TOEm	TOEmn	0: Stops the TOmn output operation by counting operation.
	0	

(d) Timer output level register m (TOLm)

	Bit n	
TOLm	TOLmn	0: Cleared to 0 when TOMmn = 0 (master channel output mode).
	0	

(e) Timer output mode register m (TOMm)

	Bit n	
TOMm	TOMmn	0: Sets master channel output mode.
	0	

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Remark If the overflow time is set to $2^{10}/f_{IL}$, the window close time and open time are as follows.

	Setting of Window Open Period		
	50%	75%	100%
Window close time	0 to 20.08 ms	0 to 10.04 ms	None
Window open time	20.08 to 29.68 ms	10.04 to 29.68 ms	0 to 29.68 ms

<When window open period is 50%>

- Overflow time:
  $2^{10}/f_{IL}$ (MAX.) = 2^{10}/34.5 kHz (MAX.) = 29.68 ms
- Window close time:
  0 to $2^{10}/f_{IL}$ (MIN.) × (1 − 0.5) = 0 to 2^{10}/25.5 kHz (MIN.) × 0.5 = 0 to 20.08 ms
- Window open time:
  $2^{10}/f_{IL}$ (MIN.) × (1 − 0.5) to $2^{10}/f_{IL}$ (MAX.) = 2^{10}/25.5 kHz (MIN.) × 0.5 to 2^{10}/34.5 kHz (MAX.) = 20.08 to 29.68 ms

12.4.4 Setting watchdog timer interval interrupt

Depending on the setting of bit 7 (WDTINT) of an option byte (000C0H), an interval interrupt (INTWDTI) can be generated when 75% of the overflow time is reached.

Table 12-5. Setting of Watchdog Timer Interval Interrupt

WDTINT	Use of Watchdog Timer Interval Interrupt
0	Interval interrupt is used.
1	Interval interrupt is generated when 75% of overflow time is reached.

Caution When operating with the X1 oscillation clock after releasing the STOP mode, the CPU starts operating after the oscillation stabilization time has elapsed.
Therefore, if the period between the STOP mode release and the watchdog timer overflow is short, an overflow occurs during the oscillation stabilization time, causing a reset.
Consequently, set the overflow time in consideration of the oscillation stabilization time when operating with the X1 oscillation clock and when the watchdog timer is to be cleared after the STOP mode release by an interval interrupt.

Remark The watchdog timer continues counting even after INTWDTI is generated (until ACH is written to the watchdog timer enable register (WDTE)). If ACH is not written to the WDTE register before the overflow time, an internal reset signal is generated.

13.3 Registers Used in A/D Converter

The A/D converter uses the following seven registers.

- Peripheral enable register 0 (PER0)
- A/D converter mode register (ADM)
- A/D port configuration register (ADPC)
- Analog input channel specification register (ADS)
- Port mode registers 2, 15, 8 Note (PM2, PM15, PM8 Note)
- 10-bit A/D conversion result register (ADCR)
- 8-bit A/D conversion result register (ADCRH)

Note Port mode register 8 is set only in the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L.

(1) Peripheral enable register 0 (PER0)

This register is used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

When the A/D converter is used, be sure to set bit 5 (ADCEN) of this register to 1.

The PER0 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-2. Format of Peripheral Enable Register 0 (PER0)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	SAU1EN Note 3	SAU0EN	TAU1EN Note 3	TAU0EN Note 3

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply. • SFR used by the A/D converter cannot be written. • The A/D converter is in the reset status.
1	Enables input clock supply. • SFR used by the A/D converter can be read/written.

Notes 1. That is not provided in 40-pin product of the 78K0R/KC3-L.

2. That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

3. 78K0R/KF3-L and 78K0R/KG3-L only.

Cautions 1. When setting the A/D converter, be sure to set the ADCEN bit to 1 first. If ADCEN = 0, writing to a control register of the A/D converter is ignored, and, even if the register is read, only the default value is read (except for port mode registers 2, 15, and 8 (PM2, PM15, and PM8)).

2. Be sure to clear the following bits to 0.

48-pin product of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: bits 0, 1, 3, 6

44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6

40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, 7

78K0R/KF3-L, 78K0R/KG3-L: bit 6

(5) Higher 7 bits of the serial data register mn (SDRmn)

The SDRmn register is the transmit/receive data register (16 bits) of channel n. Bits 7 to 0 function as a transmit/receive buffer register, and bits 15 to 9 are used as a register that sets the division ratio of the operation clock (f_{MCK}).

If the CCSmn bit of serial mode register mn (SMRmn) is cleared to 0, the clock set by dividing the operating clock by the higher 7 bits of the SDRmn register is used as the transfer clock.

The lower 8 bits of the SDRmn register function as a transmit/receive buffer register. During reception, the parallel data converted by the shift register is stored in the lower 8 bits, and during transmission, the data to be transmitted to the shift register is set to the lower 8 bits.

The SDRmn register can be read or written in 16-bit units.

However, the higher 7 bits can be written or read only when the operation is stopped (SEmn = 0). During operation (SEmn = 1), a value is written only to the lower 8 bits of the SDRmn register. When the SDRmn register is read during operation, 0 is always read.

Reset signal generation clears the SDRmn register to 0000H.

Figure 14-9. Format of Serial Data Register mn (SDRmn) (1/2)

Address: FFF10H, FFF11H (SDR00), FFF12H, FFF13H (SDR01), FFF44H, FFF45H (SDR02), FFF46H, FFF47H (SDR03), FFF48H, FFF49H (SDR10), FFF4AH, FFF4BH (SDR11), FFF14H, FFF15H (SDR12), FFF16H, FFF17H (SDR13), FFF4CH, FFF4DH (SDR20), FFF4EH, FFF4FH (SDR21) After reset: 0000H R/W

FFF11H (SDR00) FFF10H (SDR00)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDRmn								0								

SDRmn[15:9]							Transfer clock setting by dividing the operating clock (f_{MCK})
0	0	0	0	0	0	0	$f_{MCK}/2$
0	0	0	0	0	0	1	$f_{MCK}/4$
0	0	0	0	0	1	0	$f_{MCK}/6$
0	0	0	0	0	1	1	$f_{MCK}/8$
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	0	$f_{MCK}/254$
1	1	1	1	1	1	1	$f_{MCK}/256$

Cautions 1. Be sure to clear bit 8 to "0".

2. Setting SDRmn[15:9] = (0000000B, 0000001B) is prohibited when UART is used.

3. Setting SDRmn[15:9] = 0000000B is prohibited when simplified I^2C is used. Set SDRmn[15:9] to 0000001B or greater.

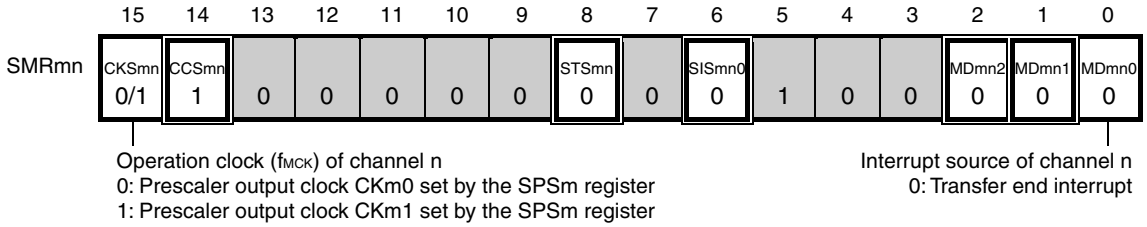
4. Do not write eight bits to the lower eight bits if operation is stopped (SEmn = 0). (If these bits are written to, the higher seven bits are cleared to 0.)

(**Remarks** are listed on the next page.)

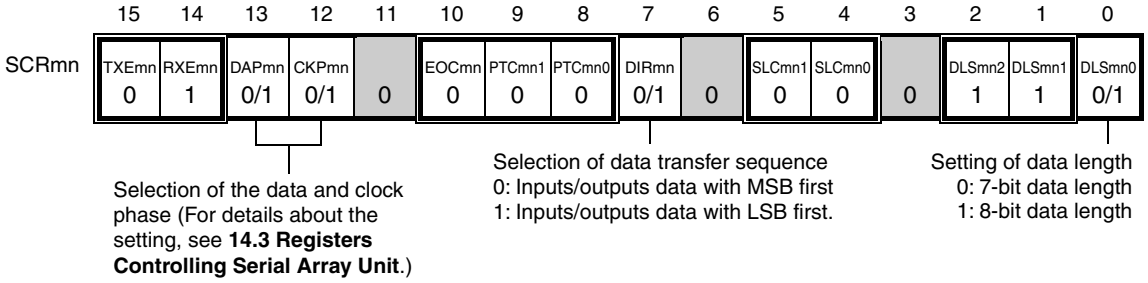
(1) Register setting

Figure 14-60. Example of Contents of Registers for Slave Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (1/2)

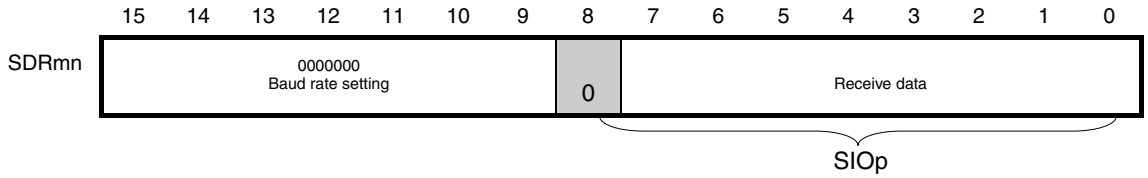
(a) Serial mode register mn (SMRmn)



(b) Serial communication operation setting register mn (SCRmn)

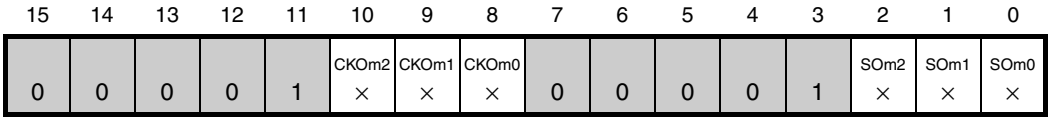


(c) Serial data register mn (SDRmn) (lower 8 bits: SIOp)



(d) Serial output register m (SOm) …The Register that not used in this mode.

<R>



Notes 1. Those bits are invalid while operating serial allay unit 1.

2. Those bits are invalid while operating serial allay unit 2.

(**Remark** is listed on the next page.)

Figure 15-6. Format of IICA Control Register 0 (IICCTL0) (1/4)

Address: F0230H After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
IICCTL0	IICE	LREL	WREL	SPIE	WTIM	ACKE	STT	SPT

IICE	I^2C operation enable
0	Stop operation. Reset the IICA status register (IICS)[Note 1]. Stop internal operation.
1	Enable operation.
Be sure to set this bit (1) while the SCL0 and SDA0 lines are at high level.	
Condition for clearing (IICE = 0)	Condition for setting (IICE = 1)
• Cleared by instruction • Reset	• Set by instruction

LREL[Notes 2, 3]	Exit from communications
0	Normal operation
1	This exits from the current communications and sets standby mode. This setting is automatically cleared to 0 after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCL0 and SDA0 lines are set to high impedance. The following flags of IICA control register 0 (IICCTL0) and the IICA status register (IICS) are cleared to 0. • STT • SPT • MSTS • EXC • COI • TRC • ACKD • STD
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LREL = 0)	Condition for setting (LREL = 1)
• Automatically cleared after execution • Reset	• Set by instruction

WREL[Notes 2, 3]	Wait cancellation
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.
When the WREL bit is set (wait canceled) during the wait period at the ninth clock pulse in the transmission status (TRC = 1), the SDA0 line goes into the high impedance state (TRC = 0).	
Condition for clearing (WREL = 0)	Condition for setting (WREL = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICA status register (IICS), the STCF and IICBSY bits of the IICA flag register (IICF), and the CLD and DAD bits of IICA control register 1 (IICCTL1) are reset.

2. The signal of this bit is invalid while IICE0 is 0.

3. When the LREL and WREL bits are read, 0 is always read.

Caution If the operation of I^2C is enabled (IICE = 1) when the SCL0 line is high level, the SDA0 line is low level, and the digital filter is turned on (DFC bit of IICCTL1 register = 1), a start condition will be inadvertently detected immediately. In this case, set (1) the LREL bit by using a 1-bit memory manipulation instruction immediately after enabling operation of I^2C (IICE = 1).

15.4 I^2C Bus Mode Functions

15.4.1 Pin configuration

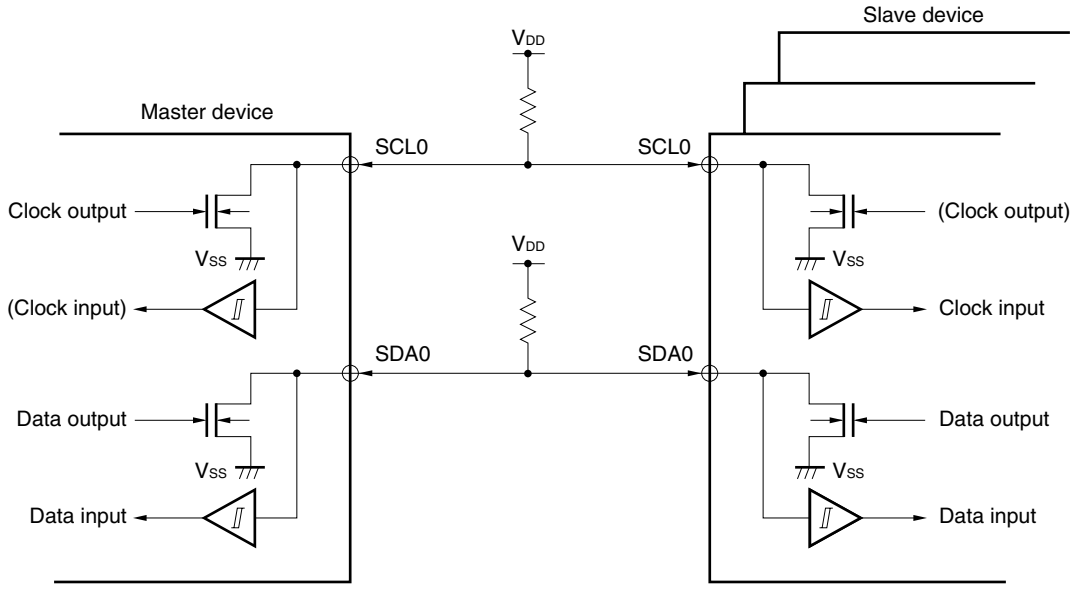
The serial clock pin (SCL0) and the serial data bus pin (SDA0) are configured as follows.

(1) SCL0..... This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

(2) SDA0 ..... This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

Figure 15-13. Pin Configuration Diagram

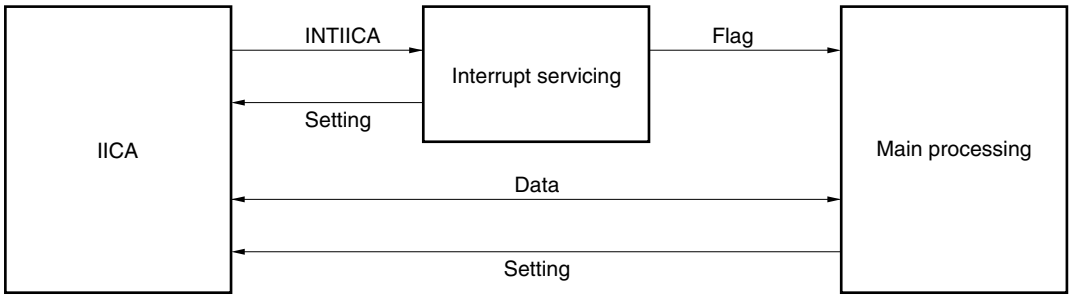


(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

This flag indicates that data communication is enabled. Its function is the same as the INTIICA interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC bit.

17.3 Registers Controlling DMA Controller

DMA controller is controlled by the following registers.

- DMA mode control register n (DMCn)
- DMA operation control register n (DRCn)

Remark n: DMA channel number (n = 0, 1)

Table 18-4. Flags Corresponding to Interrupt Request Sources (3/3)

Interrupt Source	Interrupt Request Flag		Interrupt Mask Flag		Priority Specification Flag	
		Register		Register		Register
INTP11	PIF11	IF2H	PMK11	MK2H	PPR011, PPR111	PR02H, PR12H
INTSRE4[Note]	SREIF4[Note]		SREMK4[Note]		SREPR04, SREPR14[Note]	
INTTM10	TMIF10		TMMK10		TMPR010, TMPR110	
INTTM11	TMIF11		TMMK11		TMPR011, TMPR111	
INTTM12	TMIF12		TMMK12		TMPR012, TMPR112	
INTSRE2	SREIF2		SREMK2		SREPR02, SREPR12	
INTMD	MDIF		MDMK		MDPR0, MDPR1	
INTST4[Note]	STIF4[Note]		STMK4[Note]		STPR04, STPR14[Note]	
INTCSI40[Note]	CSIIF40[Note]		CSIMK40[Note]		CSIPR040, CSIPR140[Note]	
INTSR4[Note]	SRIF4[Note]		SRMK4[Note]		SRPR04, SRPR14[Note]	
INTCSI41[Note]	CSIIF41[Note]		CSIMK41[Note]		CSIPR041, CSIPR141[Note]	

Note Those are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.2 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD}		−0.5 to +6.5	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS}		−0.5 to +0.3	V
	AV_{REF}		−0.5 to V_{DD} + 0.3 Note 1	V
	AV_{SS}		−0.5 to + 0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to + 3.6 and −0.3 to V_{DD} + 0.3 Note 2	V
Input voltage	V_{I1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P70 to P77, P120 to P124, P141, EXCLK, $\overline{\text{RESET}}$, FLMD0	−0.3 to EV_{DD} + 0.3 and −0.3 to V_{DD} + 0.3 Note 1	V
	V_{I2}	P60, P61 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P80 to P83, P150 to P153	−0.3 to AV_{REF} + 0.3 and −0.3 to V_{DD} + 0.3 Note 1	V
Output voltage	V_{O1}	P00, P01, P10 to P17, P30 to P33, P40 to P43, P50 to P53, P60, P61, P70 to P77, P120, P140, P141	−0.3 to EV_{DD} + 0.3 Note 1	V
	V_{O2}	P20 to P27, P80 to P83, P150 to P153	−0.3 to AV_{REF} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI11, PGAI, CMP0M, CMP0P, CMP1M, CMP1P	−0.3 to AV_{REF} + 0.3 Note 1 and −0.3 to V_{DD} + 0.3 Note 1	V

Notes 1. Must be 6.5 V or lower.

2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

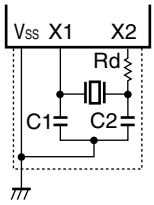
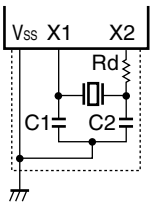
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.3 Oscillator Characteristics

30.3.1 Main system clock oscillator characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	
Crystal resonator		X1 clock oscillation frequency (f_X)Note	2.7 V ≤ V_{DD} ≤ 5.5 V	2.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	2.0		5.0	

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the internal high-speed oscillation clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

30.3.4 Recommended oscillator circuit constants

(1) X1 oscillation: Ceramic resonator (AMPH = 0, RMC = 00H, T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended Circuit Constants			Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Manufacturing Co., Ltd..	CSTCC2M00G56-R0	SMD	2.0	Internal (47)	Internal (47)	0	1.8	5.5
	CSTCR4M00G55-R0	SMD	4.0	Internal (39)	Internal (39)	0		
	CSTLS4M00G56-B0	Lead		Internal (47)	Internal (47)	0		
	CSTLS4M19G56-B0	Lead	4.194	Internal (47)	Internal (47)	0		
	CSTCR4M19G55-R0	SMD		Internal (39)	Internal (39)	0		
	CSTCR4M91G55-R0	SMD	4.915	Internal (39)	Internal (39)	0		
	CSTLS4M91G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR5M00G55-R0	SMD	5.0	Internal (39)	Internal (39)	0		
	CSTLS5M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCR6M00G53-R0	SMD	6.0	Internal (15)	Internal (15)	0		
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M00G52-R0	SMD	8.0	Internal (10)	Internal (10)	0		
	CSTLS8M00G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE8M38G52-R0	SMD	8.388	Internal (10)	Internal (10)	0		
	CSTLS8M38G53-B0	Lead		Internal (15)	Internal (15)	0		
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	0		
	CSTLS10M0G53-B0	Lead		Internal (15)	Internal (15)	0		
TDK Corporation	CCR4.0MUC8	SMD	4.0	Internal (27)	Internal (27)	0	1.8	5.5
	CCR4.19MUC8	SMD	4.19	Internal (27)	Internal (27)	0		
	CCR4.91MUC8	SMD	4.91	Internal (27)	Internal (27)	0		
	CCR5.0MUC8	SMD	5.0	Internal (27)	Internal (27)	0		
	CCR6.0MUC8	SMD	6.0	Internal (27)	Internal (27)	0		
	CCR8.0MXC8	SMD	8.0	Internal (18)	Internal (18)	0		
	CCR8.38MXC8	SMD	8.38	Internal (18)	Internal (18)	0		
	CCR10.0MXC8	SMD	10.0	Internal (18)	Internal (18)	0		

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L so that the internal operation conditions are within the specifications of the DC and AC characteristics.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

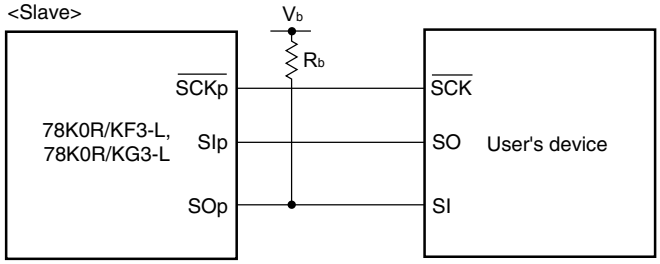
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	13.6 MHz < f_{MCK}	10/f_{MCK}			ns
			6.8 MHz < f_{MCK} ≤ 13.6 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 6.8 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	18.5 MHz < f_{MCK}	16/f_{MCK}			ns
			14.8 MHz < f_{MCK} ≤ 18.5 MHz	14/f_{MCK}			ns
			11.1 MHz < f_{MCK} ≤ 14.8 MHz	12/f_{MCK}			ns
			7.4 MHz < f_{MCK} ≤ 11.1 MHz	10/f_{MCK}			ns
			3.7 MHz < f_{MCK} ≤ 7.4 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 3.7 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		t_{KCY2}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK2}			90			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 3	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 230	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

CSI mode connection diagram (during communication at different potential)



(**Caution** and **Remark** are given on the next page.)

(6/7)

Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Change of **Figure 12-81. Flowchart of UART Reception**	CHAPTER 12 SERIAL ARRAY UNIT
	Change of **Note 2** in **Table 12-3. Selection of Operation Clock**	
	Addition of **Note** to **12.7.1 Address field transmission**	
	Change of **Figure 12-92. Timing Chart of Address Field Transmission**	
	Addition of **Note** to **12.7.2 Data transmission**	
	Change of **Figure 12-95. Timing Chart of Data Transmission**	
	Addition of **Note** to **12.7.3 Data reception**	
	Change of **Note 2** in **Table 12-4. Selection of Operation Clock**	
	Change of description of the STT bit in **Figure 13-6. Format of IICA Control Register 0 (IICCTL0) (3/4)**	CHAPTER 13 SERIAL INTERFACE IICA
	Change of **Caution** and description of the SPT bit in **Figure 13-6. Format of IICA Control Register 0 (IICCTL0) (4/4)**	
	Change of **Note** in **Figure 13-7. Format of IICA Status Register (IICS) (2/3)**	
	Change of **13.4.2 Setting transfer clock by using IICWL and IICWH registers**	
	Addition of **Caution** to **15.5.4 Holding DMA transfer pending by DWAITn bit**	CHAPTER 15 DMA CONTROLLER
	Addition of description to **15.5.5 Forced termination by software**	
	Addition of **Example 3** to **Figure 15-11. Forced Termination of DMA Transfer (2/2)**	
	Change of **15.6 (2) DMA response time**	
	Change of **16.2 Interrupt Sources and Configuration**	CHAPTER 16 INTERRUPT FUNCTIONS
	Change of **Figure 18-5. STOP Mode Release by Interrupt Request Generation (2/2)**	CHAPTER 18 STANDBY FUNCTION
	Addition of **(6) Internal reset by a reset processing check error**	CHAPTER 19 RESET FUNCTION
	Change of **Figure 19-1. Block Diagram of Reset Function**	
	Change of **Figure 19-3. Timing of Reset Due to Execution of Illegal Instruction or Watchdog Timer Overflow**	
	Change of **Note 2** in **Table 19-2. Hardware Statuses After Reset Acknowledgment (3/4)**	
	Change of **Figure 19-5. Format of Reset Control Flag Register (RESF)**	
	Change of **Table 19-3. RESF Register Status When Reset Request Is Generated**	
	Change of **Figure 20-2. Timing of Generation of Internal Reset Signal by Power-on-Clear Circuit and Low-Voltage Detector**	CHAPTER 20 POWER-ON-CLEAR CIRCUIT
	Change of **Figure 20-3. Example of Software Processing After Reset Release (2/2)**	
	Addition of **Caution 4** to **Figure 21-2. Format of Low-Voltage Detection Register (LVIM)**	CHAPTER 21 LOW-VOLTAGE DETECTOR
	Addition of **Caution 4** to **Figure 21-3. Format of Low-Voltage Detection Level Select Register (LVIS)**	
	Change of **Figure 21-11. Example of Software Processing After Reset Release (2/2)**	
	Change of **Caution 2** in **Figure 22-1. Format of Regulator Mode Control Register (RMC)**	CHAPTER 22 REGULATOR
	Change of **Figure 23-1. Format of User Option Byte (000C0H/010C0H) (1/2)**	CHAPTER 23 OPTION BYTE
	Change of **23.4 Setting of Option Byte**	