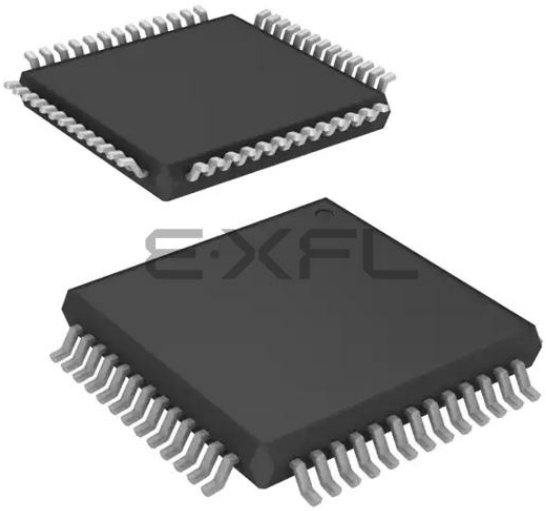
# Renesas Electronics America Inc - UPD78F1006GB-GAG-AX Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0R |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | 3-Wire SIO, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 40 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 3K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 52-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1006gb-gag-ax |

### 3.1.1 78K0R/KF3-L

#### (1) Port functions (1/2): 78K0R/KF3-L

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| P02 | I/O | Port 0.<br>5-bit I/O port.<br>Input of P03 and P04 can be set to TTL input buffer.<br>Output of P02 to P04 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | SO10/TxD1 |
| P03 | | | | SI10/RxD1/SDA10 |
| P04 | | | | $\overline{SCK10}$/SCL10 |
| P05 | | | | TI05/TO05 |
| P06 | | | | TI06/TO06 |
| P10 | I/O | Port 1.<br>8-bit I/O port.<br>Input of P10 and P11 can be set to TTL input buffer.<br>Output of P10 and P12 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | $\overline{SCK00}$ |
| P11 | | | | SI00/RxD0 |
| P12 | | | | SO00/TxD0 |
| P13 | | | | TxD3 |
| P14 | | | | RxD3 |
| P15 | | | | RTCDIV/RTCCL |
| P16 | | | | TI01/TO01/INTP5 |
| P17 | | | | TI02/TO02 |
| P20 to P27 | I/O | Port 2.<br>8-bit I/O port.<br>Input/output can be specified in 1-bit units. | Digital input port | ANI0 to ANI7 |
| P30 | I/O | Port 3.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | RTC1HZ/INTP3 |
| P31 | | | | TI03/TO03/INTP4 |
| P40[Note 1] | I/O | Port 4.<br>8-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | TOOL0 |
| P41 | | | | TOOL1 |
| P42 | | | | TI04/TO04 |
| P43 | | | | $\overline{SCK01}$ |
| P44 | | | | SI01 |
| P45 | | | | SO01 |
| P46, P47 | | | | – |
| P50 | I/O | Port 5.<br>6-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | INTP1/$\overline{SCK40}$[Note 2] |
| P51 | | | | INTP2/SI40/RxD4[Note 2] |
| P52 | | | | TO00/SO40/TxD4[Note 2] |
| P53 | | | | TI00/$\overline{SCK41}$[Note 2] |
| P54 | | | | TI07/TO07/SI41[Note 2] |
| P55 | | | | PCLBUZ1/INTP7/SO41[Note 2] |

**Notes 1.** If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally (see **Caution** in **3.2.5 P40 to P47 (port 4)**).

**2.** SCK40, SCK41, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

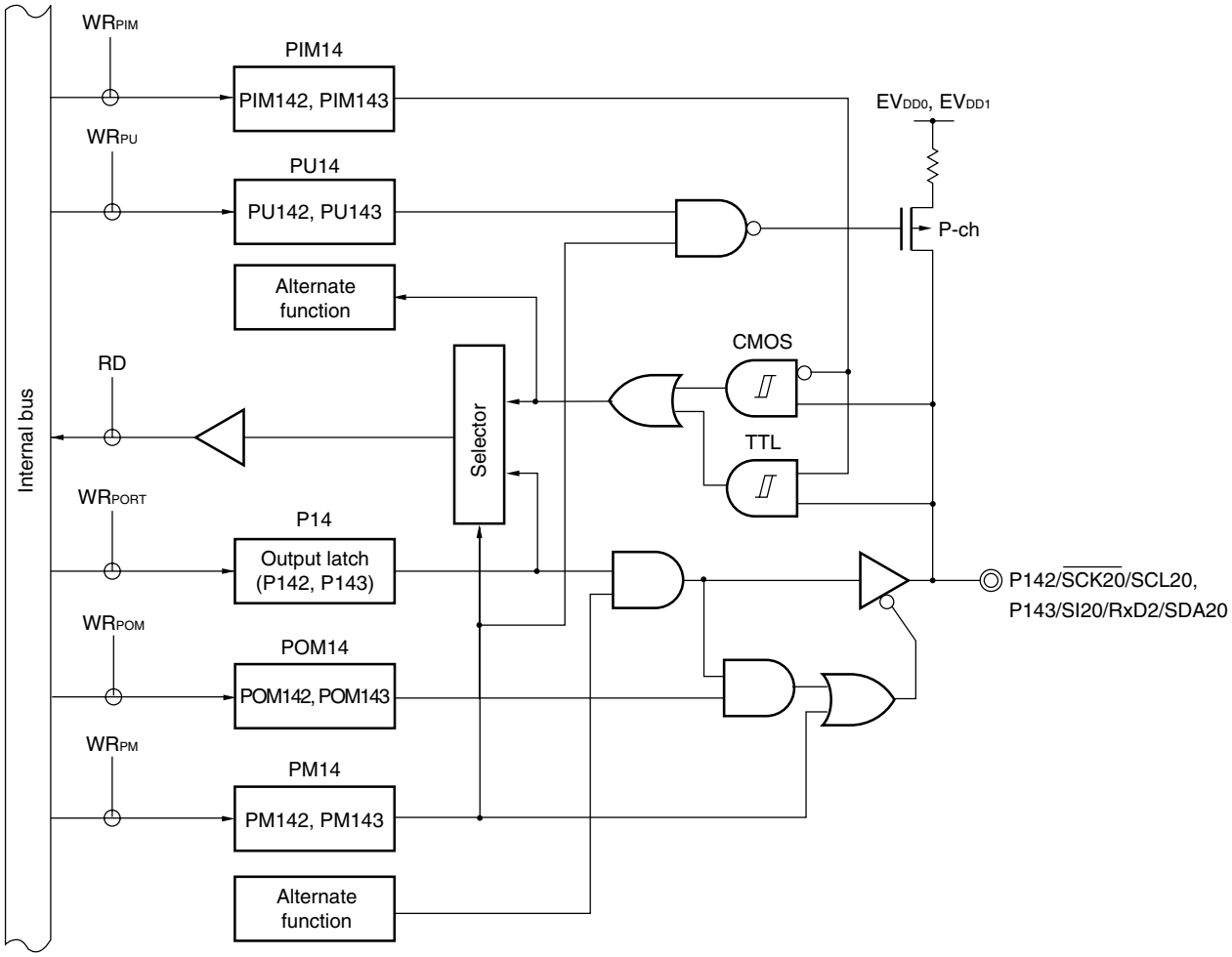
### 3.1.2 78K0R/KG3-L

**(1) Port functions (1/3): 78K0R/KG3-L**

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| P00 | I/O | Port 0.<br>7-bit I/O port.<br>Input of P03 and P04 can be set to TTL input buffer.<br>Output of P02 to P04 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | TI00 |
| P01 | | | | TO00 |
| P02 | | | | SO10/TxD1 |
| P03 | | | | SI10/RxD1/SDA10 |
| P04 | | | | $\overline{SCK10}$/SCL10 |
| P05, P06 | | | | – |
| P10 | I/O | Port 1.<br>8-bit I/O port.<br>Input of P10 and P11 can be set to TTL input buffer.<br>Output of P10 and P12 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | $\overline{SCK00}$ |
| P11 | | | | SI00/RxD0 |
| P12 | | | | SO00/TxD0 |
| P13 | | | | TxD3 |
| P14 | | | | RxD3 |
| P15 | | | | RTCDIV/RTCCL |
| P16 | | | | TI01/TO01/INTP5 |
| P17 | | | | TI02/TO02 |
| P20 to P27 | I/O | Port 2.<br>8-bit I/O port.<br>Input/output can be specified in 1-bit units. | Digital input port | ANI0 to ANI7 |
| P30 | I/O | Port 3.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | RTC1HZ/INTP3 |
| P31 | | | | TI03/TO03/INTP4 |
| P40[Note] | I/O | Port 4.<br>8-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | TOOL0 |
| P41 | | | | TOOL1 |
| P42 | | | | TI04/TO04 |
| P43 | | | | $\overline{SCK01}$ |
| P44 | | | | SI01 |
| P45 | | | | SO01 |
| P46 | | | | INTP1/TI05/TO05 |
| P47 | | | | INTP2 |

**Note** If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally (see **Caution** in **3.2.5 P40 to P47 (port 4)**).

**Figure 6-49. Block Diagram of P142 and P143**




P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
PIM14: Port input mode register 14
POM14: Port output mode register 14
RD: Read signal
WR××: Write signal

**Figure 8-4. Entire Configuration of Timer Array Unit 1 (78K0R/KF3-L, 78K0R/KG3-L only)**

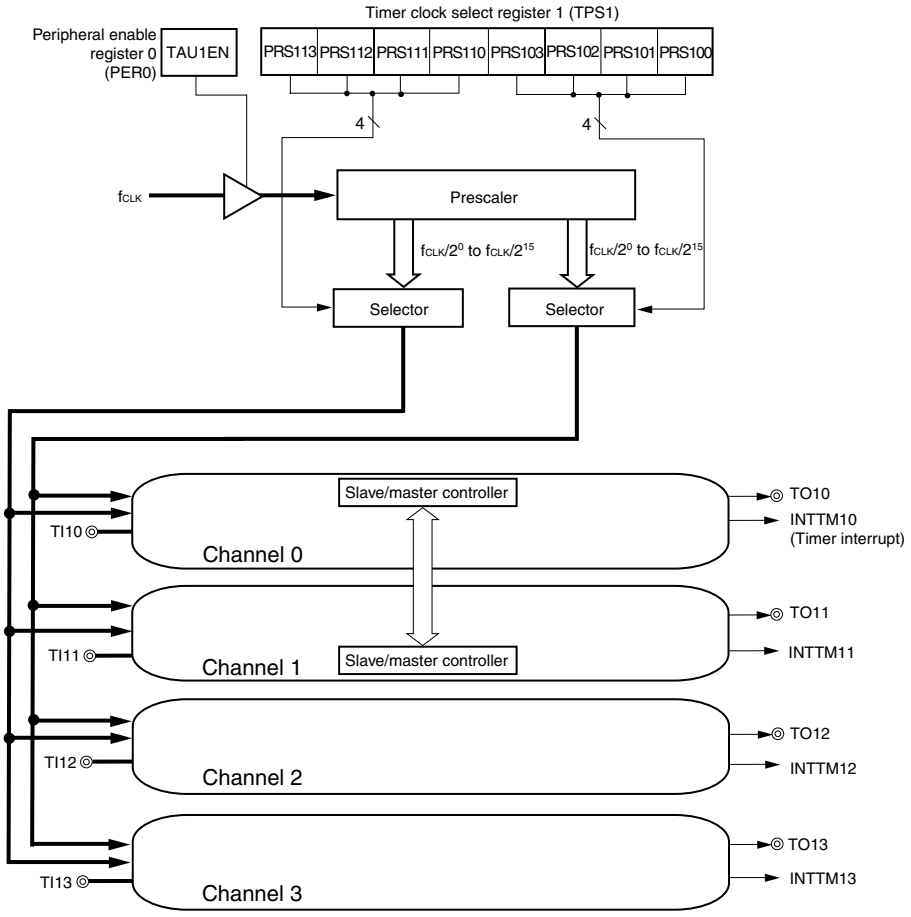
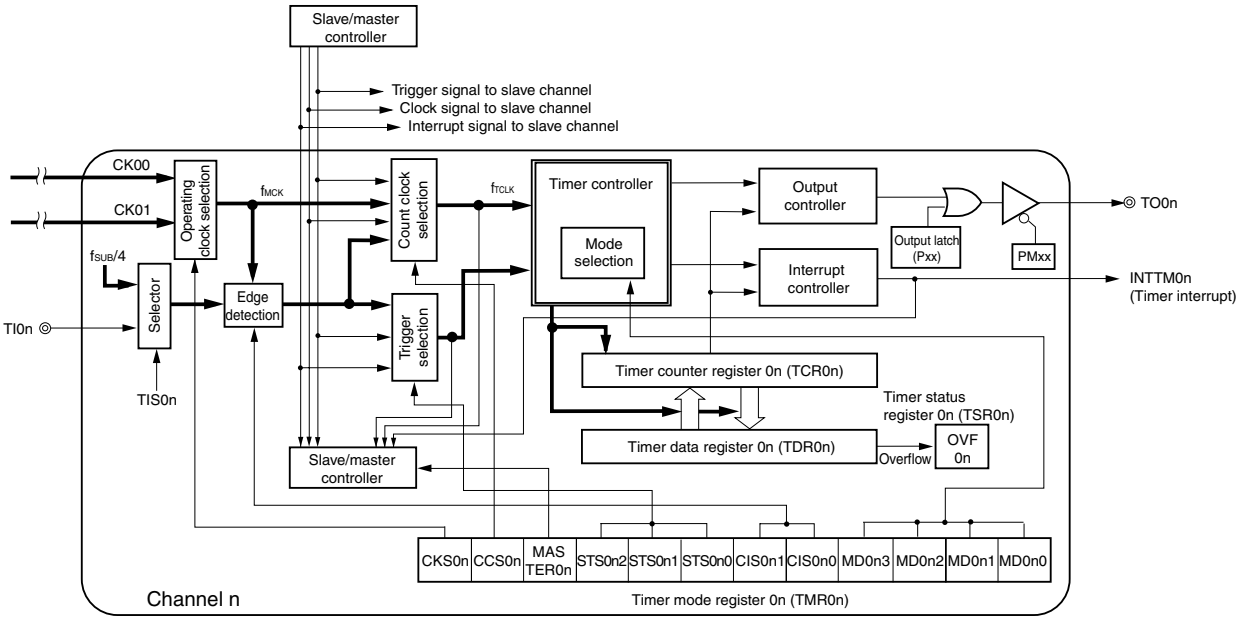



**Figure 8-5. Internal Block Diagram of Channel of Timer Array Unit 0**




**Remark** n = 0 to 7

**(4) Timer status register mn (TSRmn)**

The TSRmn register indicates the overflow status of the counter of channel n.

The TSRmn register is valid only in the capture mode (MDmn3 to MDmn1 = 010B) and capture & one-count mode (MDmn3 to MDmn1 = 110B). It will not be set in any other mode. See Table 8-3 for the operation of the OVF bit in each operation mode and set/clear conditions.

The TSRmn register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the TSRmn register can be set with an 8-bit memory manipulation instruction with TSRmnL.

Reset signal generation clears this register to 0000H.

**Figure 8-12. Format of Timer Status Register mn (TSRmn)**

Address: F01A0H, F01A1H (TSR00) to F01AEH, F01AFH (TSR07) After reset: 0000H R
F01D0H, F01D1H (TSR10) to F01D6H, F01D7H (TSR13)

| Symbol | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSRmn | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OVF |

| OVF | Counter overflow status of channel n |
|---|---|
| 0 | Overflow does not occur. |
| 1 | Overflow occurs. |
| When OVF = 1, this flag is cleared (OVF = 0) when the next value is captured without overflow. | |

**Remark** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

**Table 8-3. OVF Bit Operation and Set/Clear Conditions in Each Operation Mode**

| Timer operation mode | OVF bit | Set/clear conditions |
|---|---|---|
| • Capture mode | clear | When no overflow has occurred upon capturing |
| • Capture & one-count mode | set | When an overflow has occurred upon capturing |
| • Interval timer mode<br>• Event counter mode<br>• One-count mode | clear | – |
| | set | (Use prohibited, not set and not cleared) |

**Remark** The OVF bit does not change immediately after the counter has overflowed, but changes upon the subsequent capture.

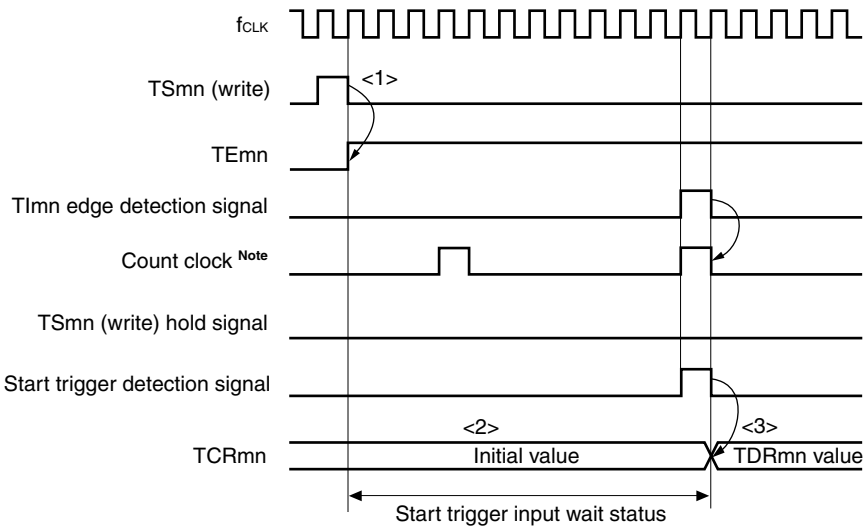
**(d) Start timing in one-count mode**

<1> Operation is enabled (TEmn = 1) by writing 1 to the TSmn bit.

<2> Enters the start trigger input wait status, and timer/counter register mn (TCRmn) holds the initial value.

<3> On start trigger detection, the value of timer data register mn (TDRmn) is loaded to the TCRmn register and count starts.

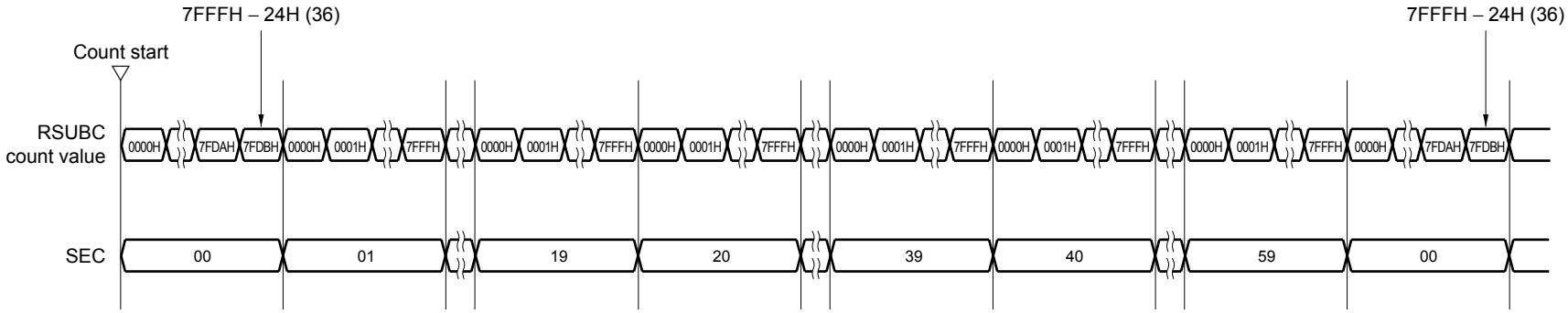
**Figure 8-18. Start Timing (In One-count Mode)**




**Note** When the one-count mode is set, the operation clock ($f_{MCK}$) is selected as count clock (CCSmn = 0).

**Caution An input signal sampling error is generated since operation starts upon start trigger detection (If the TImn pin input signal is used as a start trigger, an error of one count clock occurs.).**

**Figure 9-27. Operation when (DEV, F6, F5, F4, F3, F2, F1, F0) = (1, 1, 1, 0, 1, 1, 1, 0)**



### (5) Analog input channel specification register (ADS)

This register specifies the input channel of the analog voltage to be A/D converted.

The ADS register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Figure 13-8. Format of Analog Input Channel Specification Register (ADS) (1/2)**

Address: FFF31H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ADS | 0 | ADOAS Note 1 | 0 | 0 | ADS3 | ADS2 | ADS1 | ADS0 |

KG3-L, KF3-L, KE3-L, KD3-L, KC3-L (48-pin), KC3-L (44-pin), KC3-L (40-pin)

○ Select mode (ADMD = 0)

| ADOAS Note 1 | ADS3 | ADS2 | ADS1 | ADS0 | Analog input channel | Input source |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | ANI0 | P20/ANI0 pin |
| 0 | 0 | 0 | 0 | 1 | ANI1 | P21/ANI1 pin |
| 0 | 0 | 0 | 1 | 0 | ANI2 | P22/ANI2 pin |
| 0 | 0 | 0 | 1 | 1 | ANI3 | P23/ANI3 pin |
| 0 | 0 | 1 | 0 | 0 | ANI4 | P24/ANI4 pin |
| 0 | 0 | 1 | 0 | 1 | ANI5 | P25/ANI5 pin |
| 0 | 0 | 1 | 1 | 0 | ANI6 | P26/ANI6 pin |
| 0 | 0 | 1 | 1 | 1 | ANI7 | P27/ANI7 pin |
| 0 | 1 | 0 | 0 | 0 | ANI8 | P150/ANI8 pin |
| 0 | 1 | 0 | 0 | 1 | ANI9 | P151/ANI9 pin |
| 0 | 1 | 0 | 1 | 0 | ANI10 | P152/ANI10 pin |
| 0 | 1 | 0 | 1 | 1 | ANI11 | P153/ANI11 pin |
| 0 | 1 | 1 | 0 | 0 | ANI12 | P154/ANI12 pin |
| 0 | 1 | 1 | 0 | 1 | ANI13 | P155/ANI13 pin |
| 0 | 1 | 1 | 1 | 0 | ANI14 | P156/ANI14 pin |
| 0 | 1 | 1 | 1 | 1 | ANI15 | P157/ANI15 pin |
| 1 | × | × | × | × | PGAO | Programmable gain amplifier output signal |
| Other than the above | | | | | Setting prohibited | |

Note 2 Note 2 Note 2 Note 2 Note 2

Note 3 Note 3 Note 3 Note 3

Note 3 Note 2 Note 2 Note 2

**Notes 1.** 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only.

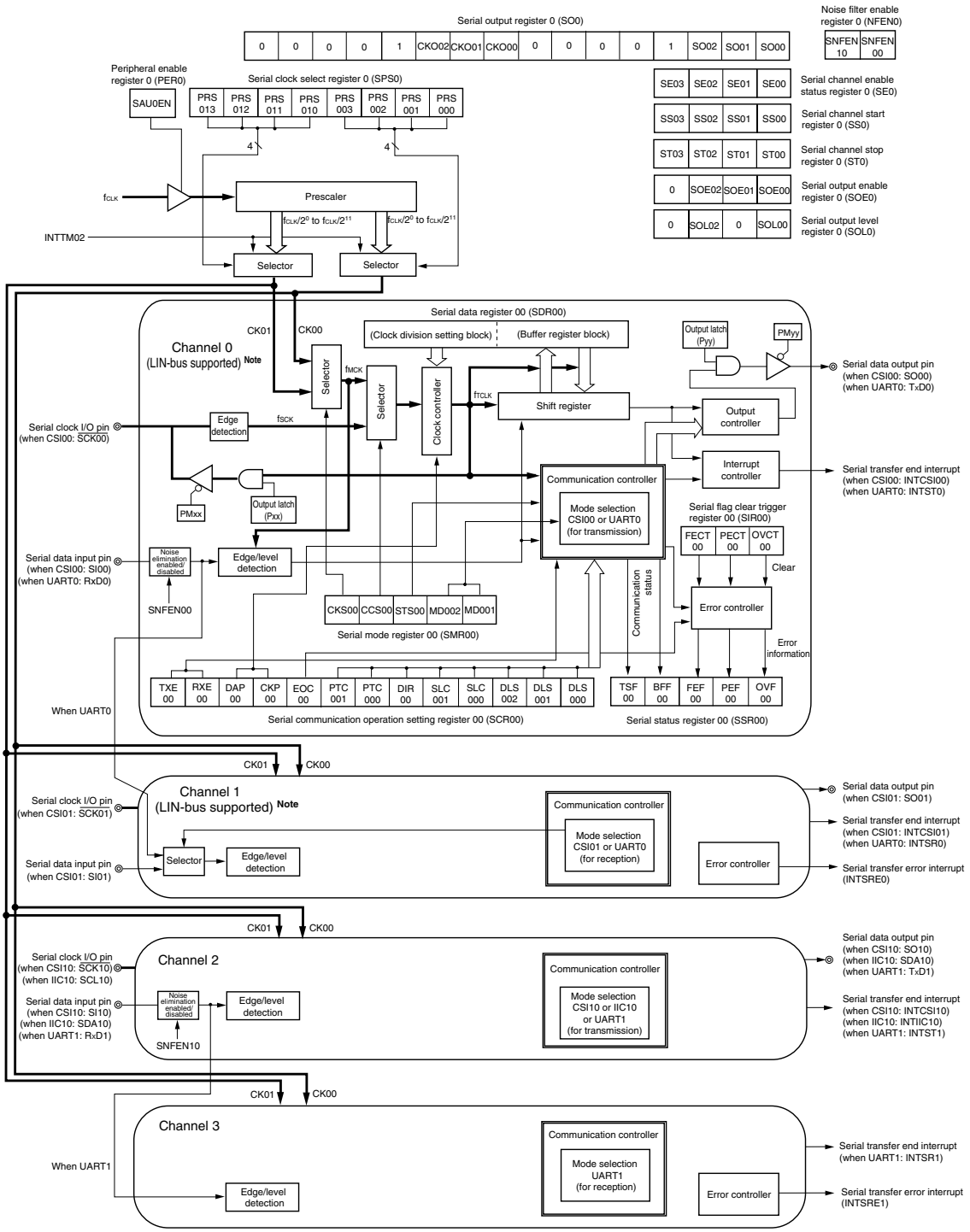
**2.** Setting permitted

**3.** Setting prohibited

(**Cautions** and **Remarks** are listed on the next page.)

Figure 14-1 shows the block diagram of the serial array unit 0.

**Figure 14-1. Block Diagram of Serial Array Unit 0**

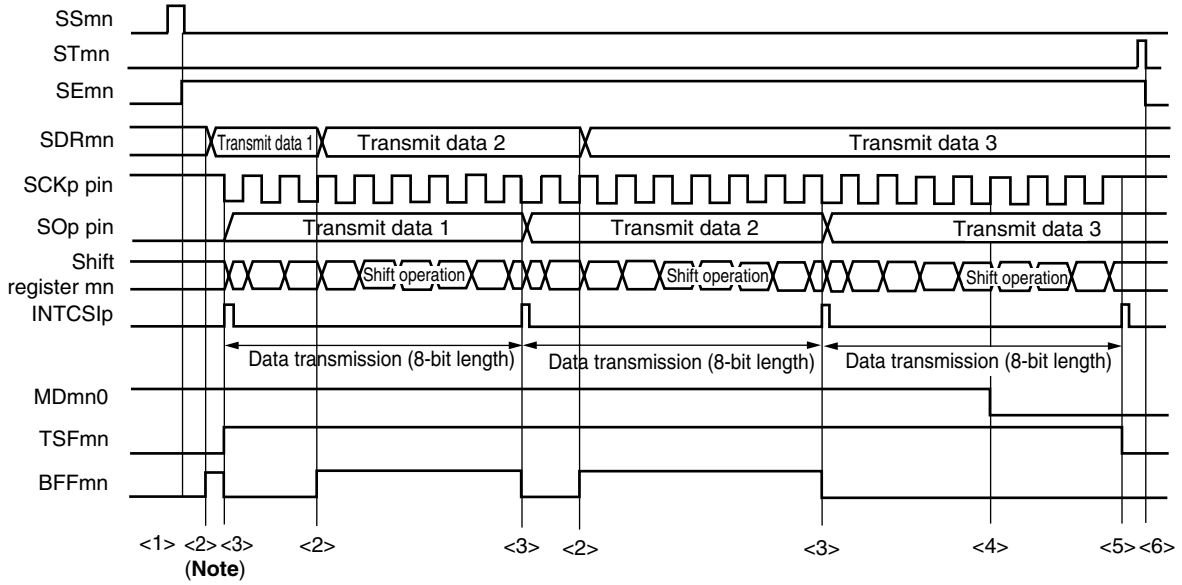



**Note** In the 78K0R/KF3-L and 78K0R/KG3-L, UART3 (unit 1, channels 2 and 3) is used for LIN-bus communication.

**Remark** 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: PMxx, Pxx = PM75, P75 PMyy, Pyy = PM73, P73
78K0R/KF3-L, 78K0R/KG3-L: PMxx, Pxx = PM10, P10 PMyy, Pyy = PM12, P12

### (4) Processing flow (in continuous transmission mode)

**Figure 14-34. Timing Chart of Master Transmission (in Continuous Transmission Mode)**
**(Type 1: DAPmn = 0, CKPmn = 0)**



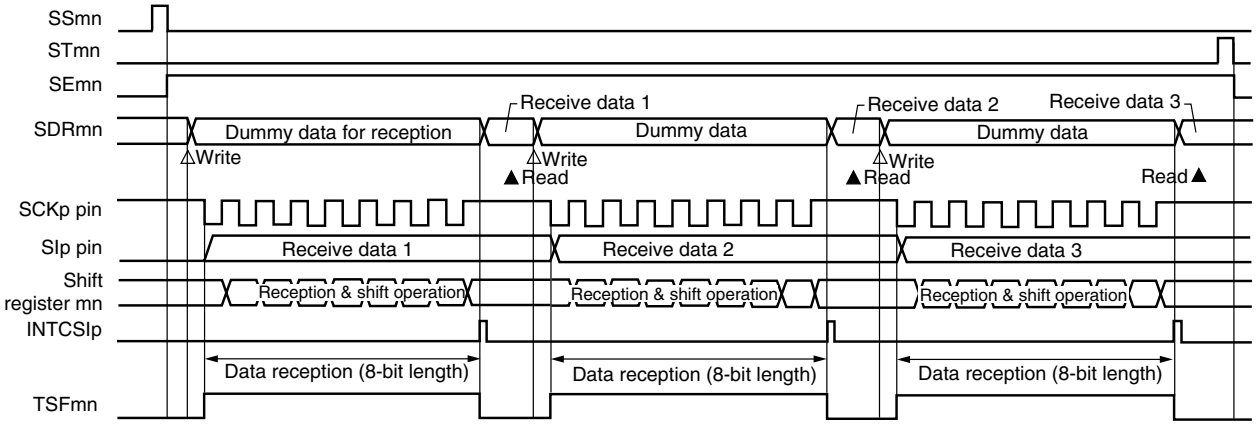

**Note** If transmit data is written to the SDRmn register while the BFFmn bit of serial status register mn (SSRmn) is 1 (valid data is stored in serial data register mn (SDRmn)), the transmit data is overwritten.

**Caution The MDmn0 bit of serial mode register mn (SMRmn) can be rewritten even during operation. However, rewrite it before transfer of the last bit is started, so that it will be rewritten before the transfer end interrupt of the last transmit data.**

**Remark** m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

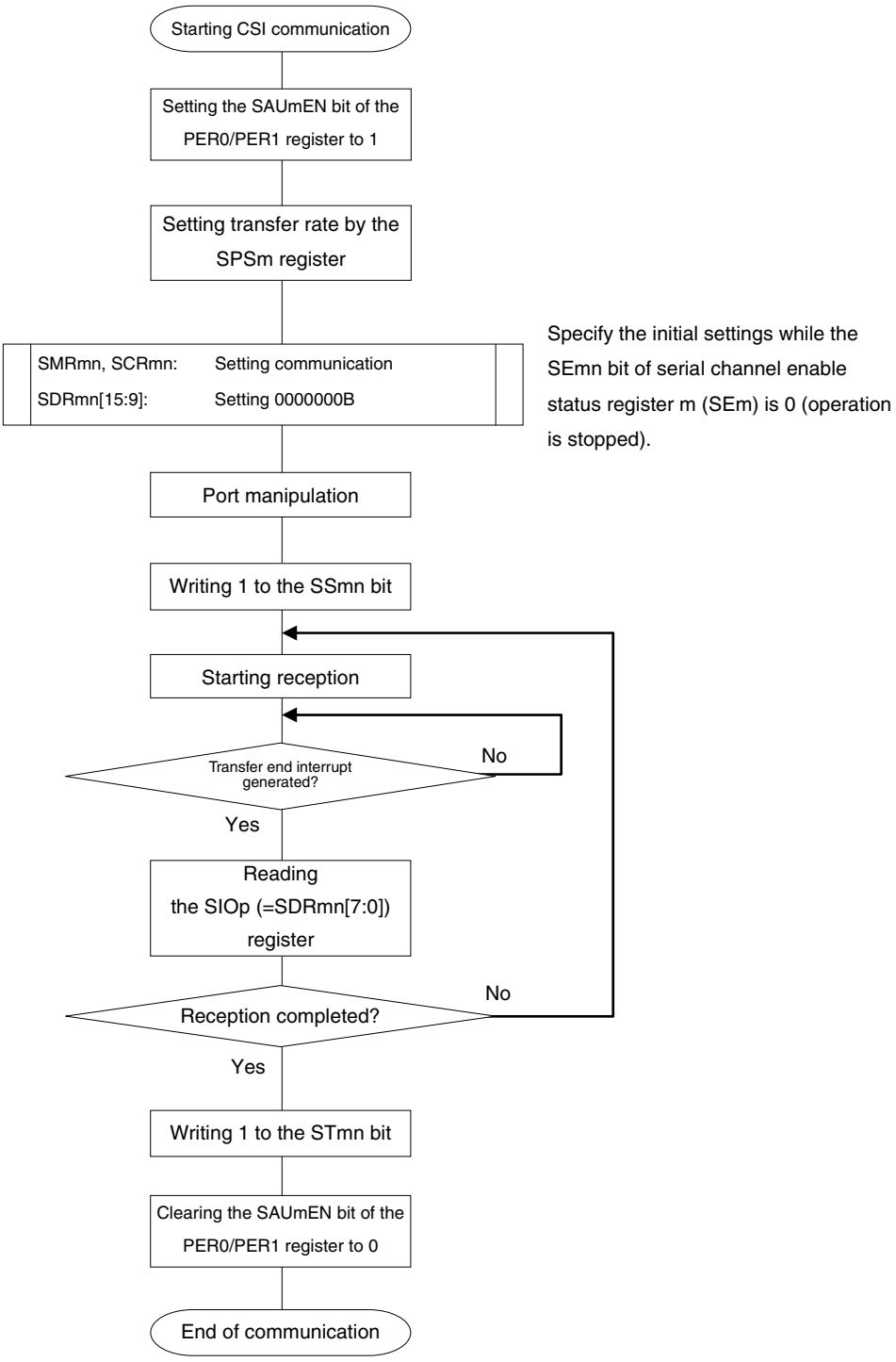
### (3) Processing flow (in single-reception mode)

**Figure 14-40. Timing Chart of Master Reception (in Single-Reception Mode)**
**(Type 1: DAPmn = 0, CKPmn = 0)**




**Remark** m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

**Figure 14-65. Flowchart of Slave Reception (in Single-Reception Mode)**




**Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more $f_{CLK}$ clocks have elapsed.**

**Figure 14-102. Example of Contents of Registers for Data Transmission of Simplified $I^2C$ (IIC10, IIC20)(2/2)**

**(f) Serial channel start register m (SSm) … Do not manipulate this register during data transmission/reception.**

<R>

| SSm | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm3 × | SSm2 0/1 Note 1 | SSm1 × | SSm0 0/1 Note 2 |

**Notes 1.** Serial array unit 0 only.

**2.** The value varies depending on the communication data during communication operation.

**Remarks 1.** m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), r: IIC number (r = 10, 20)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02, r = 10
78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10, r = 10, 20

**2.** ☐ : Setting disabled (set to the initial value)
×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)
0/1: Set to 0 or 1 depending on the usage of the user

**(2) IICA control register 0 (IICCTL0)**

This register is used to enable/stop $I^2C$ operations, set wait timing, and set other $I^2C$ operations.

The IICCTL0 register can be set by a 1-bit or 8-bit memory manipulation instruction. However, set the SPIE, WTIM, and ACKE bits while IICE = 0 or during the wait period. These bits can be set at the same time when the IICE bit is set from “0” to “1”.

Reset signal generation clears this register to 00H.

**Cautions 6. It can be selected by the option byte whether the internal low-speed oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 25 OPTION BYTE.**

**7. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.**

### 20.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

**Remark** For the registers that start, stop, or select the clock, see **CHAPTER 7 CLOCK GENERATOR**.

# CHAPTER 21 RESET FUNCTION

The following five operations are available to generate a reset signal.

(1) External reset input via $\overline{\text{RESET}}$ pin
(2) Internal reset by watchdog timer program loop detection
(3) Internal reset by comparison of supply voltage and detection voltage of power-on-clear (POC) circuit
(4) Internal reset by comparison of supply voltage of the low-voltage detector (LVI) or input voltage (EXLVI) from external input pin, and detection voltage
(5) Internal reset by execution of illegal instruction[Note]
(6) Internal reset by a reset processing check error

External and internal resets start program execution from the address at 0000H and 0001H when the reset signal is generated.

A reset is effected when a low level is input to the $\overline{\text{RESET}}$ pin, the watchdog timer overflows, or by POC and LVI circuit voltage detection or execution of illegal instruction[Note 1], and each item of hardware is set to the status shown in Tables 21-1 and 21-2. Each pin is high impedance during reset signal generation or during the oscillation stabilization time just after a reset release, except for P140[Notes 2, 3], which is low-level output.

When a low level is input to the $\overline{\text{RESET}}$ pin, the device is reset. It is released from the reset status when a high level is input to the $\overline{\text{RESET}}$ pin and program execution is started with the internal high-speed oscillation clock after reset processing. A reset by the watchdog timer is automatically released, and program execution starts using the internal high-speed oscillation clock (see **Figures 21-2** to **21-4**) after reset processing. Reset by POC and LVI circuit supply voltage detection is automatically released when $V_{DD} \geq V_{POR}$ or $V_{DD} \geq V_{LVI}$ after the reset, and program execution starts using the internal high-speed oscillation clock (see **CHAPTER 22 POWER-ON-CLEAR CIRCUIT** and **CHAPTER 23 LOW-VOLTAGE DETECTOR**) after reset processing.

**Notes 1.** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.
**2.** The P140 pin is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.
**3.** Read P140 as P130 if using the 78K0R/KF3-L or 78K0R/KG3-L.

**Cautions 1. For an external reset, input a low level for 10 μs or more to the $\overline{\text{RESET}}$ pin.**
**(To perform an external reset upon power application, a low level of at least 10 μs must be continued during the period in which the supply voltage is within the operating range ($V_{DD} \geq 1.8$ V).)**
**2. During reset input, the X1 clock, XT1 clock (except for 78K0R/KC3-L (40-pin)), internal high-speed oscillation clock, and internal low-speed oscillation clock stop oscillating. External main system clock input becomes invalid.**
**3. When the STOP mode is released by a reset, the RAM contents in the STOP mode are held during reset input.**
**4. When reset is effected, port pin P140 is set to low-level output and other port pins become high-impedance, because each SFR and 2nd SFR are initialized.**

**Remark** $V_{POR}$: POC power supply rise detection voltage

**Cautions 1. Be sure to set bits 7 to 3 to "1".**

**2. Even when the LVI default start function is used, if it is set to LVI operation prohibition by the software (bit 7 (LVION) of the low-voltage detection register (LVIM) is set to 0), it operates as follows:**

- **Does not perform low-voltage detection during LVION = 0.**
- **If a reset is generated while LVION = 0, the LVION bit will be re-set to 1 when the CPU starts after reset release. There is a period when low-voltage detection cannot be performed normally, however, when a reset occurs due to WDT and illegal instruction execution.**
  **This is due to the fact that while the pulse width detected by LVI must be 200 μs max., LVION = 1 is set upon reset occurrence, and the CPU starts operating without waiting for the LVI stabilization time.**

**Figure 25-3. Format of Option Byte (000C2H/010C2H)**

Address: 000C2H/010C2H[Note]

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Note** Be sure to set FFH to 000C2H, as these addresses are reserved areas. Also set FFH to 010C2H when the boot swap operation is used because 000C2H is replaced by 010C2H.

## 25.3 Format of On-chip Debug Option Byte

The format of on-chip debug option byte is shown below.

**Figure 25-4. Format of On-chip Debug Option Byte (000C3H/010C3H)**

Address: 000C3H/010C3H[Note]

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OCDENSET | 0 | 0 | 0 | 0 | 1 | 0 | OCDERSD |

| OCDENSET | OCDERSD | Control of on-chip debug operation |
|---|---|---|
| 0 | 0 | Disables on-chip debug operation. |
| 0 | 1 | Setting prohibited |
| 1 | 0 | Enables on-chip debugging.<br>Erases data of flash memory in case of failures in authenticating on-chip debug security ID. |
| 1 | 1 | Enables on-chip debugging.<br>Does not erases data of flash memory in case of failures in authenticating on-chip debug security ID. |

**Note** Set the same value as 000C3H to 010C3H when the boot swap operation is used because 000C3H is replaced by 010C3H.

**Caution Bits 7 and 0 (OCDENSET and OCDERSD) can only be specified a value.**
**Be sure to set 000010B to bits 6 to 1.**

**Remark** The value on bits 3 to 1 will be written over when the on-chip debug function is in use and thus it will become unstable after the setting.
However, be sure to set the default values (0, 1, and 0) to bits 3 to 1 at setting.

**Table 29-5. Operation List (14/17)**

| Instruction Group | Mnemonic | Operands | Bytes | Clocks | | Operation | Flag | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Note 1 | Note 2 | | Z | AC | CY |
| Bit manipulate | XOR1 | CY, saddr.bit | 3 | 1 | – | CY ← CY ⊻ (saddr).bit | | | × |
| | | CY, sfr.bit | 3 | 1 | – | CY ← CY ⊻ sfr.bit | | | × |
| | | CY, A.bit | 2 | 1 | – | CY ← CY ⊻ A.bit | | | × |
| | | CY, PSW.bit | 3 | 1 | – | CY ← CY ⊻ PSW.bit | | | × |
| | | CY, [HL].bit | 2 | 1 | 4 | CY ← CY ⊻ (HL).bit | | | × |
| | | CY, ES:[HL].bit | 3 | 2 | 5 | CY ← CY ⊻ (ES, HL).bit | | | × |
| | SET1 | saddr.bit | 3 | 2 | – | (saddr).bit ← 1 | | | |
| | | sfr.bit | 3 | 2 | – | sfr.bit ← 1 | | | |
| | | A.bit | 2 | 1 | – | A.bit ← 1 | | | |
| | | !addr16.bit | 4 | 2 | – | (addr16).bit ← 1 | | | |
| | | PSW.bit | 3 | 4 | – | PSW.bit ← 1 | × | × | × |
| | | [HL].bit | 2 | 2 | – | (HL).bit ← 1 | | | |
| | | ES:!addr16.bit | 5 | 3 | – | (ES, addr16).bit ← 1 | | | |
| | | ES:[HL].bit | 3 | 3 | – | (ES, HL).bit ← 1 | | | |
| | CLR1 | saddr.bit | 3 | 2 | – | (saddr.bit) ← 0 | | | |
| | | sfr.bit | 3 | 2 | – | sfr.bit ← 0 | | | |
| | | A.bit | 2 | 1 | – | A.bit ← 0 | | | |
| | | !addr16.bit | 4 | 2 | – | (addr16).bit ← 0 | | | |
| | | PSW.bit | 3 | 4 | – | PSW.bit ← 0 | × | × | × |
| | | [HL].bit | 2 | 2 | – | (HL).bit ← 0 | | | |
| | | ES:!addr16.bit | 5 | 3 | – | (ES, addr16).bit ← 0 | | | |
| | | ES:[HL].bit | 3 | 3 | – | (ES, HL).bit ← 0 | | | |
| | SET1 | CY | 2 | 1 | – | CY ← 1 | | | 1 |
| | CLR1 | CY | 2 | 1 | – | CY ← 0 | | | 0 |
| | NOT1 | CY | 2 | 1 | – | CY ← $\overline{CY}$ | | | × |

**Notes 1.** When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

**2.** When the program memory area is accessed.

**Remarks 1.** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$) selected by the system clock control register (CKC).

**2.** This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $EV_{DD}$ ≤ 5.5 V, 1.8 V ≤ $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS}$ = $AV_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low[Note 1] | $I_{OL1}$ | Per pin for P00, P01, P10 to P17, P30, P33, P40 to P43, P50 to P53, P70 to P77, P120, P140, P141 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 8.5 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 1.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 0.5 | mA |
| | | Per pin for P31, P32 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 8.5 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 1.5 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 0.6 | mA |
| | | Per pin for P60, P61 | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 15.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 3.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 2.0 | mA |
| | | Total of P00, P01, P40 to P43, P120, P140, P141 (When duty = 70%[Note 2]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 20.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P10 to P17, P30 to P33, P50 to P53, P60, P61, P70 to P77 (When duty = 70%[Note 2]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 45.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty = 60%[Note 2]) | 4.0 V ≤ $V_{DD}$ ≤ 5.5 V | | | 65.0 | mA |
| | | | 2.7 V ≤ $V_{DD}$ < 4.0 V | | | 40.0 | mA |
| | | | 1.8 V ≤ $V_{DD}$ < 2.7 V | | | 29.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P80 to P83, P150 to P153 | $AV_{REF}$ = $V_{DD}$ | | | 0.4 | mA |

**Notes 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS}$, $V_{SS}$, and $AV_{SS}$ pins.

**2.** Specification under conditions where the duty factor is 60% or 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
• Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)
<Example> Where n = 50% and $I_{OL}$ = 20.0 mA
Total output current of pins = (20.0 × 0.7)/(50 × 0.01) = 28.0 mA
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

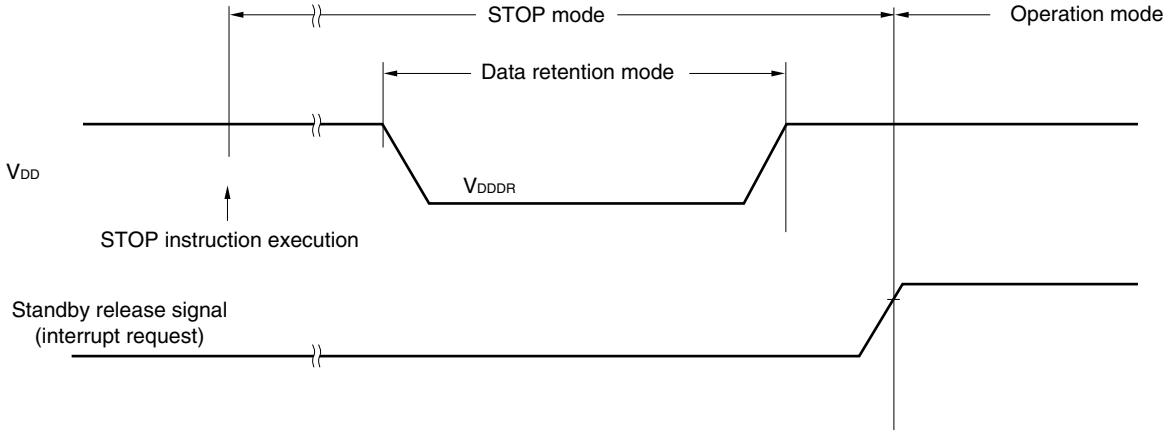
**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

## 31.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

**($T_A$ = –40 to +85°C)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.5[Note] | | 5.5 | V |

**Note** The value depends on the POC detection voltage. When the voltage drops, the data is retained before a POC reset is effected, but data is not retained when a POC reset is effected.




## 31.8 Flash Memory Programming Characteristics

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $EV_{DD0}$ = $EV_{DD1}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ supply current | $I_{DD}$ | Typ. = 10 MHz, Max. = 20 MHz | | 6 | 20 | mA |
| Number of rewrites (number of deletes per block) | $C_{erwr}$ | Used for updating programs<br>When using flash memory programmer and Renesas Electronics self programming library | Retained for 15 years | 1,000 | | Times |
| | | Used for updating data<br>When using Renesas Electronics EEPROM emulation library (available ROM area: 3 to 8 KB of 3 to 8 continuous blocks ) | Retained for 5 years | 10,000 | | Times |

**Remark** When updating data multiple times, use the flash memory as one for updating data.