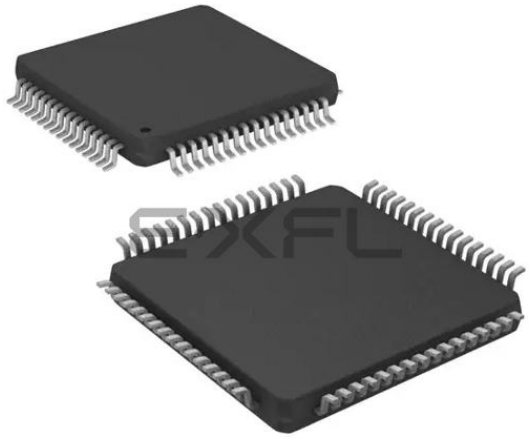
Renesas Electronics America Inc - UPD78F1007GA-HAB-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1007ga-hab-ax

(1) Port functions (2/2): 78K0R/KC3-L (40-pin)

Function Name	I/O	Function	After Reset	Alternate Function
P80	I/O	Port 8. 3-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80, P81, and P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 2-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P150, P151	I/O	Port 15. 2-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8, ANI9

(1) Port functions (2/2): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7. 8-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$
P76				KR6
P77				KR7
P80	I/O	Port 8. 4-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P82				CMP1P/INTP7
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P140	Output	Port 14. 1-bit output port.	Output port	PCLBUZ0
P150 to P152	I/O	Port 15. 3-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI10

3.2 Description of Pin Functions

Remark The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **3.1 Pin Function List**.

3.2.1 P00 to P06 (port 0)

P00 to P06 function as an I/O port. These pins also function as timer I/O, serial interface data I/O, and clock I/O.

Input to the P03 and P04 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 0 (PIM0).

Output from the P02 to P04 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 0 (POM0).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P00/TI00	–[Note 1]	√
P01/TO00	–[Note 1]	√
P02/SO10/TxD1	√	√
P03/SI10/RxD1/SDA10	√	√
P04/$\overline{SCK10}$/SCL10	√	√
P05/TI05/TO05	√	P05[Note 2]
P06/TI06/TO06	√	P06[Note 2]

Notes 1. TI00 and TO00 are shared with P53 and P52, respectively, in the 78K0R/KF3-L.

2. TI05/TO05 and TI06/TO06 are shared with P46 and P131, respectively, in the 78K0R/KG3-L.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 to P06 function as an I/O port. P00 to P06 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 to P04 function as timer I/O, serial interface data I/O, and clock I/O.

(a) TI00, TI05, and TI06

There are the pins for inputting an external count clock/capture trigger to 16-bit timers 00, 05, and 06.

(b) TO00, TO05, and TO06

These are the timer output pins of 16-bit timers 00, 05, and 06.

(c) SI10

This is a serial data input pin of serial interface CSI10.

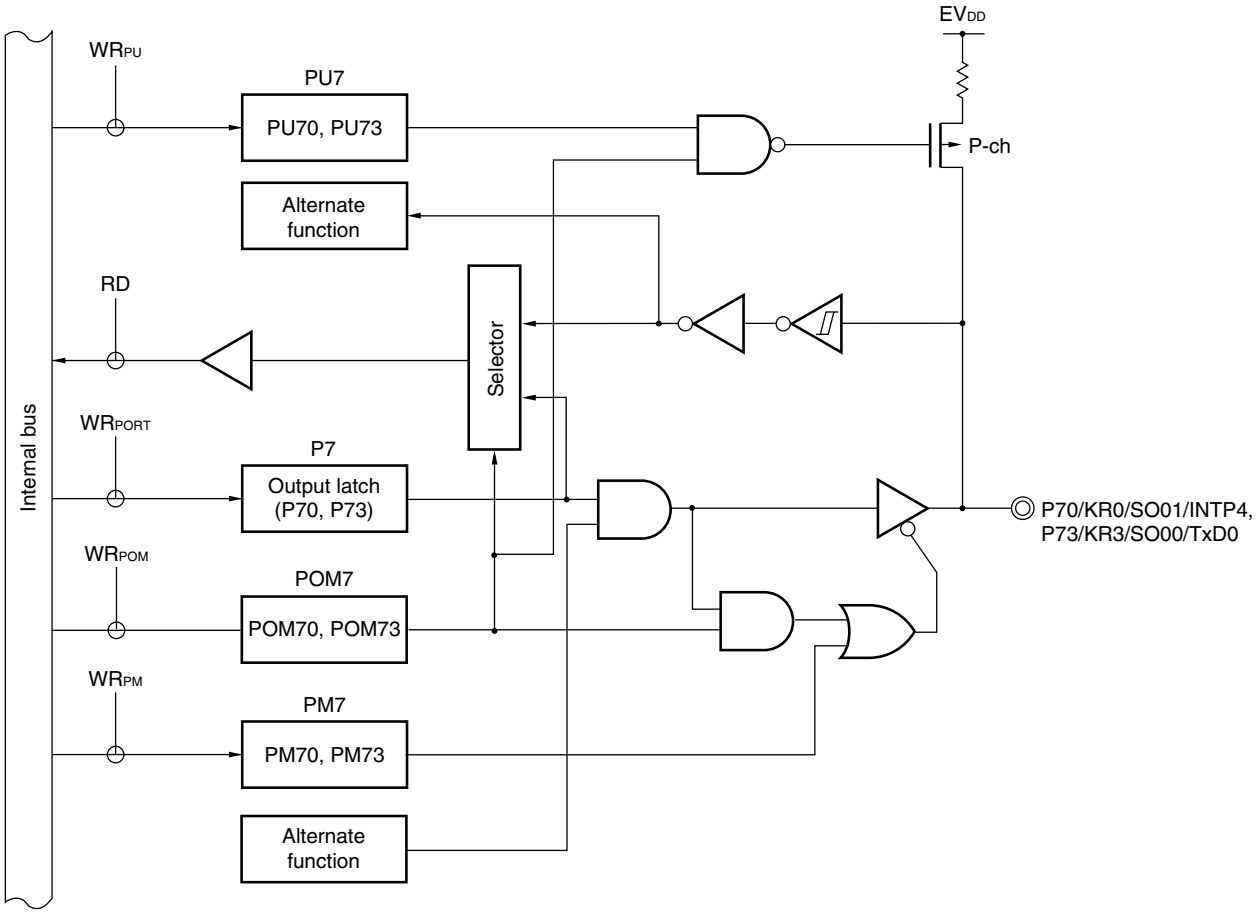
(d) SO10

This is a serial data output pin of serial interface CSI10.

Table 4-6. Extended SFR (2nd SFR) List (4/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0158H	Serial communication operation setting register 10	SCR10		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F0159H															
F015AH	Serial communication operation setting register 11	SCR11		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015BH															
F015CH	Serial communication operation setting register 12	SCR12		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015DH															
F015EH	Serial communication operation setting register 13	SCR13		R/W	–	–	√	0087H	–	–	–	–	–	√	√
F015FH															
F0160H	Serial channel enable status register 1	SE1L	SE1	R	√	√	√	0000H	–	–	–	–	–	√	√
F0161H		–			–	–			–	–	–	–	–	√	√
F0162H	Serial channel start register 1	SS1L	SS1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F0163H		–			–	–			–	–	–	–	–	√	√
F0164H	Serial channel stop register 1	ST1L	ST1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F0165H		–			–	–			–	–	–	–	–	√	√
F0166H	Serial clock select register 1	SPS1L	SPS1	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0167H		–			–	–			–	–	–	–	–	√	√
F0168H	Serial output register 1	SO1		R/W	–	–	√	0F0FH	–	–	–	–	–	√	√
F0169H															
F016AH	Serial output enable register 1	SOE1L	SOE1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F016BH		–			–	–			–	–	–	–	–	√	√
F0174H	Serial output level register 1	SOL1L	SOL1	R/W	–	√	√	0000H	–	–	–	–	–	√	√
F0175H		–			–	–			–	–	–	–	–	√	√
F0180H	Timer counter register 00	TCR00		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0181H															
F0182H	Timer counter register 01	TCR01		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0183H															
F0184H	Timer counter register 02	TCR02		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0185H															
F0186H	Timer counter register 03	TCR03		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0187H															
F0188H	Timer counter register 04	TCR04		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F0189H															
F018AH	Timer counter register 05	TCR05		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018BH															
F018CH	Timer counter register 06	TCR06		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018DH															
F018EH	Timer counter register 07	TCR07		R	–	–	√	FFFFH	√	√	√	√	√	√	√
F018FH															

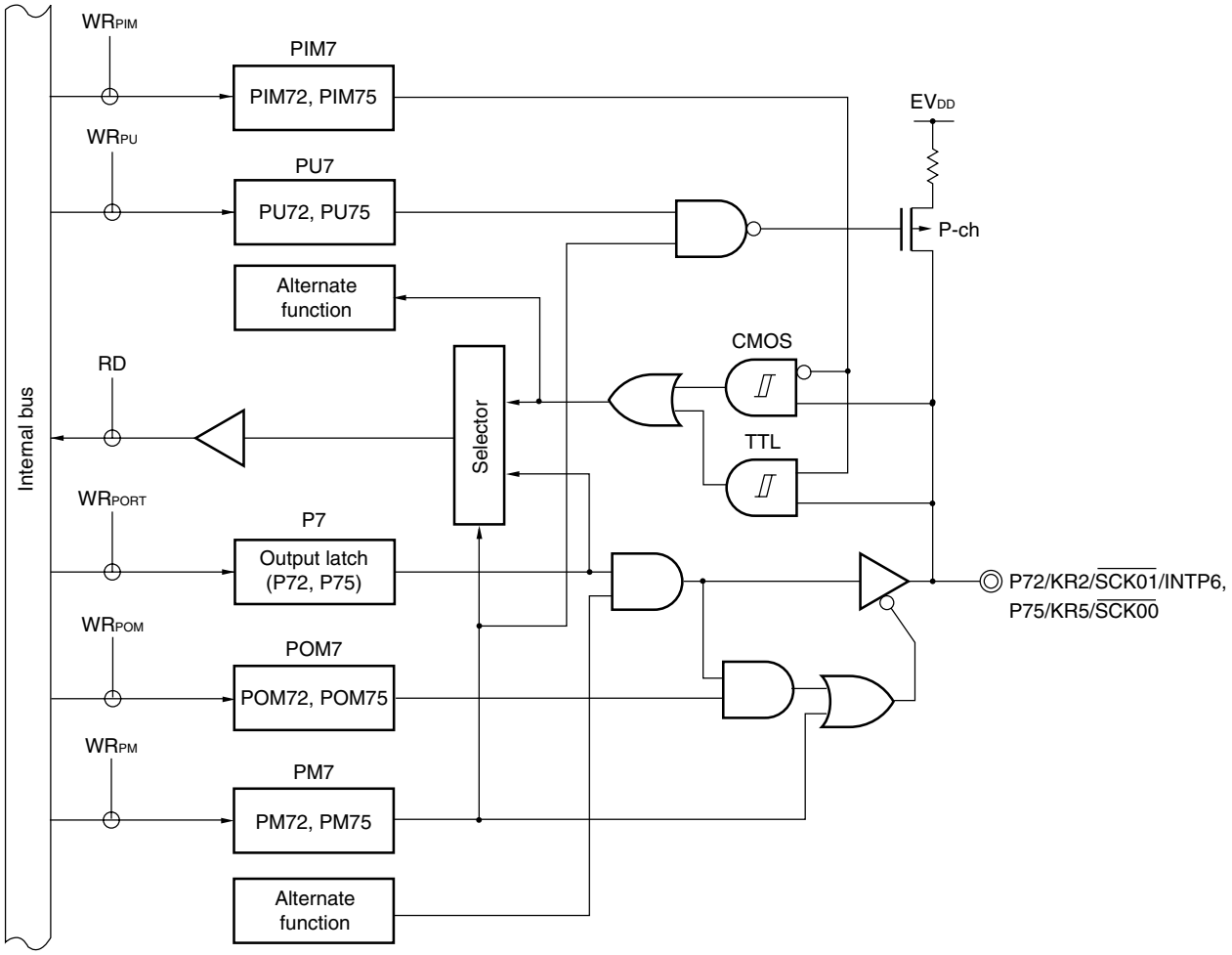
Figure 5-15. Block Diagram of P70 and P73



P7: Port register 7
PU7: Pull-up resistor option register 7
POM7: Port output mode register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 5-17. Block Diagram of P72 and P75



P7: Port register 7
PU7: Pull-up resistor option register 7
PM7: Port mode register 7
PIM7: Port input mode register 7
POM7: Port output mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

Figure 6-54. Format of Port Register (78K0R/KF3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	P06	P05	P04	P03	P02	0	0	FFF00H	00H (output latch)	R/W
P1	P17	P16	P15	P14	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	0	P31	P30	FFF03H	00H (output latch)	R/W
P4	P47	P46	P45	P44	P43	P42	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	P55	P54	P53	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	P67	P66	P65	P64	P63	P62	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P9	0	0	0	0	0	0	P91	P90	FFF09H	00H (output latch)	R/W
P11	0	0	0	0	0	0	P111	P110	FFF0BH	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P13	0	0	0	0	0	0	0	P130	FFF0DH	00H (output latch)	R/W
P14	0	0	0	P144	P143	P142	0	P140	FFF0EH	00H (output latch)	R/W
P15	0	0	0	0	P153	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 7, 9, 11 to 15; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Note P121 to P124 are read-only.

(2) System clock control register (CKC)

This register is used to select a CPU/peripheral hardware clock and a division ratio.

The CKC register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 09H.

Figure 7-5. Format of System Clock Control Register (CKC)

Address: FFFA4H After reset: 09H R/W[Note 1]

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
CKC	CLS[Note 2]	CSS	MCS	MCM0	1	MDIV2	MDIV1	MDIV0

CLS[Note 2]	Status of CPU/peripheral hardware clock (f_{CLK})
0	Main system clock (f_{MAIN})
1	Subsystem clock divided by 2 ($f_{SUB}/2$)

MCS	Status of Main system clock (f_{MAIN})
0	Internal high-speed oscillation clock (f_{IH}) or 20 MHz internal high-speed oscillation clock (f_{IH20})
1	High-speed system clock (f_{MX})

MCM0	Main system clock (f_{MAIN}) operation control
0	Selects the internal high-speed oscillation clock (f_{IH}) or 20 MHz internal high-speed oscillation clock (f_{IH20}) as the main system clock (f_{MAIN})
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN})

CSS	MDIV2	MDIV1	MDIV0	Selection of CPU/peripheral hardware clock (f_{CLK})
0	0	0	0	f_{MAIN}
	0	0	1	$f_{MAIN}/2$ (This is the default setting if MCM0 = 0.)
	0	1	0	$f_{MAIN}/2^2$
	0	1	1	$f_{MAIN}/2^3$ [Note 3]
	1	0	0	$f_{MAIN}/2^4$ [Note 3]
	1	0	1	$f_{MAIN}/2^5$ [Notes 3, 4]
1 [Note 5]	×	×	×	$f_{SUB}/2$
Other than above				Setting prohibited

Notes 1. Bits 7 and 5 are read-only.

2. CLS bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), bit 7 is fixed to 0.

3. Setting is prohibited if the 1 MHz Internal high-speed oscillation clock frequency (f_{IH1}) is selected as the main system clock (f_{MAIN}).

4. Setting is prohibited if the high-speed system clock (f_{MX}) is selected as the main system clock (f_{MAIN}) and if $f_{MX} < 4$ MHz.

5. Changing the value of the MCM0 bit is prohibited while the CSS bit is set to 1.

(**Remarks** and **Cautions** are listed on the next page.)

Table 7-5. Changing CPU Clock (2/2)

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Subsystem clock[Note]	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • HIOSTOP = 0, MCS = 0	XT1 oscillation can be stopped (XTSTOP = 1)
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 0, MSTOP = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from the EXCLK pin and selection of high-speed system clock as main system clock • OSCSEL = 1, EXCLK = 1, MSTOP = 0 • MCS = 1	
	20 MHz internal high-speed oscillation clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
20 MHz internal high-speed oscillation clock	Internal high-speed oscillation clock	• SELDSC = 0 (Set when changing the clock.)	20 MHz internal high-speed oscillation clock can be stopped (DSCON = 0)
	X1 clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
	External main system clock	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–
	Subsystem clock[Note]	Transition cannot be performed unless the clock is changed to the internal high-speed oscillation clock once.	–

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

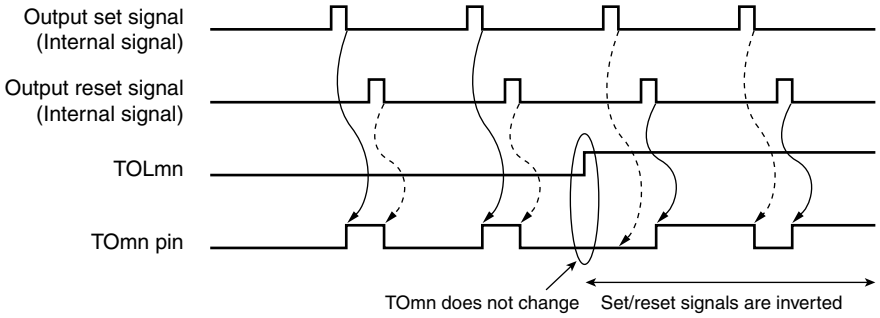
(3) Operation of TOmn pin in slave channel output mode (TOMmn = 1)

(a) When timer output level register m (TOLm) setting has been changed during timer operation

When the TOLm register setting has been changed during timer operation, the setting becomes valid at the generation timing of the TOmn pin change condition. Rewriting the TOLm register does not change the output level of the TOmn pin.

The operation when TOMmn is set to 1 and the value of the TOLm register is changed while the timer is operating (TEmn = 1) is shown below.

Figure 8-34. Operation when TOLm Register Has Been Changed during Timer Operation



Remarks 1. Set: The output signal of the TOmn pin changes from inactive level to active level.
Reset: The output signal of the TOmn pin changes from active level to inactive level.

2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Here is an example of setting the alarm.

Time of Alarm	Day							12-Hour Display				24-Hour Display			
	Sunday WW0	Monday WW1	Tuesday WW2	Wednesday WW3	Thursday WW4	Friday WW5	Saturday WW6	Hour 10	Hour 1	Minute 10	Minute 1	Hour 10	Hour 1	Minute 10	Minute 1
Every day, 0:00 a.m.	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
Every day, 1:30 a.m.	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
Every day, 11:59 a.m.	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
Monday through Friday, 0:00 p.m.	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
Sunday, 1:30 p.m.	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
Monday, Wednesday, Friday, 11:59 p.m.	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

13.4.3 A/D converter operation modes

The select mode and scan mode are provided as the A/D converter operation modes.

(1) Select mode

One analog input specified by the analog input channel specification register (ADS), while the ADMD bit of the A/D converter mode register (ADM) is 0, is A/D converted.

When A/D conversion is complete, the conversion result is stored in the A/D conversion result register (ADCR) and the A/D conversion end interrupt request signal (INTAD) is generated.

After A/D conversion has been completed, A/D conversion is repeated successively, unless the ADCS bit is set to 0.

If anything is written to the ADM or ADS register during conversion, A/D conversion is aborted. In this case, A/D conversion is started again from the beginning.

Figure 13-14. Example of Select Mode Operation Timing

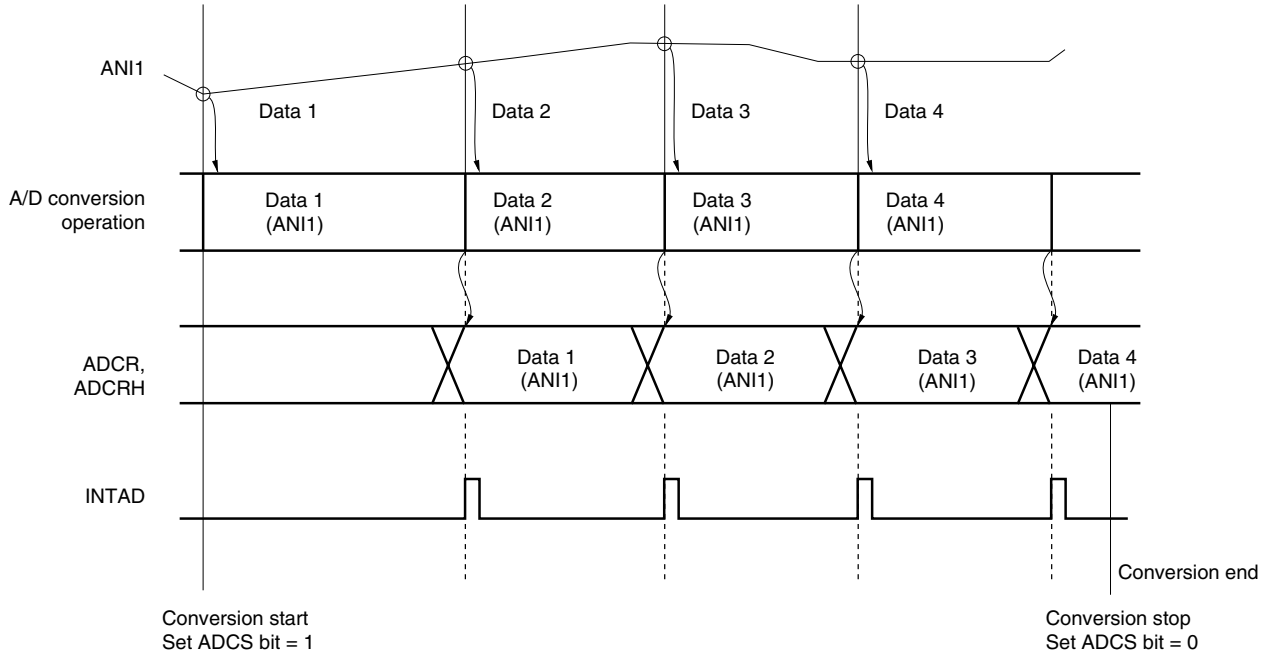
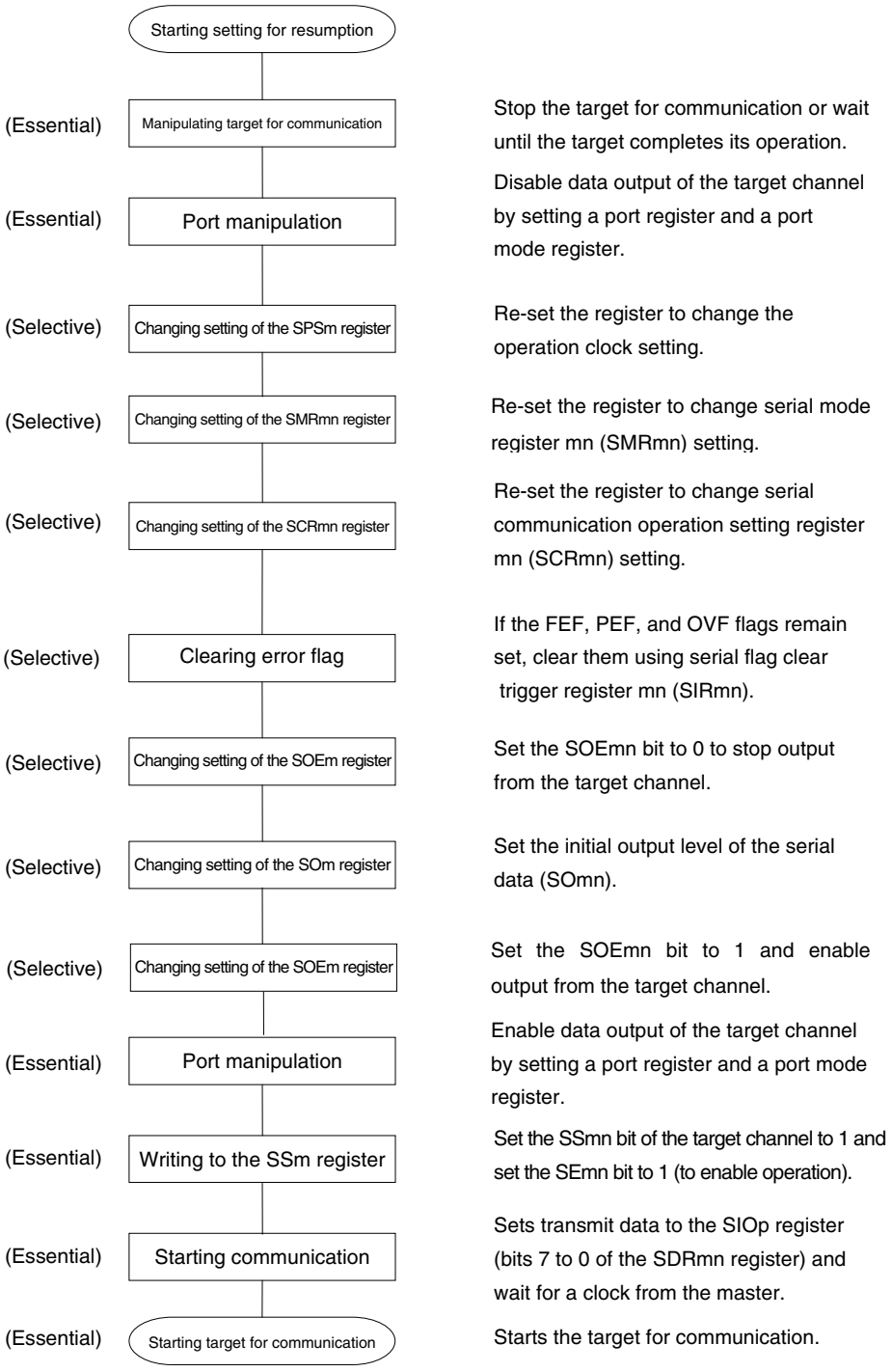


Figure 14-69. Procedure for Resuming Slave Transmission/Reception



Caution Be sure to set transmit data to the SIOp register before the clock from the master is started.

Figure 15-4. Format of Slave Address Register (SVA)

Address: F0234H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
SVA	A6	A5	A4	A3	A2	A1	A0	0Note

Note Bit 0 is fixed to 0.

(3) SO latch

The SO latch is used to retain the SDA0 pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request (INTIICA) when the address received by this register matches the address value set to the slave address register (SVA) or when an extension code is received.

(5) Serial clock counter

This counter counts the serial clocks that are output or input during transmit/receive operations and is used to verify that 8-bit data was transmitted or received.

(6) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICA).

An I^2C interrupt request is generated by the following two triggers.

- Falling edge of eighth or ninth clock of the serial clock (set by the WTIM bit)
- Interrupt request generated when a stop condition is detected (set by the SPIE bit)

Remark WTIM bit: Bit 3 of IICA control register 0 (IICCTL0)
SPIE bit: Bit 4 of IICA control register 0 (IICCTL0)

(7) Serial clock controller

In master mode, this circuit generates the clock output via the SCL0 pin from a sampling clock.

(8) Serial clock wait controller

This circuit controls the wait timing.

(9) ACK generator, stop condition detector, start condition detector, and ACK detector

These circuits generate and detect each status.

(10) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(11) Start condition generator

This circuit generates a start condition when the STT bit is set to 1.

However, in the communication reservation disabled status (IICRSV bit = 1), when the bus is not released (IICBSY bit = 1), start condition requests are ignored and the STCF bit is set to 1.

(12) Stop condition generator

This circuit generates a stop condition when the SPT bit is set to 1.

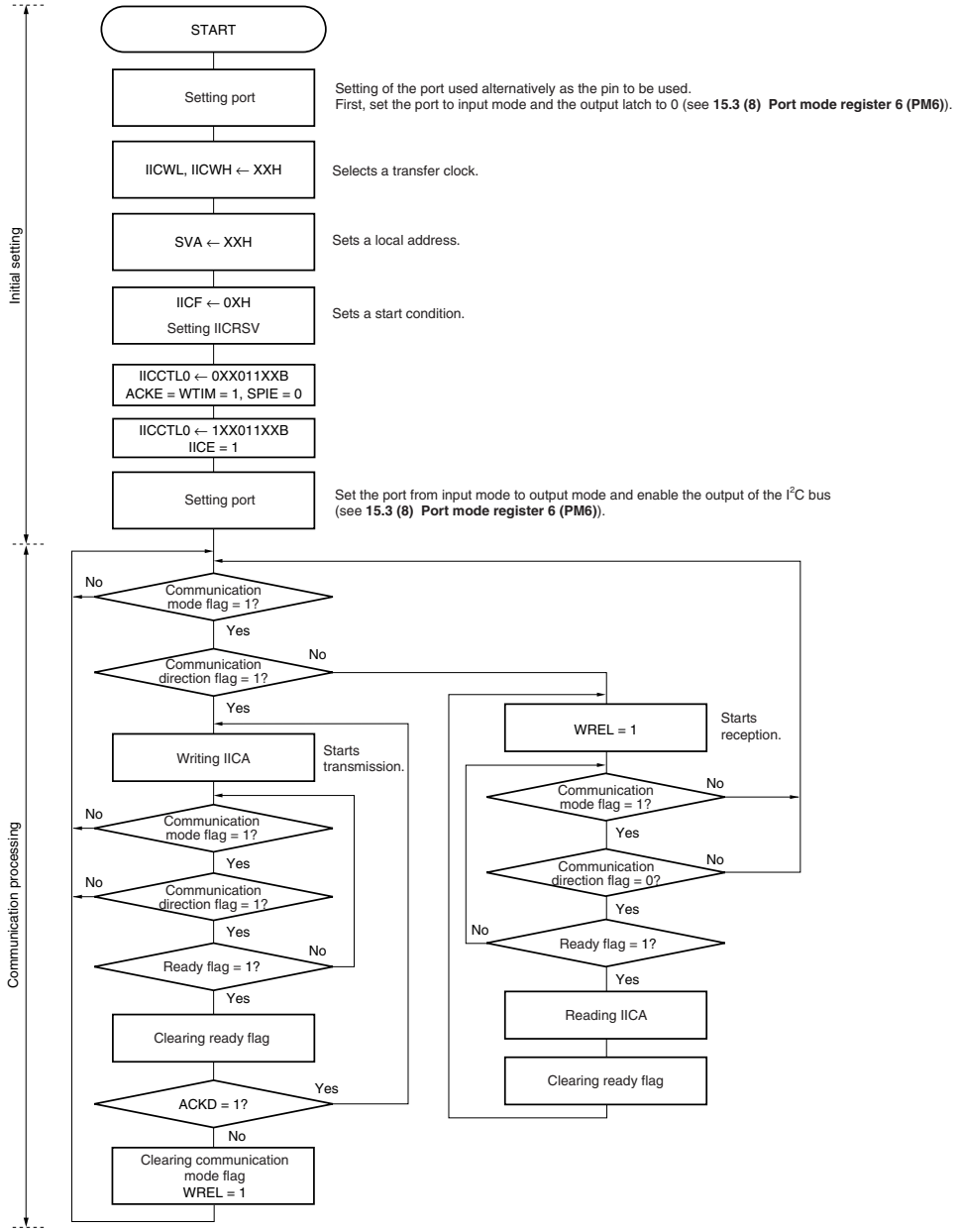
The main processing of the slave operation is explained next.

Start serial interface IICA and wait until communication is enabled. When communication is enabled, execute communication by using the communication mode flag and ready flag (processing of the stop condition and start condition is performed by an interrupt. Here, check the status by using the flags).

The transmission operation is repeated until the master no longer returns $\overline{ACK}$. If $\overline{ACK}$ is not returned from the master, communication is completed.

For reception, the necessary amount of data is received. When communication is completed, $\overline{ACK}$ is not returned as the next data. After that, the master generates a stop condition or restart condition. Exit from the communication status occurs in this way.

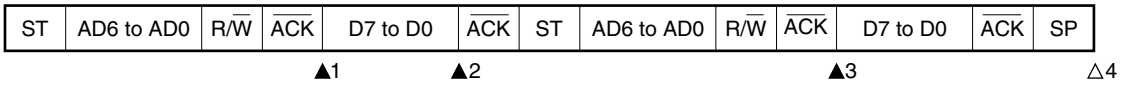
Figure 15-30. Slave Operation Flowchart (1)



Remark Conform to the specifications of the product that is in communication, regarding the transmission and reception formats.

(d) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

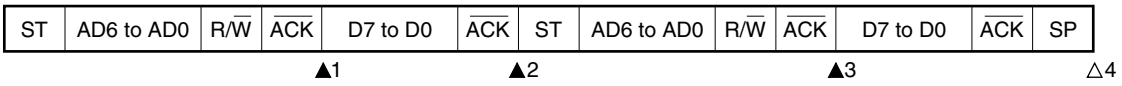
(i) When WTIM = 0 (after restart, does not match address (= not extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 00000110B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1 (after restart, does not match address (= not extension code))



▲1: IICS = 0001×110B
▲2: IICS = 0001××00B
▲3: IICS = 00000110B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

The meanings of <1> to <6> in (1) Start condition ~ address ~ data in Figure 15-32 are explained below.

<R> <1> The start condition trigger is set by the master device (STT = 1) and a start condition (i.e. SCL0 = 1 changes SDA0 from 1 to 0) is generated once the bus data line goes low (SDA0). When the start condition is subsequently detected, the master device enters the master device communication status (MSTS = 1). The master device is ready to communicate once the bus clock line goes low (SCL0 = 0) after the hold time has elapsed.

<2> The master device writes the address + W (transmission) to the IICA shift register (IICA) and transmits the slave address.

<R> <3> In the slave device if the address received matches the address (SVA value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<R> <4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCL0 = 0) and issues an interrupt (INTIICA: address match)[Note].

<5> The master device writes the data to transmit to the IICA register and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL = 1), the master device starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

(1) Multiplication/division data register A (MDAH, MDAL)

The MDAH and MDAL registers set the values that are used for a multiplication or division operation and store the operation result. They set the multiplier and multiplicand data in the multiplication mode, and set the dividend data in the division mode. Furthermore, the operation result (quotient) is stored in the MDAH and MDAL registers in the division mode.

The MDAH and MDAL registers can be set by a 16-bit manipulation instruction.

Reset signal generation clears these registers to 0000H.

Figure 16-2. Format of Multiplication/Division Data Register A (MDAH, MDAL)

Address: FFFF0H, FFFF1H, FFFF2H, FFFF3H After reset: 0000H, 0000H R/W

Symbol FFFF3H FFFF2H

MDAH	MDAH 15	MDAH 14	MDAH 13	MDAH 12	MDAH 11	MDAH 10	MDAH 9	MDAH 8	MDAH 7	MDAH 6	MDAH 5	MDAH 4	MDAH 3	MDAH 2	MDAH 1	MDAH 0

Symbol FFFF1H FFFF0H

MDAL	MDAL 15	MDAL 14	MDAL 13	MDAL 12	MDAL 11	MDAL 10	MDAL 9	MDAL 8	MDAL 7	MDAL 6	MDAL 5	MDAL 4	MDAL 3	MDAL 2	MDAL 1	MDAL 0

Cautions 1. Do not rewrite the MDAH and MDAL registers values during division operation processing (while the multiplication/division control register (MDUC) is 81H). The operation will be executed in this case, but the operation result will be an undefined value.

2. The MDAH and MDAL registers values read during division operation processing (while MDUC is 81H) will not be guaranteed.

The following table shows the functions of the MDAH and MDAL registers during operation execution.

Table 16-2. Functions of MDAH and MDAL Registers During Operation Execution

DIVMODE	Operation Mode	Setting	Operation Result
0	Multiplication mode	MDAH: Multiplier MDAL: Multiplicand	–
1	Division mode	MDAH: Divisor (higher 16 bits) MDAL: Dividend (lower 16 bits)	MDAH: Division result (quotient) Higher 16 bits MDAL: Division result (quotient) Lower 16 bits

Remark DIVMODE: Bit 7 of the multiplication/division control register (MDUC)

29.2 Operation List

Table 29-5. Operation List (1/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
8-bit data transfer	MOV	r, #byte	2	1	–	r ← byte			
		saddr, #byte	3	1	–	(saddr) ← byte			
		sfr, #byte	3	1	–	sfr ← byte			
		!addr16, #byte	4	1	–	(addr16) ← byte			
		A, r Note 3	1	1	–	A ← r			
		r, A Note 3	1	1	–	r ← A			
		A, saddr	2	1	–	A ← (saddr)			
		saddr, A	2	1	–	(saddr) ← A			
		A, sfr	2	1	–	A ← sfr			
		sfr, A	2	1	–	sfr ← A			
		A, !addr16	3	1	4	A ← (addr16)			
		!addr16, A	3	1	–	(addr16) ← A			
		PSW, #byte	3	3	–	PSW ← byte	×	×	×
		A, PSW	2	1	–	A ← PSW			
		PSW, A	2	3	–	PSW ← A	×	×	×
		ES, #byte	2	1	–	ES ← byte			
		ES, saddr	3	1	–	ES ← (saddr)			
		A, ES	2	1	–	A ← ES			
		ES, A	2	1	–	ES ← A			
		CS, #byte	3	1	–	CS ← byte			
		A, CS	2	1	–	A ← CS			
		CS, A	2	1	–	CS ← A			
		A, [DE]	1	1	4	A ← (DE)			
		[DE], A	1	1	–	(DE) ← A			
		[DE + byte], #byte	3	1	–	(DE + byte) ← byte			
		A, [DE + byte]	2	1	4	A ← (DE + byte)			
		[DE + byte], A	2	1	–	(DE + byte) ← A			
		A, [HL]	1	1	4	A ← (HL)			
		[HL], A	1	1	–	(HL) ← A			
		[HL + byte], #byte	3	1	–	(HL + byte) ← byte			

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

2. When the program memory area is accessed.

3. Except r = A

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	13.6 MHz < f_{MCK}	10/f_{MCK}			ns
			6.8 MHz < f_{MCK} ≤ 13.6 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 6.8 MHz	6/f_{MCK}			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	18.5 MHz < f_{MCK}	16/f_{MCK}			ns
			14.8 MHz < f_{MCK} ≤ 18.5 MHz	14/f_{MCK}			ns
			11.1 MHz < f_{MCK} ≤ 14.8 MHz	12/f_{MCK}			ns
			7.4 MHz < f_{MCK} ≤ 11.1 MHz	10/f_{MCK}			ns
			3.7 MHz < f_{MCK} ≤ 7.4 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 3.7 MHz	6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		f_{KCY2}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		f_{KCY2}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑)[Note 1]	t_{SIK2}			90			ns
SIp hold time (from $\overline{SCKp}$↑)[Note 2]	t_{KSI2}			1/f_{MCK} + 50			ns
Delay time from $\overline{SCKp}$↓ to SOp output[Note 3]	t_{KSO2}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ				2/f_{MCK} + 120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 230	ns

(Notes, Caution and Remarks are given on the next page.)