Renesas Electronics America Inc - UPD78F1007GB-GAH-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1007gb-gah-ax

1.7 Outline of Functions

1. 7. 1 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L

(1/2)

Item		78K0R/KC3-L											78K0R/KD3-L			78K0R/KE3-L		
		40-pin				44-pin				48-pin								
		μPD78F1000	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1000	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1001	μPD78F1002	μPD78F1003	μPD78F1004	μPD78F1005	μPD78F1006	μPD78F1007	μPD78F1008	μPD78F1009
Internal memory	Flash memory (KB)	16	32	48	64	16	32	48	64	32	48	64	32	48	64	32	48	64
	RAM (KB)	1	1.5	2	3/2 Note 1	1	1.5	2	3/2 Note 1	1.5	2	3/2 Note 1	1.5	2	3/2 Note 1	1.5	2	3/2 Note 1
Memory space		1 MB																
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 2 to 5 MHz: V_{DD} = 1.8 to 5.5 V																
	Internal high-speed oscillation clock	Internal oscillation 1 MHz (TYP.), 8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V																
	20 MHz internal high-speed oscillation clock	Internal oscillation 20 MHz (TYP.): V_{DD} = 2.7 to 5.5 V																
Subsystem clock		–				XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V												
Internal low-speed oscillation clock (dedicated to WDT)		Internal oscillation 30 kHz (TYP.): V_{DD} = 1.8 to 5.5 V																
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)																
Minimum instruction execution time		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)																
		–				61 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)												
Instruction set		• 8-bit operation, 16-bit operation • Multiplication (8 bits × 8 bits) • Bit manipulation (Set, reset, test, and Boolean operation), etc.																
I/O port	Total	33				37				41			45			55		
	CMOS I/O	31				33				34			38			48		
	CMOS input	2				4				4			4			4		
	CMOS output	–				–				1			1			1		
	N-ch open-drain I/O (6 V tolerance)	–				–				2			2			2		
Timer	16-bit timer	8 channels																
	Watchdog timer	1 channel																
	Real-time counter (RTC)	–				1 channel												
	Timer output	6 (PWM outputs: 6 Note 2)				8 (PWM outputs: 7 Note 2)												
	RTC output	–				2 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz) • 512 Hz, 16.384 kHz, or 32.768 kHz (subsystem clock: f_{SUB} = 32.768 kHz)													

Notes 1. This is 2 KB when the self-programming function is used.

2. The number of outputs varies, depending on the setting.

2.1.1 78K0R/KC3-L (40-pin products)

(1) Port functions (1/2): 78K0R/KC3-L (40-pin)

Function Name	I/O	Function	After Reset	Alternate Function
P10	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04
P13				TI05/TO05
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/INTP1
P32				$\overline{\text{SCK10}}$/SCL10/INTP2
P40[Note]	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P50	I/O	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06
P51				TI07/TO07
P70	I/O	Port 7. 6-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

2.2.16 FLMD0

This is a pin for setting flash memory programming mode.

Perform either of the following processing.

(a) In normal operation mode

It is recommended to leave this pin open during normal operation.

The FLMD0 pin must always be kept at the V_{SS} level before reset release but does not have to be pulled down externally because it is internally pulled down by reset. However, pulling it down must be kept selected (i.e., FLMDPUP = "0", default value) by using bit 7 (FLMDPUP) of the background event control register (BECTL) (see **26.5 (1) Back ground event control register**). To pull it down externally, use a resistor of 200 kΩ or smaller.

Self programming and the rewriting of flash memory with the programmer can be prohibited using hardware, by directly connecting this pin to the V_{SS} pin.

(b) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

In the self programming mode, the setting is switched to pull up in the self programming library.

(c) In flash memory programming mode

Directly connect this pin to a flash memory programmer when data is written by the flash memory programmer. This supplies a writing voltage of the V_{DD} level to the FLMD0 pin.

The FLMD0 pin does not have to be pulled down externally because it is internally pulled down by reset. To pull it down externally, use a resistor of 1 kΩ to 200 kΩ.

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

3.3.1 78K0R/KF3-L

Table 3-3 shows the types of pin I/O circuits and the recommended connections of unused pins. For I/O Circuit Type, see **Figure 3-1. Pin I/O Circuit List**.

Table 3-3. Connection of Unused Pins (1/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P02/SO10/TxD1	5-AG	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P03/SI10/RxD1/SDA10	5-AN		
P04/$\overline{SCK10}$/SCL10			
P05/TI05/TO05	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P06/TI06/TO06			
P10/$\overline{SCK00}$	5-AN		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P11/SI00/RxD0			Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P12/SO00/TxD0	5-AG		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P13/TxD3			Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P14/RxD3	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P15/RTCDIV/RTCCL	5-AG		
P16/TI01/TO01/INTP5	8-R		
P17/TI02/TO02			
P20/ANI0 to P27/ANI7[Note]	11-G		Input: Independently connect to AV_{REF} or AV_{SS} via a resistor. Output: Leave open.
P30/RTC1HZ/INTP3	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P31/TI03/TO03/INTP4			
P40/TOOL0			<When on-chip debugging is enabled> Pull this pin up (pulling it down is prohibited). <When on-chip debugging is disabled> Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.

Note P20/ANI0 to P27/ANI7 are set in the digital input port mode after release of reset.

4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)

Unlike a general-purpose register, each extended SFR (2nd SFR) has a special function.

Extended SFRs are allocated to the F0000H to F07FFH area. SFRs other than those in the SFR area (FFF00H to FFFFFH) are allocated to this area. An instruction that accesses the extended SFR area, however, is 1 byte longer than an instruction that accesses the SFR area.

Extended SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (!addr16.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (!addr16). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (!addr16). When specifying an address, describe an even address.

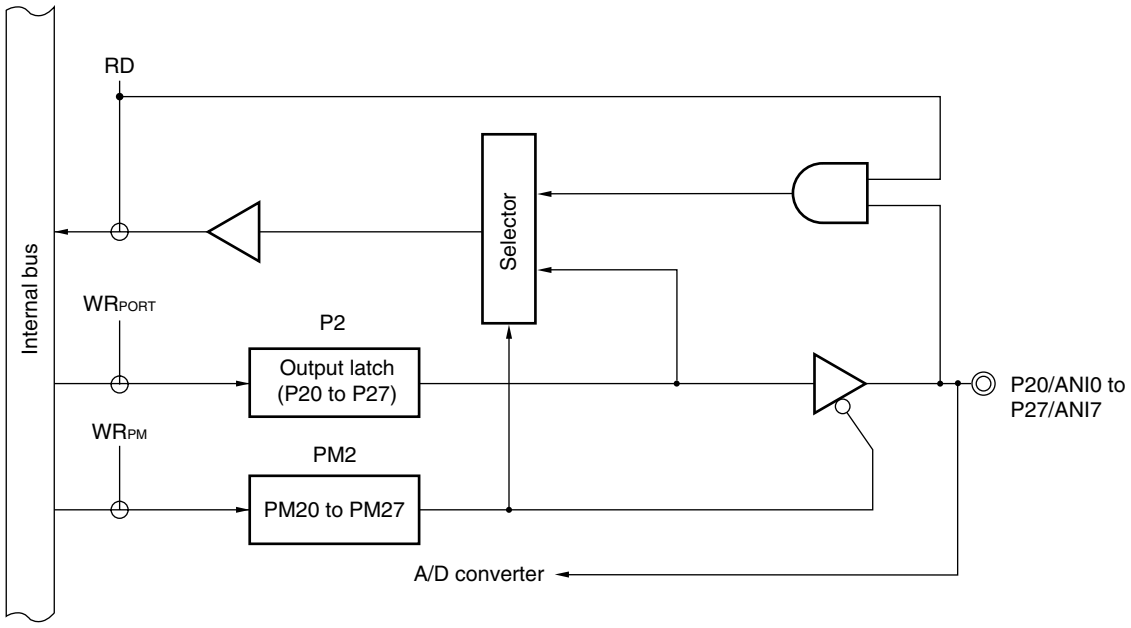
Table 4-6 gives a list of the extended SFRs. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of an extended SFR. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, ID78K0R-QB, and SM+ for 78K0R, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding extended SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For SFRs in the SFR area, see **4.2.4 Special function registers (SFRs)**.

Figure 5-5. Block Diagram of P20 to P27



P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

5.2.9 Port 8

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P80/CMP0P/ INTP3/PGAI	√		√	√	√
P81/CMP0M	√		√	√	√
P82/CMP1P/ INTP7	–	√	√	√	√
P83/CMP1M	√		√	√	√

Remark √: Mounted

Port 8 is an I/O port with an output latch. Port 8 can be set to the input mode or output mode in 1-bit units using port mode register 8 (PM8).

Inputs to the P80 to P83 pins must be enabled or disabled in 1-bit units using port input mode register 8 (PIM8).

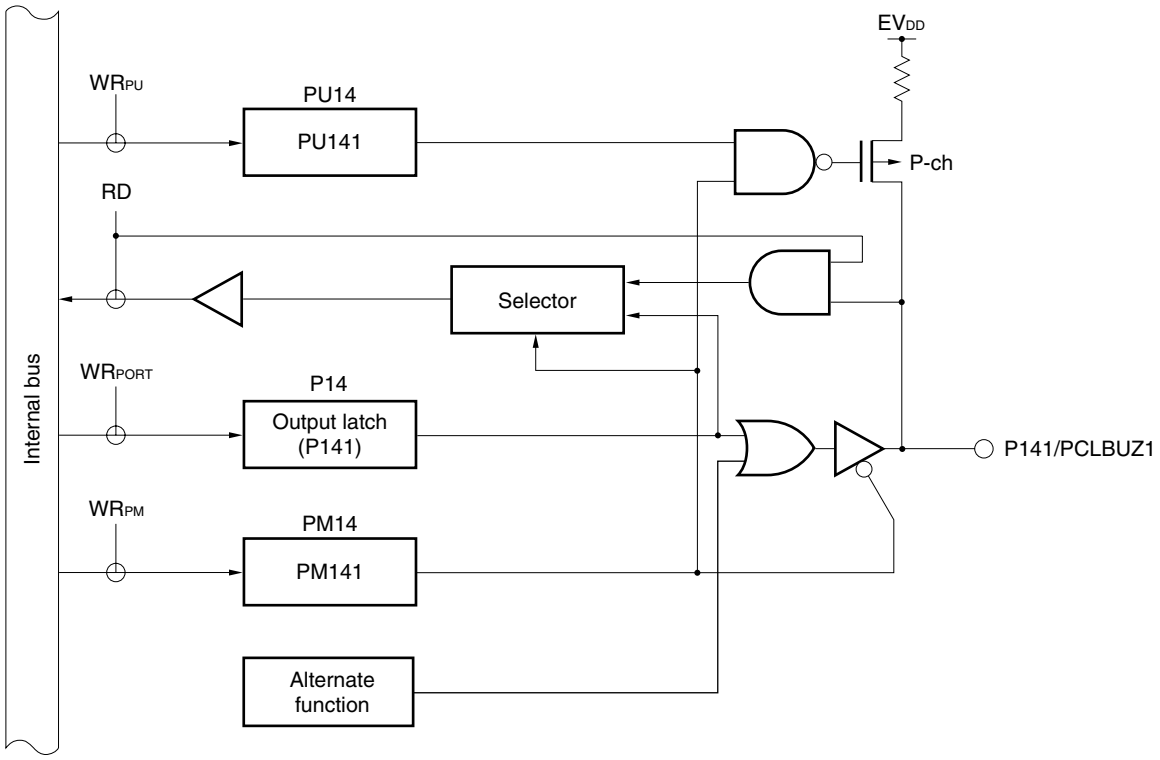
This port can also be used for an input voltage on the (+) sides of comparators 0 and 1, an input voltage on the (–) sides of comparators 0 and 1, an external interrupt request input, and a programmable gain amplifier input.

Reset signal generation sets port 8 to analog input mode.

Figures 5-19 to 5-21 show block diagrams of port 8.

Caution In the case of the 78K0R/KC3-L (40-pin), be sure to clear bit2 of the PM8 register to "0" after the reset release.

Figure 5-26. Block Diagram of P141



P14: Port register 14
PU14: Pull-up resistor option register 14
PM14: Port mode register 14
RD: Read signal
WR××: Write signal

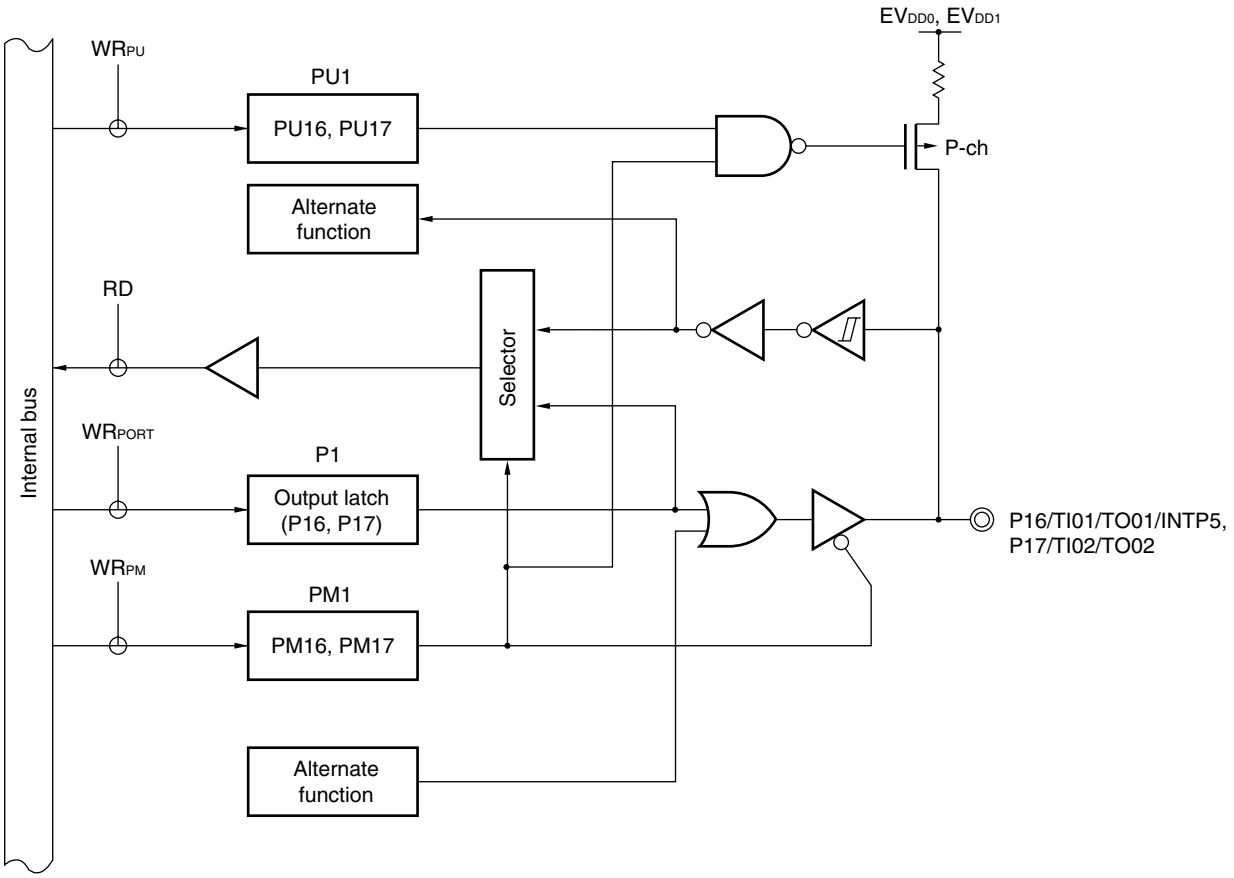
Figure 5-30. Format of Port Mode Register (78K0R/KD3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	1	1	1	1	1	PM01	PM00	FFF20H	FFH	R/W
PM1	1	1	1	1	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	PM32	PM31	PM30	FFF23H	FFH	R/W
PM4	1	1	1	1	1	1	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	1	1	1	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	1	1	1	1	1	1	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM8	1	1	1	1	PM83	PM82	PM81	PM80	FFF28H	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM15	1	1	1	1	1	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 8, 12, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 2 to 7 of the PM0 register, bits 4 to 7 of the PM1 register, bits 3 to 7 of the PM3 register, bits 2 to 7 of the PM4 register, bits 3 to 7 of the PM5 register, bits 2 to 7 of the PM6 register, bits 4 to 7 of the PM8 register, bits 1 to 7 of the PM12 register, and bits 3 to 7 of the PM15 register to 1.

Figure 6-12. Block Diagram of P16 and P17



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Table 8-4. Operations from Count Operation Enabled State to Timer/counter Register mn (TCRmn) Count Start

Timer operation mode	Operation when TSmn = 1 is set
• Interval timer mode	No operation is carried out from start trigger detection (TSmn=1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see **8.3 (6) (a) Start timing in interval timer mode**).
• Event counter mode	Writing 1 to the TSmn bit loads the value of the TDRmn register to the TCRmn register. The subsequent count clock performs count down operation. The external trigger detection selected by the STSmn2 to STSmn0 bits in the TMRmn register does not start count operation (see **8.3 (6) (b) Start timing in event counter mode**).
• Capture mode	No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see **8.3 (6) (c) Start timing in capture mode**).
• One-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation (see **8.3 (6) (d) Start timing in one-count mode**).
• Capture & one-count mode	The waiting-for-start-trigger state is entered by writing 1 to the TSmn bit while the timer is stopped (TEmn = 0). No operation is carried out from start trigger detection until count clock generation. The first count clock loads 0000H to the TCRmn register and the subsequent count clock performs count up operation (see **8.3 (6) (e) Start timing in capture & one-count mode**).

Figure 8-75. Operation Procedure When Multiple PWM Output Function Is Used (2/3)

	Software Operation	Hardware Status
Operation start	(Sets the TOEmp and TOEmq (slave) bits to 1 only when resuming operation.) The TSmn bit (master), and TSmp and TSmq (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. The TSmn, TSmp, and TSmq bits automatically return to 0 because they are trigger bits.	→ TEmn = 1, TEmp, TEmq = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn, TMRmp, TMRmq registers, TOMmn, TOMmp, TOMmq, TOLmn, TOLmp, and TOLmq bits cannot be changed. Set values of the TDRmn, TDRmp, and TDRmq registers can be changed after INTTMmn of the master channel is generated. The TCRmn, TCRmp, and TCRmq registers can always be read. The TSRmn, TSRmp, and TSRmq registers are not used. Set values of the TOm and TOEm registers can be changed.	The counter of the master channel loads the TDRmn register value to timer/counter register mn (TCRmn) and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel 1, the values of the TDRmp register are transferred to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmp become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. At the slave channel 2, the values of the TDRmq register are transferred to TCRmq regster, triggered by INTTMmn of the master channel, and the counter starts counting down. The output levels of TOmq become active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmq = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn bit (master), TTmp, and TTmq (slave) bits are set to 1 at the same time. The TTmn, TTmp, and TTmq bits automatically return to 0 because they are trigger bits.	→ TEmn, TEmp, TEmq = 0, and count operation stops. The TCRmn, TCRmp, and TCRmq registers hold count value and stop. The TOmp and TOmq output are not initialized but hold current status.
	The TOEmp and TOEmq bits of slave channels are cleared to 0 and value is set to the TOmp and TOmq bits.	→ The TOmp and TOmq pins output the TOmp and TOmq set levels.
TAU stop	To hold the TOmp and TOmq pin output levels Clears the TOmp and TOmq bits to 0 after the value to be held is set to the port register.	→ The TOmp and TOmq pin output levels are held by port function.
	When holding the TOmp and TOmq pin output levels are not necessary Switches the port mode register to input mode.	→ The TOmp and TOmq pin output levels go into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note]	→ Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp and TOmq bits are cleared to 0 and the TOmp and TOmq pins are set to port mode.)

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

(**Remark** is listed on the next page.)

10.2 Configurations of Comparator and Programmable Gain Amplifier

The comparators and programmable gain amplifiers consist of the following hardware.

Table 10-1. Configurations of Comparator and Programmable Gain Amplifier

Item	Configuration
Control registers	Peripheral enable register 1 (PER1) Programmable gain amplifier control register (OAM) Comparator 0 and 1 control registers (C0CTL, C1CTL) Comparator 0 and 1 internal reference voltage setting registers (C0RVM, C1RVM) Port input mode register 8 (PIM8) Port mode register 8 (PM8)

10.3 Registers Controlling Comparators and Programmable Gain Amplifiers

The comparators and programmable gain amplifiers use the following eight registers.

- Peripheral enable register 1 (PER1)
- Programmable gain amplifier control register (OAM)
- Comparator 0 and 1 control registers (C0CTL, C1CTL)
- Comparator 0 and 1 internal reference voltage setting registers (C0RVM, C1RVM)
- Port input mode register 8 (PIM8)
- Port mode register 8 (PM8)

14.1 Functions of Serial Array Unit

Each serial interface supported by the 78K0R/Kx3-L has the following features.

14.1.1 3-wire serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41)

Data is transmitted or received in synchronization with the serial clock ($\overline{SCK}$) output from the master channel.

3-wire serial communication is clocked communication performed by using three communication lines: one for the serial clock ($\overline{SCK}$), one for transmitting serial data (SO), one for receiving serial data (SI).

For details about the settings, see **14.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) Communication.**

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

  During master communication: Max. $f_{CLK}/4$, during slave communication: Max. $f_{MCK}/6$ Note

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

Note Use the clocks within a range satisfying the $\overline{SCK}$ cycle time (t_{KCY}) characteristics (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)** or **CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

14.1.3 Simplified I²C (IIC10, IIC20)

This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA). This simplified I²C is designed for single communication with a device such as EEPROM, flash memory, or A/D converter, and therefore, it functions only as a master.

Make sure by using software, as well as operating the control registers, that the AC specifications of the start and stop conditions are observed.

For details about the settings, see **14.8 Operation of Simplified I²C (IIC10, IIC20)**

[Data transmission/reception]

- Master transmission, master reception (only master function with a single master)
- ACK output function[Note] and ACK detection function
- Data length of 8 bits (When an address is transmitted, the address is specified by the higher 7 bits, and the least significant bit is used for R/W control.)
- Manual generation of start condition and stop condition

[Interrupt function]

- Transfer end interrupt

[Error detection flag]

- Parity error (ACK error)

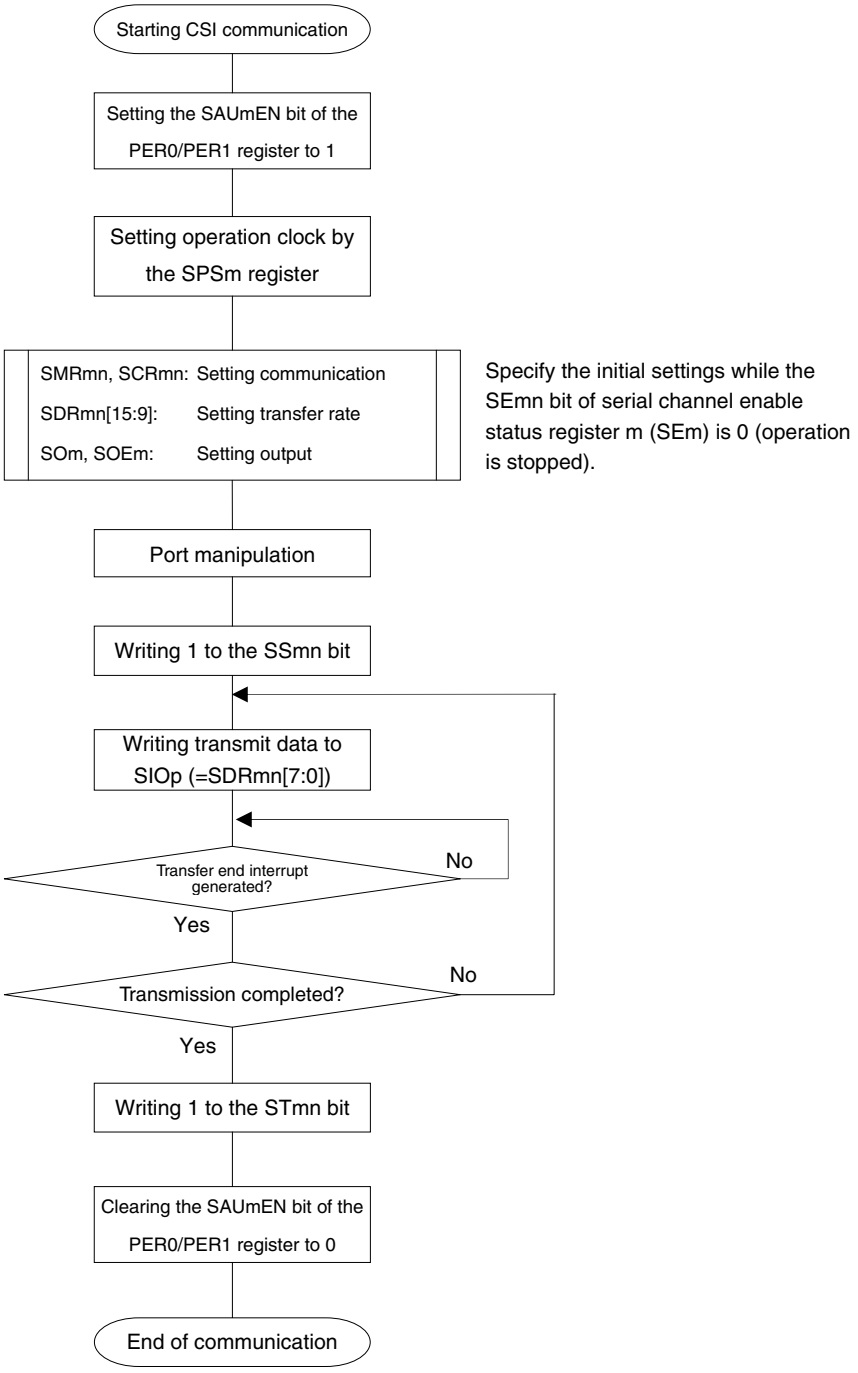
* [Functions not supported by simplified I²C]

- Slave transmission, slave reception
- Arbitration loss detection function
- Wait detection functions

Note When receiving the last data, ACK will not be output if 0 is written to the SOEmn bit (serial output enable register m (SOEm)) and serial communication data output is stopped. See the processing flow in **14.8.3 (2)** for details.

Remark To use an I²C bus of full function, see **CHAPTER 15 SERIAL INTERFACE IICA**.

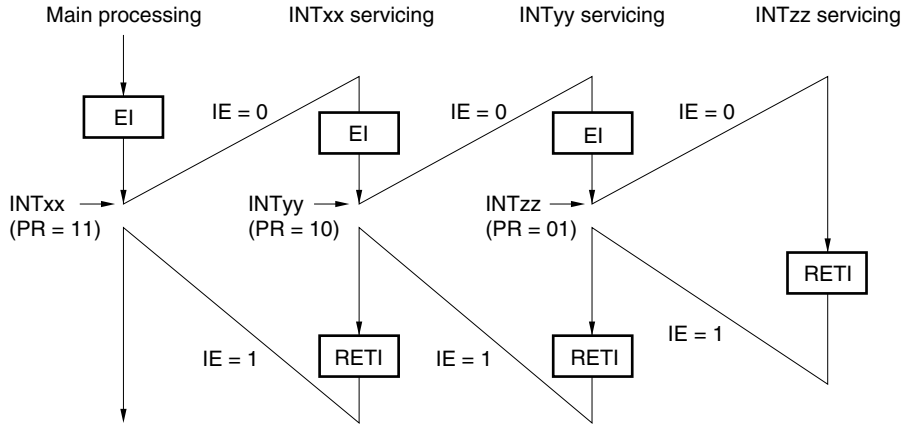
Figure 14-33. Flowchart of Master Transmission (in Single-Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

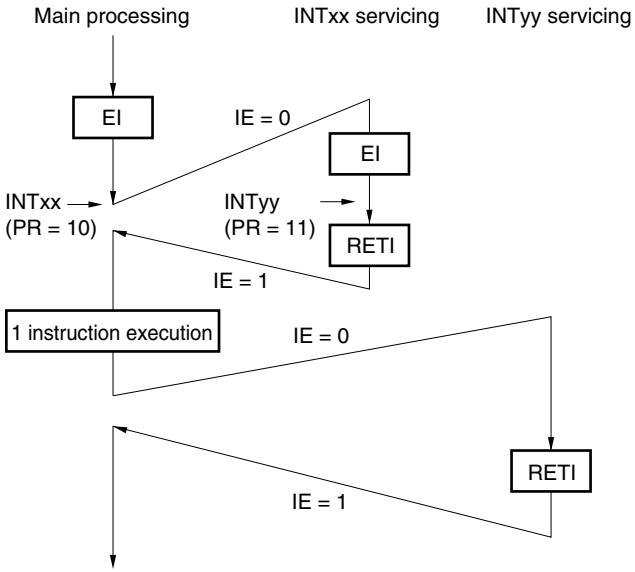
Figure 18-15. Examples of Multiple Interrupt Servicing (1/2)

Example 1. Multiple interrupt servicing occurs twice



During servicing of interrupt INTxx, two interrupt requests, INTyy and INTzz, are acknowledged, and multiple interrupt servicing takes place. Before each interrupt request is acknowledged, the EI instruction must always be issued to enable interrupt request acknowledgment.

Example 2. Multiple interrupt servicing does not occur due to priority control



Interrupt request INTyy issued during servicing of interrupt INTxx is not acknowledged because its priority is lower than that of INTxx, and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

30.6 Peripheral Functions Characteristics

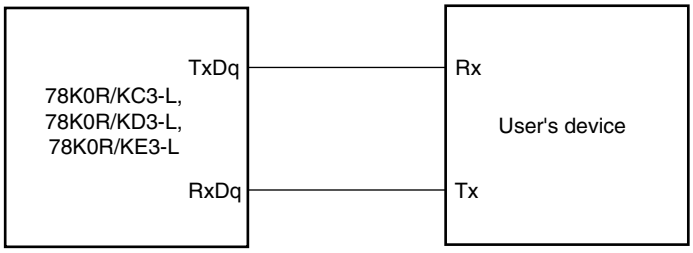
30.6.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

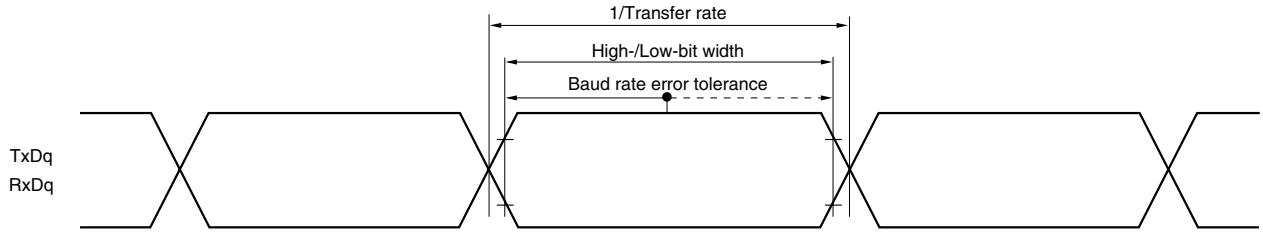
(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		1.8 V ≤ V_{DD} ≤ 5.5 V			f_{MCK}/6	bps
		f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}, 2.7 V ≤ V_{DD} ≤ 5.5 V			3.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0, 1) , g: PIM and POM number (g = 3, 7)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of serial mode register 0n (SMR0n). n: Channel number (n = 0 to 3))

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2, 4), g: PIM and POM number (g = 0, 1, 14)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(6) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, $\overline{SCKp}$... internal clock (1/2)

(T_A = –40 to +85°C, 2.7 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	400 Note 1			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	800 Note 1			ns
$\overline{SCKp}$ high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 75			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 170			ns
$\overline{SCKp}$ low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	t_{KCY1}/2 – 20			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 35			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	150			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	275			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	30			ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	30			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ			120	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			215	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 01, 10, 20, 40, 41), g: PIM and POM number (g = 0, 1, 14)

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

3. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance,
C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V