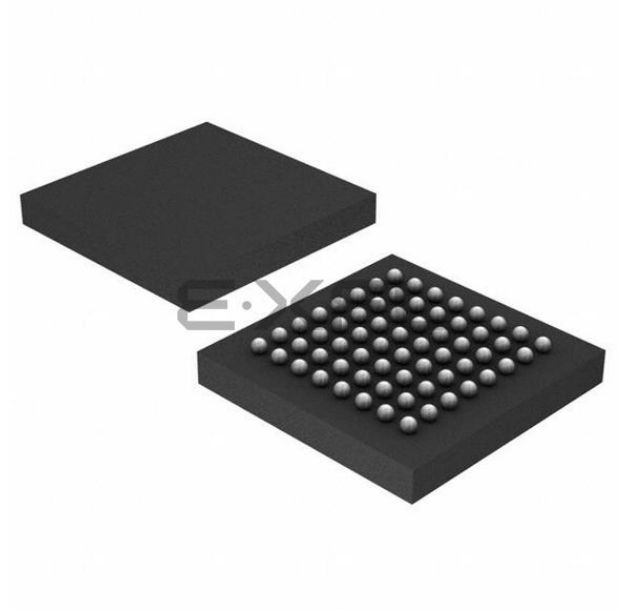

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0R |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | 3-Wire SIO, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 50 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFBGA |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1008f1-an1-a |

**Conventions**

| | | |
|---|---|---|
| Data significance: | Higher digits on the left and lower digits on the right | |
| Active low representations: | $\overline{\times\times\times}$ (overscore over pin and signal name) | |
| **Note**: | Footnote for item marked with **Note** in the text | |
| **Caution**: | Information requiring particular attention | |
| **Remark**: | Supplementary information | |
| Numerical representations: | Binary | ···×××× or ××××B |
| | Decimal | ···×××× |
| | Hexadecimal | ···××××H |

**Related Documents** The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

**Documents Related to Devices**

| Document Name | Document No. |
|---|---|
| 78K0R/Kx3-L User's Manual | This manual |
| 78K0R Microcontroller Instructions User's Manual | U17792E |
| 78K0R Microcontroller Self Programming Library Type02 User's Manual[Note] | U19193E |

**Note** This document is classified under engineering management. Contact an Renesas Electronics sales representative.

**Documents Related to Development Tools (Software) (User's Manuals)**

| Document Name | | Document No. |
|---|---|---|
| CC78K0R Ver. 2.00 C Compiler | Operation | U18549E |
| | Language | U18548E |
| RA78K0R Ver. 1.20 Assembler Package | Operation | U18547E |
| | Language | U18546E |
| SM+ System Simulator | Operation | U18010E |
| PM+ Ver. 6.30 | | U18416E |
| ID78K0R-QB Ver. 3.20 Integrated Debugger | Operation | U17839E |

**Documents Related to Development Tools (Hardware) (User's Manuals)**

| Document Name | Document No. |
|---|---|
| QB-MINI2 On-Chip Debug Emulator with Programming Function | U18371E |
| QB-78K0RIX3 In-Circuit Emulator (compatible with 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L) | U19228E |
| QB-78K0RKX3C In-Circuit Emulator (compatible with 78K0R/KF3-L and 78K0R/KG3-L ($\mu$PD78F1010, 78F1011, 78F1012, 78F1013, and 78F1014)) | U19324E |
| QB-78F1030 In-Circuit Emulator (compatible with 78K0R/KF3-L and 78K0R/KG3-L ($\mu$PD78F1027, 78F1028, 78F1029, and 78F1030)) | Under development |

**Documents Related to Flash Memory Programming**

| Document Name | Document No. |
|---|---|
| PG-FP5 Flash Memory Programmer User's Manual | R02UT0008E |

**Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.**

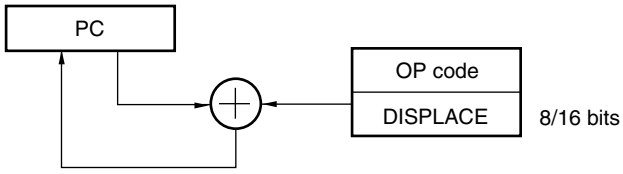
## 4.3 Instruction Address Addressing

### 4.3.1 Relative addressing

**[Function]**

Relative addressing stores in the program counter (PC) the result of adding a displacement value included in the instruction word (signed complement data: −128 to +127 or −32768 to +32767) to the program counter (PC)'s value (the start address of the next instruction), and specifies the program address to be used as the branch destination. Relative addressing is applied only to branch instructions.

**Figure 4-26. Outline of Relative Addressing**




### 4.3.2 Immediate addressing

**[Function]**

Immediate addressing stores immediate data of the instruction word in the program counter, and specifies the program address to be used as the branch destination.

For immediate addressing, CALL !!addr20 or BR !!addr20 is used to specify 20-bit addresses and CALL !addr16 or BR !addr16 is used to specify 16-bit addresses. 0000 is set to the higher 4 bits when specifying 16-bit addresses.

**Figure 4-27. Example of CALL !!addr20/BR !!addr20**

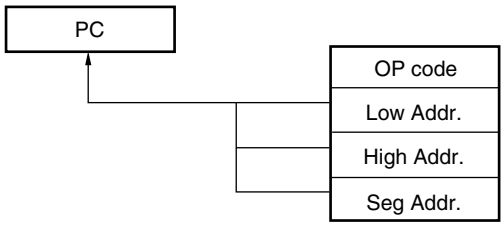



**Figure 4-28. Example of CALL !addr16/BR !addr16**

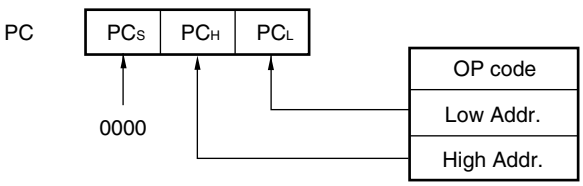
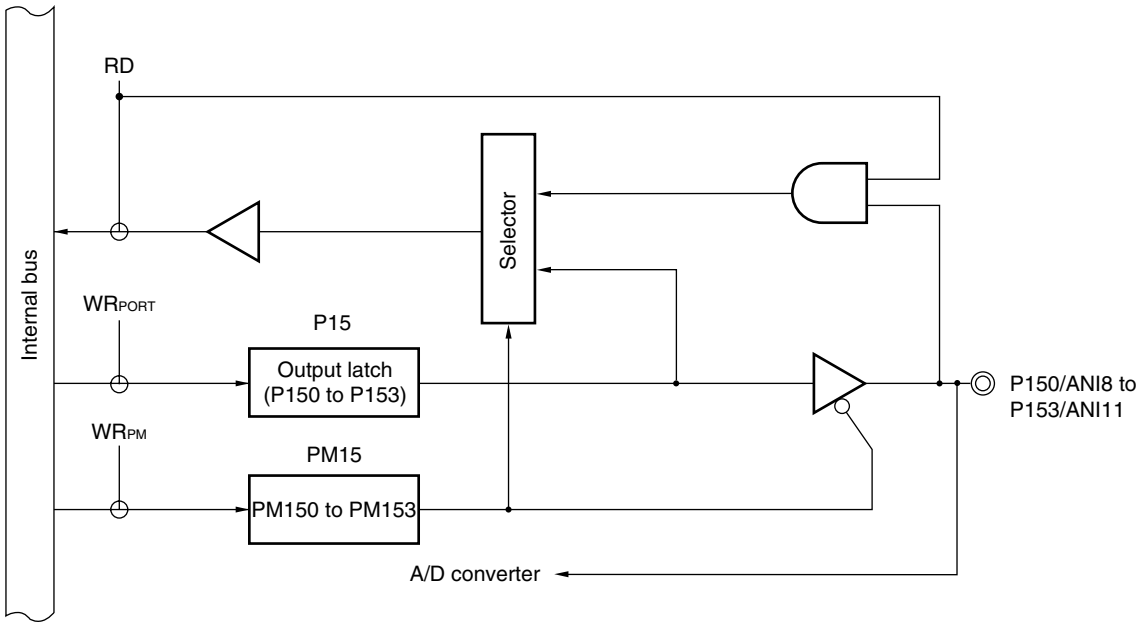
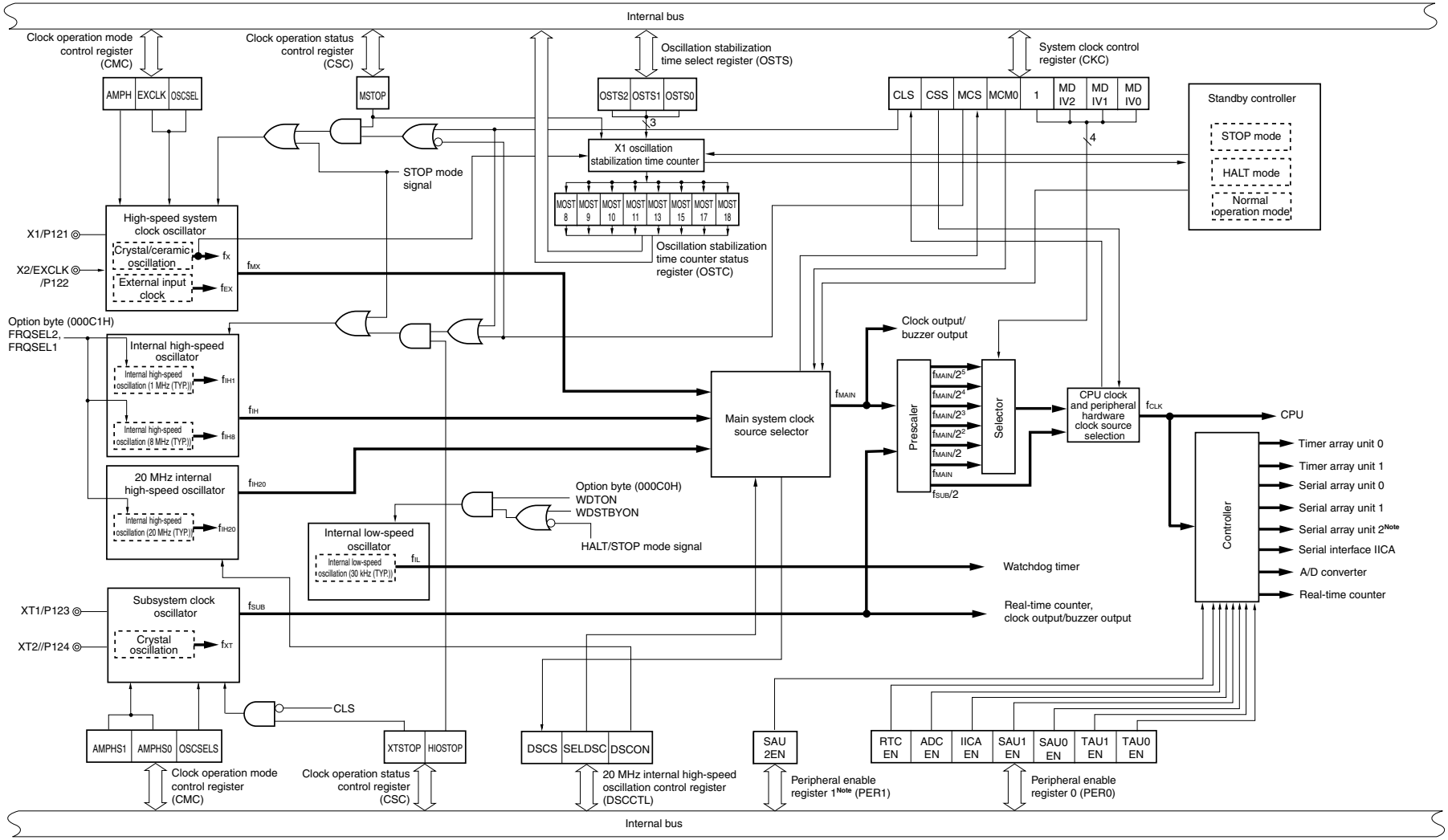


**Figure 5-27. Block Diagram of P150 to P153**




P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

**Figure 7-3. Block Diagram of Clock Generator (78K0R/KF3-L, 78K0R/KG3-L)**




**Note** Those are are only mounted in the μPD78F1027, 78F1028, 78F1029, and 78F1030.

(**Remark** is listed on the next page.)

**Figure 7-8. Format of Oscillation Stabilization Time Select Register (OSTS)**

Address: FFFA3H After reset: 07H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| OSTS | 0 | 0 | 0 | 0 | 0 | OSTS2 | OSTS1 | OSTS0 |

| OSTS2 | OSTS1 | OSTS0 | Oscillation stabilization time selection | | |
|---|---|---|---|---|---|
| | | | | $f_X$ = 10 MHz | $f_X$ = 20 MHz |
| 0 | 0 | 0 | $2^8/f_X$ | 25.6 $\mu$s | Setting prohibited |
| 0 | 0 | 1 | $2^9/f_X$ | 51.2 $\mu$s | 25.6 $\mu$s |
| 0 | 1 | 0 | $2^{10}/f_X$ | 102.4 $\mu$s | 51.2 $\mu$s |
| 0 | 1 | 1 | $2^{11}/f_X$ | 204.8 $\mu$s | 102.4 $\mu$s |
| 1 | 0 | 0 | $2^{13}/f_X$ | 819.2 $\mu$s | 409.6 $\mu$s |
| 1 | 0 | 1 | $2^{15}/f_X$ | 3.27 ms | 1.64 ms |
| 1 | 1 | 0 | $2^{17}/f_X$ | 13.11 ms | 6.55 ms |
| 1 | 1 | 1 | $2^{18}/f_X$ | 26.21 ms | 13.11 ms |

**Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set the OSTS register before executing the STOP instruction.**

**2. Setting the oscillation stabilization time to 20 $\mu$s or less is prohibited.**

**3. Change the setting of the OSTS register before setting the MSTOP bit of the clock operation status control register (CSC) to 0.**

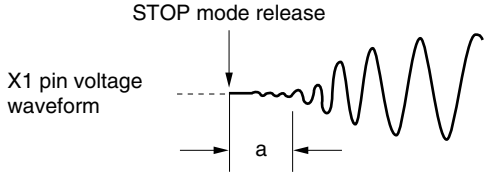
**4. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.**

**5. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the OSTS register.**

**In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.**

- **If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating. (Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)**

**6. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).**




**Remark** $f_X$: X1 clock oscillation frequency

**Table 7-4. CPU Clock Transition and SFR Register Setting Examples (4/6)**

**(9) CPU clock changing from high-speed system clock (C) to subsystem clock (D) (products other than 78K0R/KC3-L (40-pin))**

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CSC Register | Waiting for Oscillation Stabilization | CKC Register |
|---|---|---|---|
| | XTSTOP | | CSS |
| (C) → (D) | 0 | Necessary | 1 |

Unnecessary if the CPU is operating with the subsystem clock

**(10) CPU clock changing from subsystem clock (D) to internal high-speed oscillation clock (B) (products other than 78K0R/KC3-L (40-pin))**

(Setting sequence of SFR registers) →

| Setting Flag of SFR Register / Status Transition | CSC Register | CKC Register | |
|---|---|---|---|
| | HIOSTOP | MCM0 | CSS |
| (D) → (B) | 0 | 0 | 0 |

Unnecessary if the CPU is operating with the internal high-speed oscillation clock

Unnecessary if this register is already set

**Remark** (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

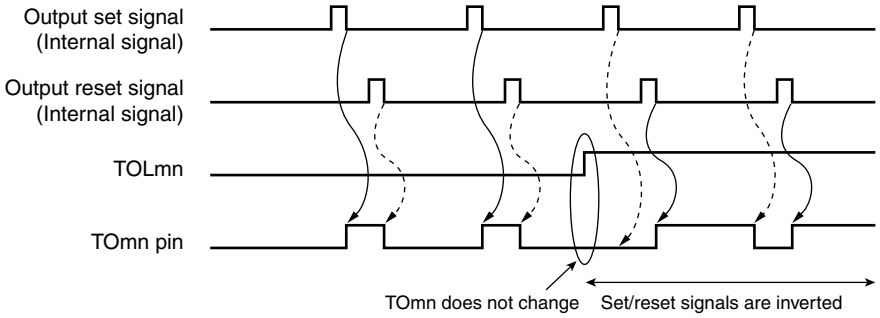
### (3) Operation of TOmn pin in slave channel output mode (TOMmn = 1)

#### (a) When timer output level register m (TOLm) setting has been changed during timer operation

When the TOLm register setting has been changed during timer operation, the setting becomes valid at the generation timing of the TOmn pin change condition. Rewriting the TOLm register does not change the output level of the TOmn pin.

The operation when TOMmn is set to 1 and the value of the TOLm register is changed while the timer is operating (TEmn = 1) is shown below.

**Figure 8-34. Operation when TOLm Register Has Been Changed during Timer Operation**




**Remarks 1.** Set: The output signal of the TOmn pin changes from inactive level to active level.
Reset: The output signal of the TOmn pin changes from active level to inactive level.

**2.** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

# CHAPTER 11 CLOCK OUTPUT/BUZZER OUTPUT CONTROLLER

The number of output pins of the clock output and buzzer output controllers differs, depending on the product. Furthermore, 44-pin product of the 78K0R/KC3-L are not provided with clock output and buzzer output controllers.

| Output pin | KC3-L (40-pin) | KC3-L (44-pin) | KC3-L (48-pin) | KD3-L | KE3-L | KF3-L | KG3-L |
|---|---|---|---|---|---|---|---|
| PCLBUZ0 | – | – | √ | √ | √ | √ | √ |
| PCLBUZ1 | – | – | – | – | √ | √ | √ |

## 11.1 Functions of Clock Output/Buzzer Output Controller

The clock output controller is intended for carrier output during remote controlled transmission and clock output for supply to peripheral ICs.

Buzzer output is a function to output a square wave of buzzer frequency.

One pin can be used to output a clock or buzzer sound.

Two output pins, PCLBUZ0 and PCLBUZ1, are available.

The PCLBUZn pin outputs a clock selected by clock output select register n (CKSn).

Figure 11-1 shows the block diagram of clock output/buzzer output controller.

**Remark** n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

**(18) Port mode registers 0, 1, 3, 4, 5, 7, and 14 (PM0, PM1, PM3, PM4, PM5, PM7, PM14)**

These registers set input/output of ports 0, 1, 3, 4, 5, 7, and 14 in 1-bit units.

The port pins that are shared with the serial data I/O pin or serial clock output I/O pin differ depending on the product. When using the serial array unit, set the following port mode registers according to the product used.

| | |
|---|---|
| 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L | : PM3, PM7 |
| 78K0R/KF3-L ($\mu$PD78F1010, 78F1011, 78F1012) | : PM0, PM1, PM4, PM14 |
| 78K0R/KF3-L ($\mu$PD78F1027, 78F1028) | : PM0, PM1, PM4, PM5, PM14 |
| 78K0R/KG3-L ($\mu$PD78F1013, 78F1014) | : PM0, PM1, PM4, PM14 |
| 78K0R/KF3-L ($\mu$PD78F1029, 78F1030) | : PM0, PM1, PM4, PM5, PM14 |

When using the ports (such as P30/SO10/TxD1, P31/SI10/RxD1/SDA10/INTP1) to be shared with the serial data output pin or serial clock output pin for serial data output or serial clock output, set the port mode register (PMxx) bit corresponding to each port to 0. And set the port register (Pxx) bit corresponding to each port to 1

Example: When using P30/SO10/TxD1 for serial data output or serial clock output
Set the PM30 bit of the port mode register 3 to 0.
Set the P30 bit of the port register 3 to 0.

When using the ports (such as P31/SI10/RxD1/SDA10/INTP1, P32/$\overline{\text{SCK10}}$/SCL10/INTP2) to be shared with the serial data input pin or serial clock input pin for serial data input or serial clock input, set the port mode register (PMxx) bit corresponding to each port to 1. At this time, the port register (Pxx) bit may be 0 or 1.

Example: When using P31/SI10/RxD1/SDA10/INTP1 for serial data input or serial clock input
Set the PM31 bit of port mode register 3 to 1.
Set the P31 bit of port register 3 to 0 or 1.

The PM0, PM1, PM3, PM4, PM5, PM7, and PM14 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets the PM0, PM1, PM3, PM4, PM5, PM7, and PM14 registers to FFH.

### 14.4.1 Stopping the operation by units

The stopping of the operation by units is set by using peripheral enable registers 0 and 1 (PER0, PER1).

The PER0 register and the PER1 register are used to enable or disable supplying the clock to the peripheral hardware. Clock supply to a hardware macro that is not used is stopped in order to reduce the power consumption and noise.

To stop the operation of serial array unit 0, clear bit 2 (SAU0EN) of the PER0 register to 0. In the 78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012) and 78K0R/KG3-L (μPD78F1013, 78F1014), to stop the operation of serial array unit 1, clear bit 3 (SAU1EN) of the PER0 register to 0.

Furthermore, in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030), to stop the operation of serial array unit 2, clear bit 0 (SAU2EN) of the PER1 register to 0.

**Figure 14-26. Peripheral Enable Register 0 (PER0) Setting When Stopping the Operation by Units**

**(a) Peripheral enable register 0 (PER0) … Set only the bit of SAUm to be stopped to 0.**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PER0 | RTCEN Note 1 | | ADCEN | IICAEN Note 2 | SAU1EN Note 3 | SAU0EN | TAU1EN Note 3 | TAU0EN Note 3 |
| | × | 0 | × | × | 0/1 | 0/1 | × | × |

Control of SAUm input clock
0: Stops supply of input clock
1: Supplies input clock

**Notes 1.** That is not provided in 40-pin product of the 78K0R/KC3-L.

**2.** That is not provided in 40-pin and 44-pin products of the 78K0R/KC3-L.

**3.** 78K0R/KF3-L and 78K0R/KG3-L only.

**(b) Peripheral enable register 1 (PER1) … Set only the bit of SAU2 to be stopped to 0.**

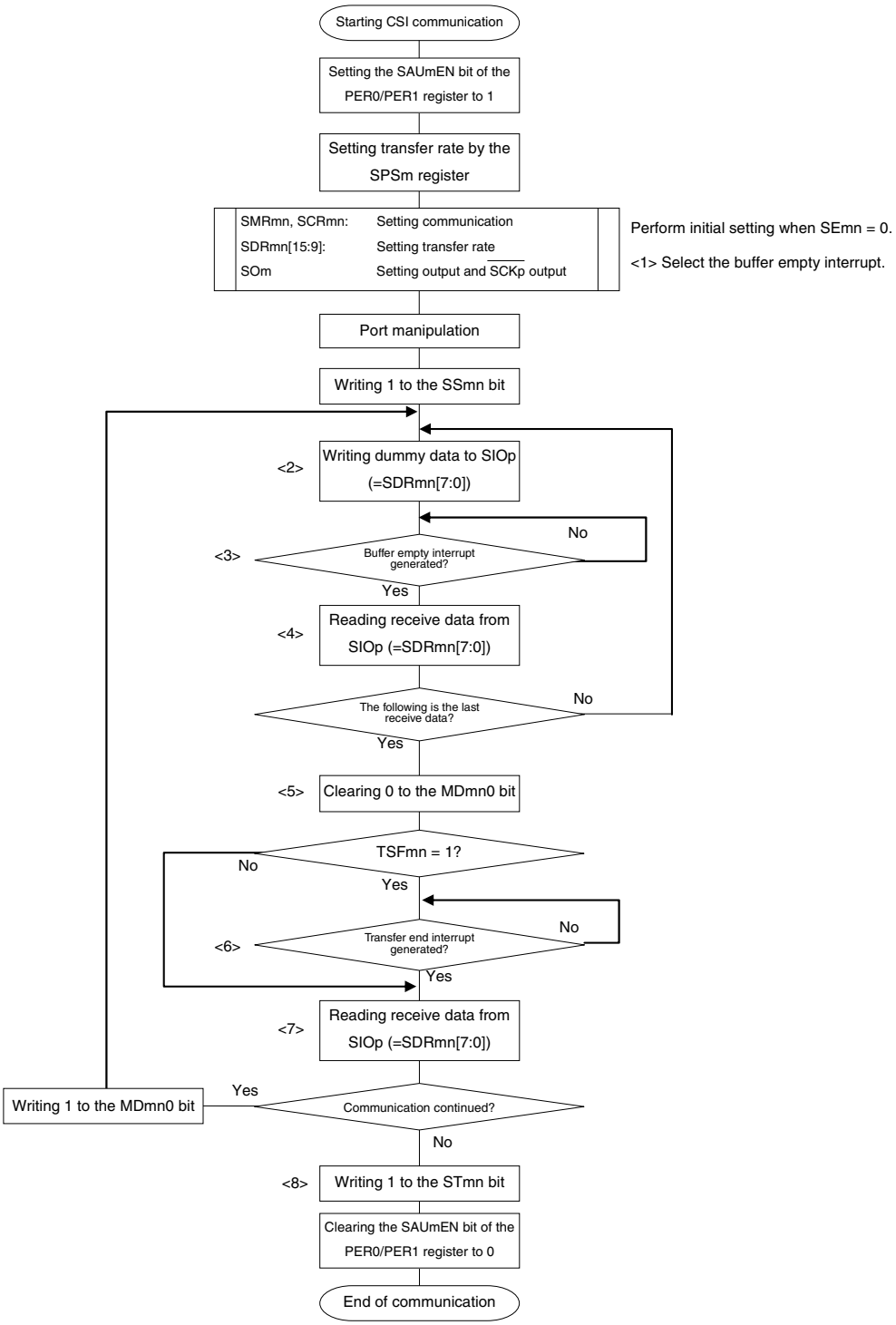
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| PER1 | | | | | | | | SAU2EN |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1 |

Control of SAU2 input clock
0: Stops supply of input clock
1: Supplies input clock

**Cautions 1. If SAUmEN = 0, writing to a control register of serial array unit m is ignored, and, even if the register is read, only the default value is read**
**Note that this does not apply to the following registers.**
**78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:**
**ISC, NFEN0, PIM3, PIM7, POM3, POM7, PM3, PM7, P3, and P7 registers.**
**78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012), 78K0R/KG3-L (μPD78F1013, 78F1014):**
**ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM14, P0, P1, P4, and P14 registers.**
**78K0R/KF3-L (μPD78F1027, 78F1028), 78K0R/KG3-L (μPD78F1029, 78F1030):**
**ISC, NFEN0, PIM0, PIM1, PIM14, POM0, POM1, POM14, PM0, PM1, PM4, PM5, PM14, P0, P1, P4, P5, and P14 registers.**

(**Caution 2** and **Remark** is listed on the next page.)

**Figure 14-43. Flowchart of Master Reception (in Continuous Reception Mode)**




**Caution After setting the PER0/PER1 register to 1, be sure to set the SPSm register after 4 or more clocks have elapsed.**

**Remark** <1> to <8> in the figure correspond to <1> to <8> in **Figure 14-42 Timing Chart of Master Reception (in Continuous Reception Mode)**.

**Table 14-11. Relationship between register settings and pins**
**(Channel 2 of unit 0: CSI10, UART1 transmission, IIC10)**

| SE 02 Note 1 | MD 022 | MD 021 | SOE 02 | SO 02 | CKO 02 | TXE 02 | RXE 02 | PM 04 | P04 | PM03 Note 2 | P03 Note 2 | PM02 | P02 | Operation mode | Pin Function | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | $\overline{\text{SCK10}}$/ SCL10/P04 | SI10/SDA10/ RxD1/P03 Note 2 | SO10/ TxD1/P02 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | Operation stop mode | P04 | P03 | P02 |
| | 0 | 1 | | | | | | | | | | | | | | P03/RxD1 | |
| | 1 | 0 | | | | | | | | | | | | | | P03 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | × | 1 | × | × Note 3 | × Note 3 | Slave CSI10 reception | $\overline{\text{SCK10}}$ (input) | SI10 | P02 |
| | | | 1 | 0/1 Note 4 | 1 | 1 | 0 | 1 | × | × Note 3 | × Note 3 | 0 | 1 | Slave CSI10 transmission | $\overline{\text{SCK10}}$ (input) | P03 | SO10 |
| | | | 1 | 0/1 Note 4 | 1 | 1 | 1 | 1 | × | 1 | × | 0 | 1 | Slave CSI10 transmission /reception | $\overline{\text{SCK10}}$ (input) | SI10 | SO10 |
| | | | 0 | 1 | 0/1 Note 4 | 0 | 1 | 0 | 1 | 1 | × | × Note 3 | × Note 3 | Master CSI10 reception | $\overline{\text{SCK10}}$ (output) | SI10 | P02 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 0 | 0 | 1 | × Note 3 | × Note 3 | 0 | 1 | Master CSI10 transmission | $\overline{\text{SCK10}}$ (output) | P03 | SO10 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 1 | 0 | 1 | 1 | × | 0 | 1 | Master CSI10 transmission /reception | $\overline{\text{SCK10}}$ (output) | SI10 | SO10 |
| | 0 | 1 | 1 | 0/1 Note 4 | 1 | 1 | 0 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | 0 | 1 | UART1 transmission Note 5 | P04 | P03/RxD1 | TxD1 |
| 0 | 1 | 0 | 0 | 0/1 Note 6 | 0/1 Note 6 | 0 | 0 | 0 | 1 | 0 | 1 | × Note 3 | × Note 3 | IIC10 start condition | SCL10 | SDA10 | P02 |
| | | | | | | 1 | 0 | | | | | | | | | | |
| | | | | | | 0 | 1 | | | | | | | | | | |
| 1 | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 0 | 0 | 1 | 0 | 1 | × Note 3 | × Note 3 | IIC10 address field transmission | SCL10 | SDA10 | P02 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 0 | 0 | 1 | 0 | 1 | × Note 3 | × Note 3 | IIC10 data transmission | SCL10 | SDA10 | P02 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 0 | 1 | 0 | 1 | 0 | 1 | × Note 3 | × Note 3 | IIC10 data reception | SCL10 | SDA10 | P02 |
| 0 | | | 0 | 0/1 Note 7 | 0/1 Note 7 | 0 | 0 | 0 | 1 | 0 | 1 | × Note 3 | × Note 3 | IIC10 stop condition | SCL10 | SDA10 | P02 |
| | | | | | | 1 | 0 | | | | | | | | | | |
| | | | | | | 0 | 1 | | | | | | | | | | |

**Notes 1.** Serial channel enable register 0 (SE0) is a read-only status register which is set using serial channel statrt register 0 (SS0) and serial channel stop register 0 (ST0).

**2.** When channel 3 of unit 0 is set to UART1 reception, this pin becomes an RxD1 function pin (refer to **Table 14-12**). In this case, operation stop mode or UART1 transmission must be selected for channel 2 of unit 0.

**3.** This pin can be set as a port function pin.

**4.** This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

**5.** When using UART1 transmission and reception in a pair, set channel 3 of unit 0 to UART1 reception (refer to **Table 14-12**).

**6.** Set the CKO02 bit to 1 before a start condition is generated. Clear the SO02 bit from 1 to 0 when the start condition is generated.

**7.** Set the CKO02 bit to 1 before a stop condition is generated. Clear the SO02 bit from 0 to 1 when the stop condition is generated.

**Remark** X: Don't care

**Table 14-17. Relationship between register settings and pins (Channel 0 of unit 2: CSI40, UART4 transmission)**

**(μPD78F1027, 78F1028, 78F1029, 78F1030 only)**

| SE 20 Note 1 | MD 202 | MD 201 | SOE 20 | SO 20 | CKO 20 | TXE 20 | RXE 20 | PM 50 | P50 | PM 51 Note 2 | P51 Note 2 | PM 52 | P52 | Operation mode | Pin Function | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | $\overline{\text{SCK40}}$/ INTP1/ P50 | SI40/ RxD4/ INTP2/ P51 Note 2 | SO40/ TxD4/ TO00/P52 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | Operation stop mode | INTP1/ P50 | INTP2/ P51 | TO00/P52 |
| | 0 | 1 | | | | | | | | | | | | | | INTP2/ P51/RxD4 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | × | 1 | × | × Note 3 | × Note 3 | Slave CSI40 reception | $\overline{\text{SCK40}}$ (input) | SI40 | TO00/P52 |
| | | | 1 | 0/1 Note 4 | 1 | 1 | 0 | 1 | × | × Note 3 | × Note 3 | 0 | 1 | Slave CSI40 transmission | $\overline{\text{SCK40}}$ (input) | INTP2/P51 | SO40 |
| | | | 1 | 0/1 Note 4 | 1 | 1 | 1 | 1 | × | 1 | × | 0 | 1 | Slave CSI40 transmission/ reception | $\overline{\text{SCK40}}$ (input) | SI40 | SO40 |
| | | | 0 | 1 | 0/1 Note 4 | 0 | 1 | 0 | 1 | 1 | × | × Note 3 | × Note 3 | Master CSI40 reception | $\overline{\text{SCK40}}$ (output) | SI40 | TO00/P52 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 0 | 0 | 1 | × Note 3 | × Note 3 | 0 | 1 | Master CSI40 transmission | $\overline{\text{SCK40}}$ (output) | INTP2/P51 | SO40 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 1 | 0 | 1 | 1 | × | 0 | 1 | Master CSI40 transmission/ reception | $\overline{\text{SCK40}}$ (output) | SI40 | SO40 |
| | 0 | 1 | 1 | 0/1 Note 4 | 1 | 1 | 0 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | 0 | 1 | UART4 transmission Note 5 | INTP1/ P50 | INTP2/ P51/RxD4 | TxD4 |

**Notes 1.** Serial channel enable register 2 (SE2) is a read-only status register which is set using serial channel start register 2 (SS2) and serial channel stop register 2 (ST2).

**2.** When channel 1 of unit 2 is set to UART4 reception, this pin becomes an RxD4 function pin (refer to **Table 14-18**). In this case, operation stop mode or UART4 transmission must be selected for channel 0 of unit 2.

**3.** This pin can be set as a port function pin.

**4.** This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

**5.** When using UART4 transmission and reception in a pair, set channel 1 of unit 2 to UART4 reception (refer to **Table 14-18**).

**Remark** X: Don't care

**Table 18-1. Interrupt Source List (3/3)**

| Interrupt Type | Default Priority Note 1 | Interrupt Source | | Internal/ External | Vector Table Address | Basic Configuration Type Note 2 | KC3-L (40-pin) | KC3-L (44-pin) | KC3-L (48-pin) | KD3-L | KE3-L | KF3-L | KG3-L |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Name | Trigger | | | | | | | | | | |
| Maskable | 41 | INTTM10 | End of timer channel 10 count or capture | Internal | 0056H | (A) | – | – | – | – | – | √ | √ |
| | 42 | INTTM11 | End of timer channel 11 count or capture | | 0058H | | – | – | – | – | – | √ | √ |
| | 43 | INTTM12 | End of timer channel 12 count or capture | | 005AH | | – | – | – | – | – | √ | √ |
| | 44 | INTSRE2 | UART2 reception communication error occurrence | | 005CH | | – | – | – | – | – | √ | √ |
| | 45 | INTMD | End of A/D conversion | | 005EH | | – | – | – | – | – | √ | √ |
| | 46 | INTST4 /INTCSI40 | UART4 transmission transfer end or buffer empty interrupt/CSI40 transfer end or buffer empty interrupt | | 0060H | | – | – | – | – | – | Note 3 | Note 3 |
| | 47 | INTSR4 /INTCSI41 | UART4 reception transfer end/CSI41 transfer end or buffer empty interrupt | | 0062H | | – | – | – | – | – | Note 3 | Note 3 |
| Software | – | BRK | Execution of BRK instruction | – | 007EH | (D) | √ | √ | √ | √ | √ | √ | √ |
| Reset | – | RESET | $\overline{\text{RESET}}$ pin input | – | 0000H | – | √ | √ | √ | √ | √ | √ | √ |
| | | POC | Power-on-clear | | | | √ | √ | √ | √ | √ | √ | √ |
| | | LVI | Low-voltage detection Note 4 | | | | √ | √ | √ | √ | √ | √ | √ |
| | | WDT | Overflow of watchdog timer | | | | √ | √ | √ | √ | √ | √ | √ |
| | | TRAP | Execution of illegal instruction Note 5 | | | | √ | √ | √ | √ | √ | √ | √ |

**Notes 1.** The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 47 indicate the lowest priority.

**2.** Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 18-1.

**3.** INTST4, INTCSI40, INTSR4, INTCSI41 are only mounted in the 78K0R/KF3-L ($\mu$PD78F1027 and 78F1028) and the 78K0R/KG3-L ($\mu$PD78F1029 and 78F1030).

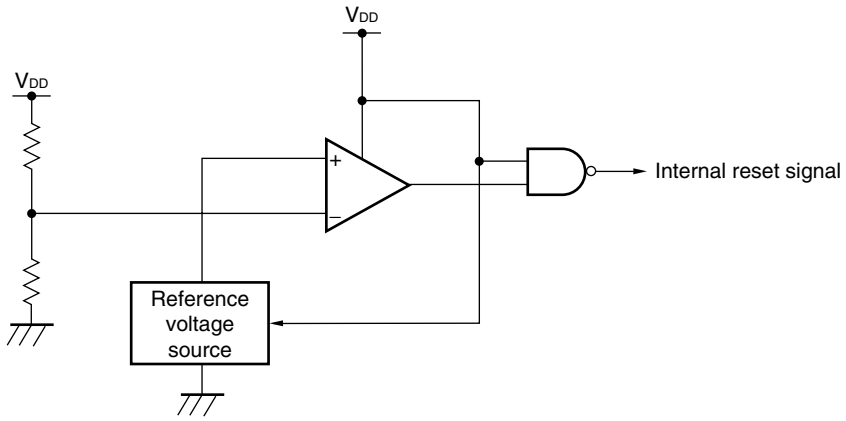
**4.** When bit 1 (LVIMD) of the low-voltage detection register (LVIM) is set to 1.

**5.** When the instruction code in FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

## 22.2 Configuration of Power-on-Clear Circuit

The block diagram of the power-on-clear circuit is shown in Figure 22-1.

**Figure 22-1. Block Diagram of Power-on-Clear Circuit**




## 22.3 Operation of Power-on-Clear Circuit

- An internal reset signal is generated on power application. When the supply voltage ($V_{DD}$) exceeds the detection voltage ($V_{PDR}$ = 1.61 V ±0.09 V), the reset status is released.

  **Caution If the low-voltage detector (LVI) is set to ON by an option byte by default, the reset signal is not released until the supply voltage ($V_{DD}$) exceeds 2.07 V ±0.2 V.**

- The supply voltage ($V_{DD}$) and detection voltage ($V_{PDR}$ = 1.59 V ±0.09 V) are compared. When $V_{DD} < V_{PDR}$, the internal reset signal is generated.

The timing of generation of the internal reset signal by the power-on-clear circuit and low-voltage detector is shown below.

**Table 29-5. Operation List (10/17)**

| Instruction Group | Mnemonic | Operands | Bytes | Clocks | | Operation | Flag | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Note 1 | Note 2 | | Z | AC | CY |
| 8-bit operation | CMP | A, #byte | 2 | 1 | – | A – byte | × | × | × |
| | | saddr, #byte | 3 | 1 | – | (saddr) – byte | × | × | × |
| | | A, r Note 3 | 2 | 1 | – | A – r | × | × | × |
| | | r, A | 2 | 1 | – | r – A | × | × | × |
| | | A, saddr | 2 | 1 | – | A – (saddr) | × | × | × |
| | | A, !addr16 | 3 | 1 | 4 | A – (addr16) | × | × | × |
| | | A, [HL] | 1 | 1 | 4 | A – (HL) | × | × | × |
| | | A, [HL + byte] | 2 | 1 | 4 | A – (HL + byte) | × | × | × |
| | | A, [HL + B] | 2 | 1 | 4 | A – (HL + B) | × | × | × |
| | | A, [HL + C] | 2 | 1 | 4 | A – (HL + C) | × | × | × |
| | | !addr16, #byte | 4 | 1 | 4 | (addr16) – byte | × | × | × |
| | | A, ES:!addr16 | 4 | 2 | 5 | A – (ES:addr16) | × | × | × |
| | | A, ES:[HL] | 2 | 2 | 5 | A – (ES:HL) | × | × | × |
| | | A, ES:[HL + byte] | 3 | 2 | 5 | A – ((ES:HL) + byte) | × | × | × |
| | | A, ES:[HL + B] | 3 | 2 | 5 | A – ((ES:HL) + B) | × | × | × |
| | | A, ES:[HL + C] | 3 | 2 | 5 | A – ((ES:HL) + C) | × | × | × |
| | | ES:!addr16, #byte | 5 | 2 | 5 | (ES:addr16) – byte | × | × | × |
| | CMP0 | A | 1 | 1 | – | A – 00H | × | × | × |
| | | X | 1 | 1 | – | X – 00H | × | × | × |
| | | B | 1 | 1 | – | B – 00H | × | × | × |
| | | C | 1 | 1 | – | C – 00H | × | × | × |
| | | saddr | 2 | 1 | – | (saddr) – 00H | × | × | × |
| | | !addr16 | 3 | 1 | 4 | (addr16) – 00H | × | × | × |
| | | ES:!addr16 | 4 | 2 | 5 | (ES:addr16) – 00H | × | × | × |
| | CMPS | X, [HL + byte] | 3 | 1 | 4 | X – (HL + byte) | × | × | × |
| | | X, ES:[HL + byte] | 4 | 2 | 5 | X – ((ES:HL) + byte) | × | × | × |

**Notes 1.** When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

**2.** When the program memory area is accessed.

**3.** Except r = A

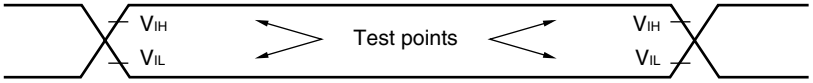
**Remarks 1.** One instruction clock cycle is one cycle of the CPU clock ($f_{CPU}$) selected by the system clock control register (CKC).

**2.** This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

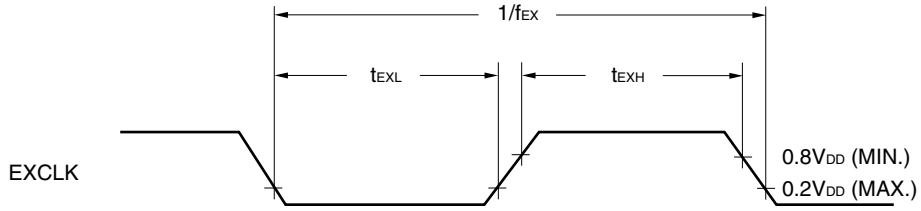
**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

### 30.5.2 Measurement conditions

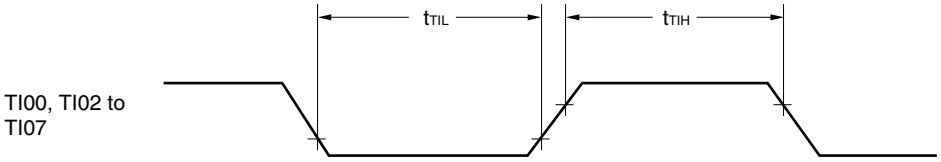
**AC Timing Test Points**



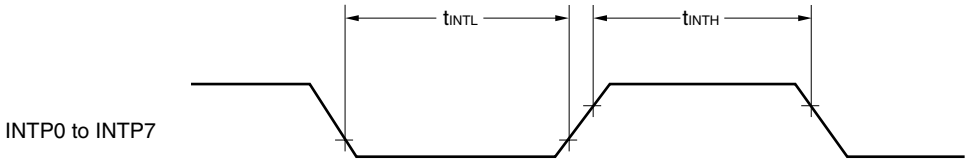

**External Main System Clock Timing**



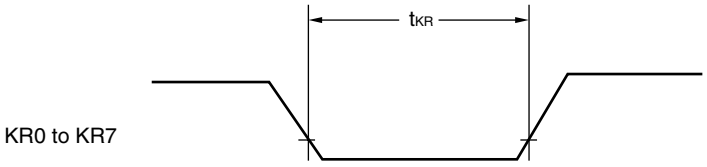

**TI Timing**



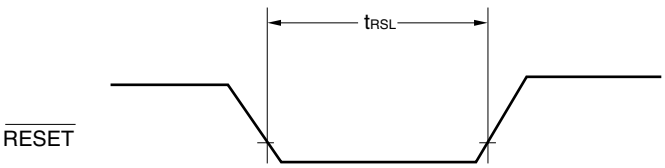

**Interrupt Request Input Timing**




**Key Interrupt Input Timing**

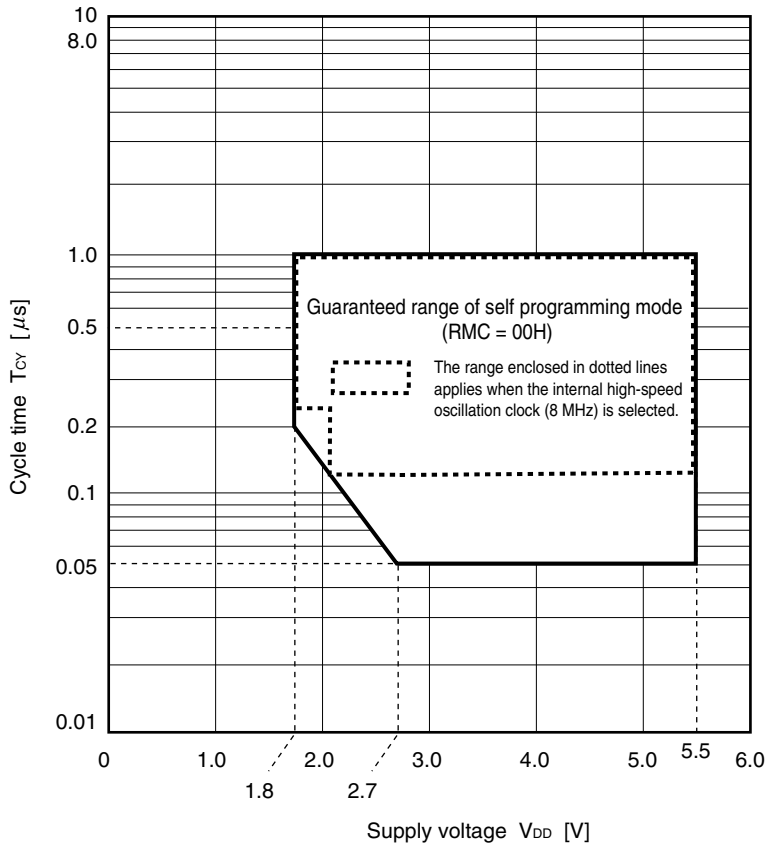



**$\overline{\text{RESET}}$ Input Timing**



**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

**Minimum instruction execution time during self programming mode (RMC = 00H)**




**Remarks 1.** RMC: Regulator mode control register (RMC)

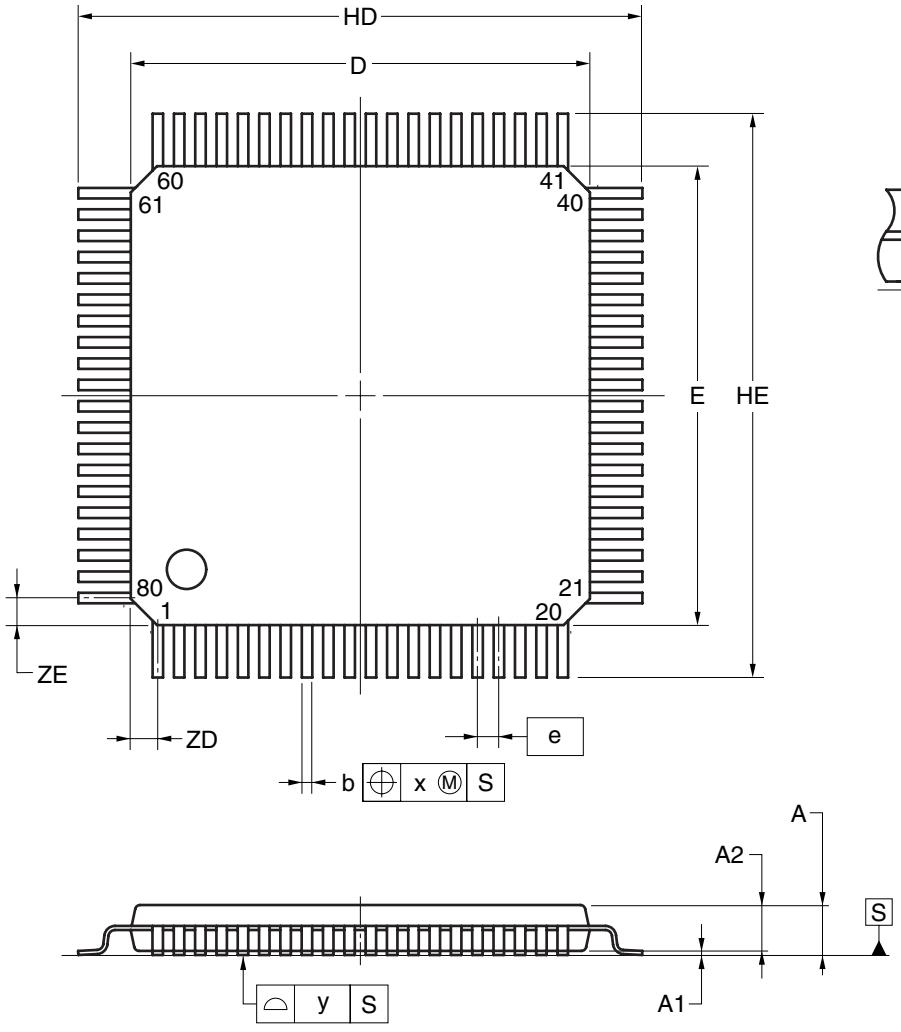
**2.** The self programming function cannot be used when the CPU operates with the subsystem clock.

**3.** The entire voltage range is 1 MHz when RMC is set to 5AH.

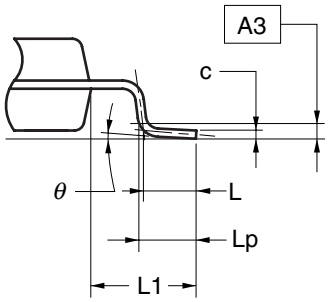
### 32.6 78K0R/KF3-L

$\mu$PD78F1010GC-GAD-AX, 78F1011GC-GAD-AX, 78F1012GC-GAD-AX, 78F1027GC-GAD-AX, 78F1028GC-GAD-AX

## 80-PIN PLASTIC LQFP (14x14)




detail of lead end




(UNIT:mm)

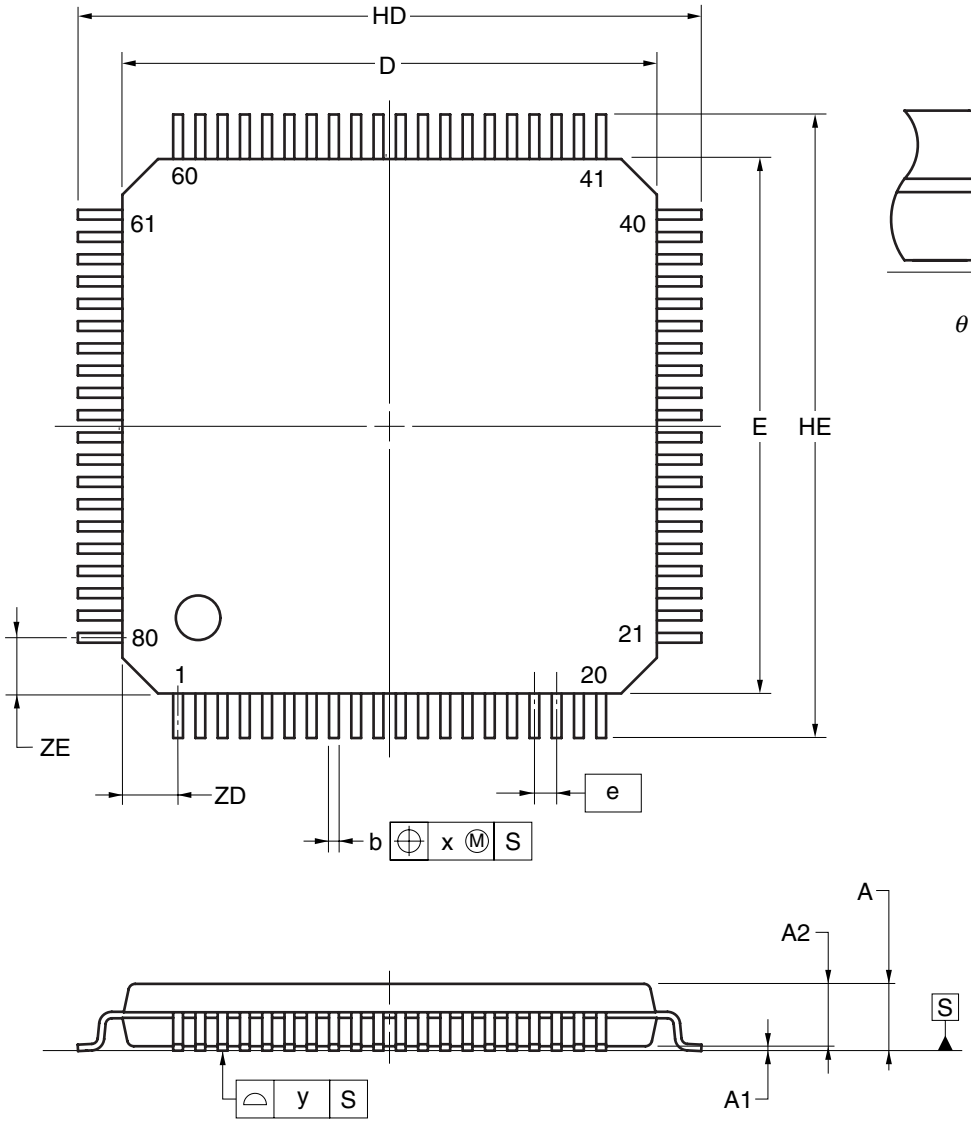
| ITEM | DIMENSIONS |
|---|---|
| D | 14.00±0.20 |
| E | 14.00±0.20 |
| HD | 17.20±0.20 |
| HE | 17.20±0.20 |
| A | 1.70 MAX. |
| A1 | 0.125±0.075 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.30^{+0.08}_{-0.04}$ |
| c | $0.125^{+0.075}_{-0.025}$ |
| L | 0.80 |
| Lp | 0.886±0.15 |
| L1 | 1.60±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 0.825 |
| ZE | 0.825 |

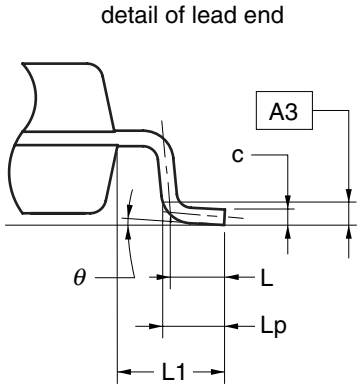
P80GC-65-GAD

**NOTE**
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

μPD78F1010GK-GAK-AX, 78F1011GK-GAK-AX, 78F1012GK-GAK-AX, 78F1027GK-GAK-AX, 78F1028GK-GAK-AX

## 80-PIN PLASTIC LQFP (FINE PITCH) (12x12)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.20^{+0.07}_{-0.03}$ |
| c | $0.125^{+0.075}_{-0.025}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

P80GK-50-GAK

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.