Renesas Electronics America Inc - UPD78F1008GB-GAH-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

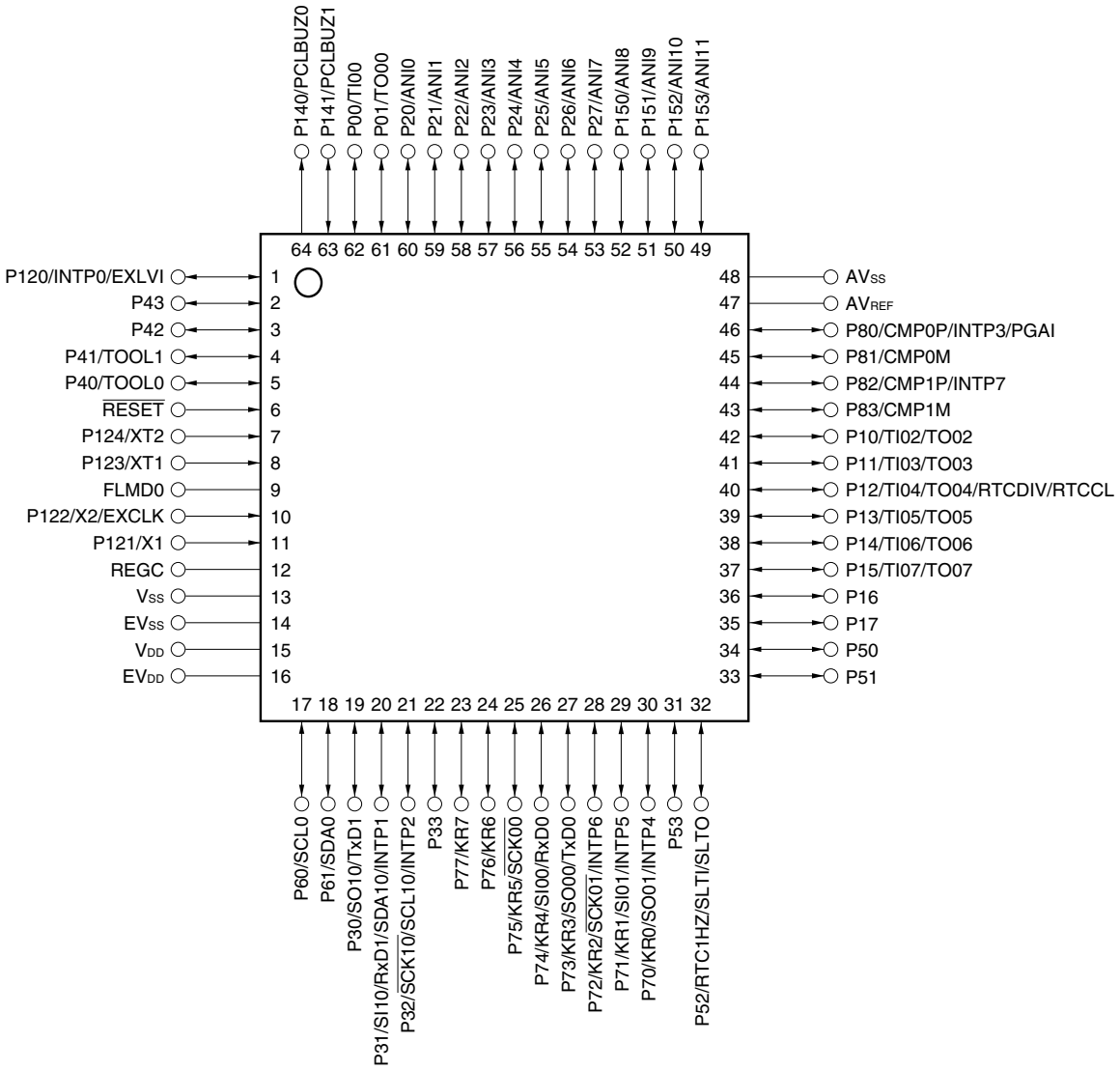
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1008gb-gah-ax

1.4.3 78K0R/KE3-L

- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic TQFP (fine pitch) (7 × 7)



Cautions 1. Make AVSS and EVSS the same potential as VSS.

2. Make EVDD the same potential as VDD.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

4. P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 are set as analog inputs in the order of P153/ANI11, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 as analog inputs, start designing from P153/ANI11 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remarks 1. For pin identification, see **1.5 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separate ground lines.

2.2.2 P10 to P17 (port 1)

P10 to P17 function as an I/O port. These pins also function as timer I/O and real-time counter clock output.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P10/TI02/TO02	√		√	√	√
P11/TO00/TI03/ TO03	√		√	√	√
P12/TI04/TO04/ RTCDIV/RTCCL	P12/TI04/ TO04Note 1	√	√	√	√
P13/TI05/TO05	√		√	√	√
P14/TI06/TO06	–Note 2		–Note 2	–Note 2	√
P15/TI07/TO07	–Note 2		–Note 2	–Note 2	√
P16	–		–	–	√
P17	–		–	–	√

Notes 1. 40-pin product of the 78K0R/KC3-L does not have a RTCDIV/RTCCL pin.

2. TI06/TO06 and TI07/TO07 are shared with P50 and P51, respectively, in products other than the 78K0R/KE3-L.

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P10 to P17 function as an I/O port. P10 to P17 can be set to input or output port in 1-bit units using port mode register 1 (PM1). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 1 (PU1).

(2) Control mode

P10 to P17 function as timer I/O and real-time counter clock output.

(a) TI02 to TI07

These are the pins for inputting an external count clock/capture trigger to 16-bit timers 02 to 07.

(b) TO02 to TO07

These are the timer output pins of 16-bit timers 02 to 07.

(c) RTCDIV

This is the real-time counter clock (32 kHz division) output pin.

(d) RTCCL

This is the real-time counter clock (32 kHz original oscillation) output pin.

3.2.10 P90, P91 (port 9)

P90 and P91 function as an I/O port.

P90 and P91 can be set to input or output port in 1-bit units using port mode register 9 (PM9). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 9 (PU9).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P90	√	–
P91	√	√

3.2.11 P110, P111 (port 11)

P110 and P111 function as an I/O port.

P110 and P111 can be set to input or output port in 1-bit units using port mode register 11 (PM11). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 11 (PU11).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P110	√	√
P111	√	√

3.2.12 P120 to P124 (port 12)

P120 function as a 1-bit I/O port. P121 to P124 functions as a 4-bit input port. These pins also function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P120/INTP0/EXLVI	√	√
P121/X1	√	√
P122/X2/EXCLK	√	√
P123/XT1	√	√
P124/XT2	√	√

The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as a 1-bit I/O port. P120 can be set to input or output port using port mode register 12 (PM12). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 functions as a 4-bit input port.

Table 3-3. Connection of Unused Pins (2/3)

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P41/TOOL1	5-AG	I/O	Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P42/TI04/TO04	8-R		
P43/$\overline{SCK01}$			
P44/SI01			
P45/SO01	5-AG		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open. <When N-ch open-drain> Set the port output latch to 0 and leave open with low level out put.
P46, P47	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P50/$\overline{SCK40}$/INTP1			
P51/SI40/RxD4/INTP2			
P52/SO40/TO00/TxD4	5-AG		
P53/$\overline{SCK41}$/TI00	8-R		
P54/SI41/TI07/TO07			
P55/PCLBUZ1/SO41/INTP7			
P60/SCL0	13-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor, or connect directly to EV_{SS0}. Output: Set the port output latch to 0 and leave open with low level out put.
P61/SDA0			
P62			
P63	13-P		
P64/TI10/TO10	8-R		Input: Independently connect to EV_{DD0} or EV_{SS0} via a resistor. Output: Leave open.
P65/TI11/TO11			
P66/TI12/TO12			
P67/TI13/TO13			
P70/KR0 to P73//KR3			
P74/KR4/INTP8 to P77/KR7/INTP11			
P90, P91	5-AG		
P110	8-R		
P111	5-AG		
P120/INTP0/EXLVI	8-R		

4.4.6 Register indirect addressing

[Function]

Register indirect addressing directly specifies the target addresses using the contents of the register pair specified with the instruction word as an operand address.

[Operand format]

Identifier	Description
–	[DE], [HL] (only the space from F0000H to FFFFFH is specifiable)
–	ES:[DE], ES:[HL] (higher 4-bit addresses are specified by the ES register)

Figure 4-37. Example of [DE], [HL]

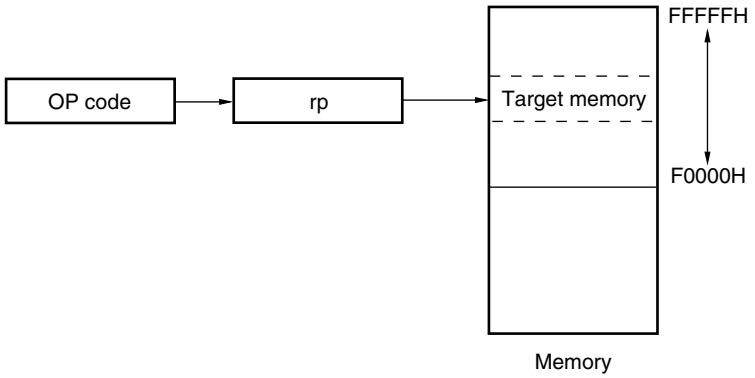


Figure 4-38. Example of ES:[DE], ES:[HL]

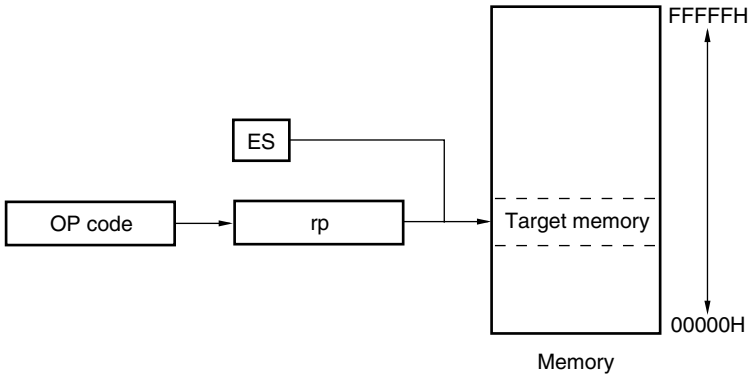
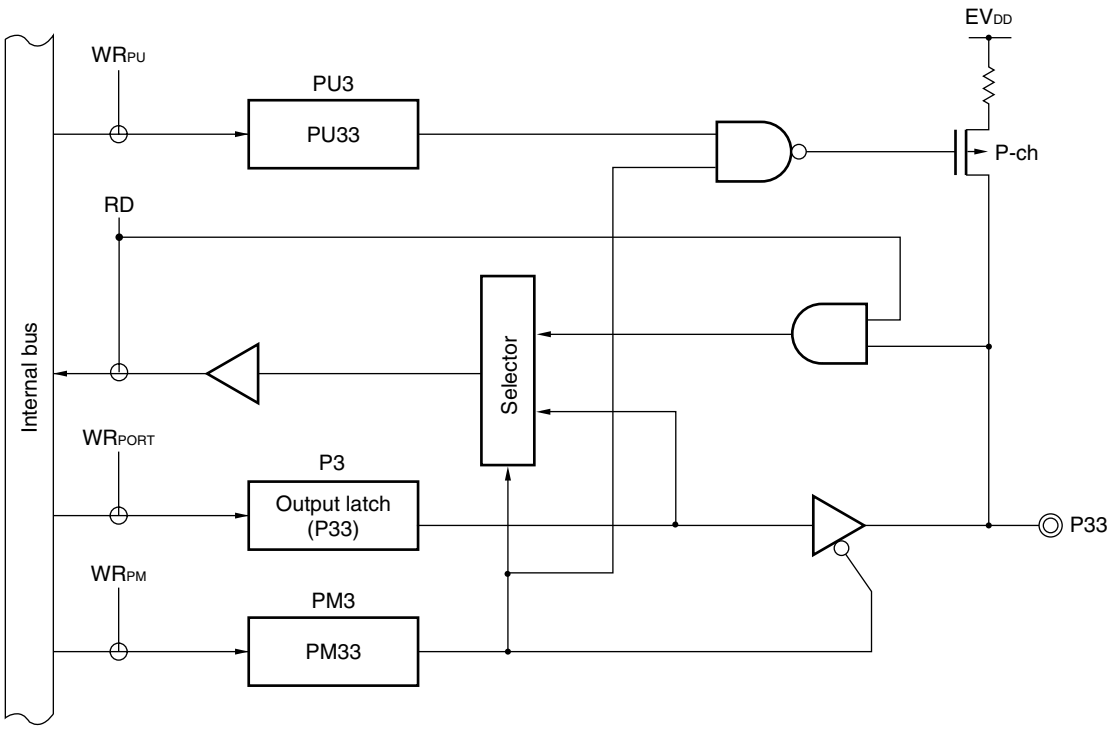
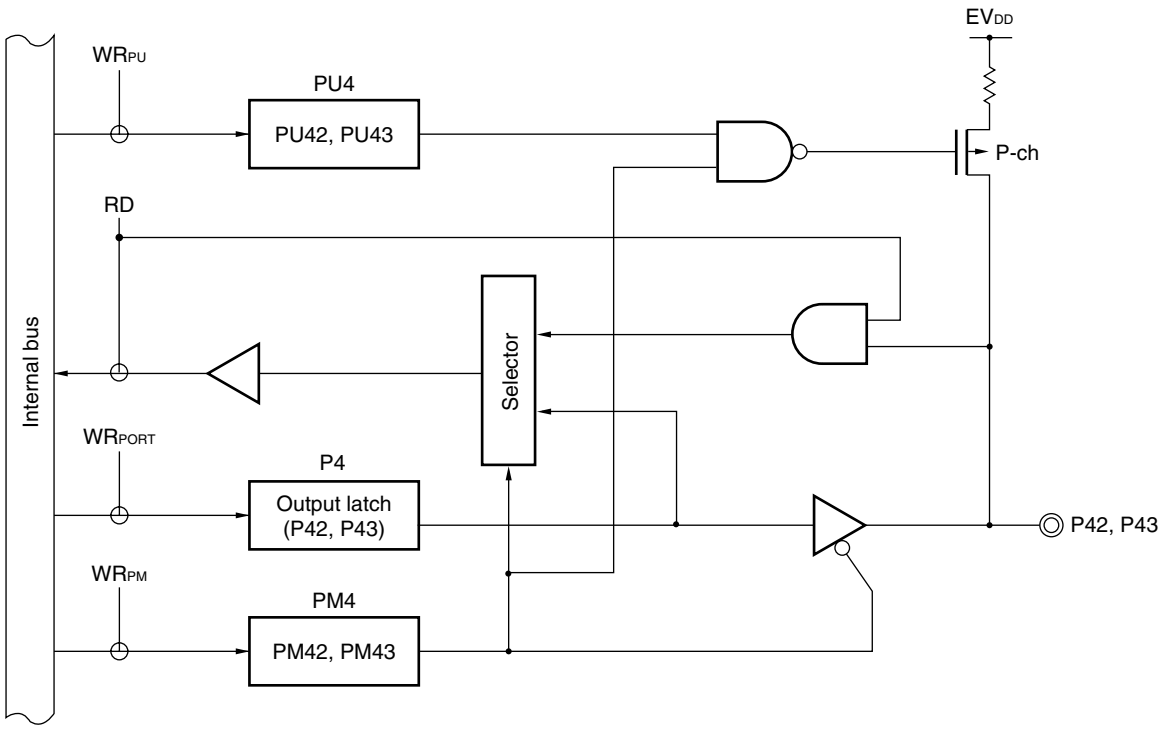


Figure 5-8. Block Diagram of P33



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

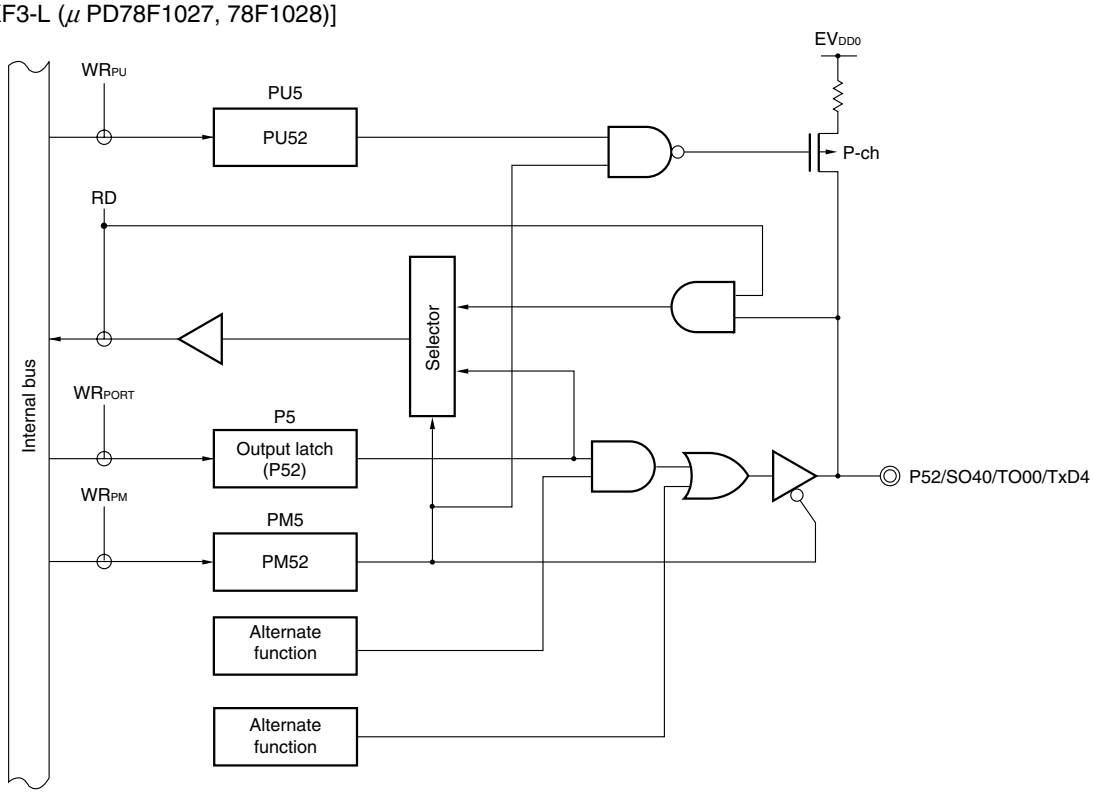
Figure 5-10. Block Diagram of P42 and P43



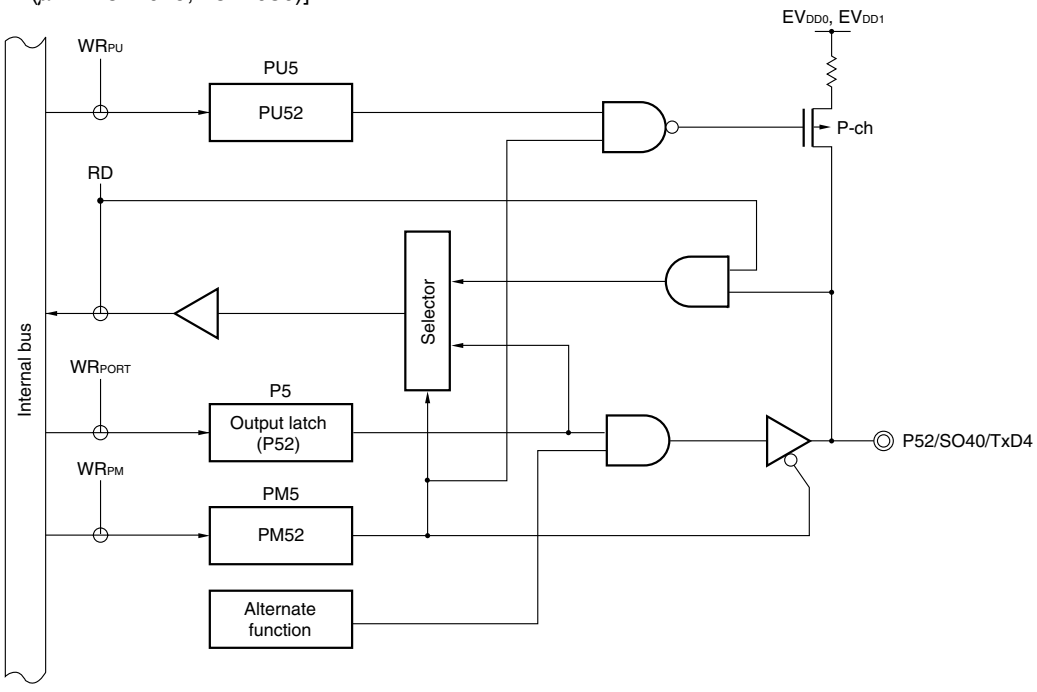
P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-29. Block Diagram of P52

[78K0R/KF3-L (μPD78F1027, 78F1028)]



[78K0R/KG3-L (μPD78F1029, 78F1030)]



P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

7.6.4 Example of setting X1 oscillation clock

After a reset release, the CPU/peripheral hardware clock (f_{CLK}) always starts operating with the internal high-speed oscillation clock. To subsequently change the clock to the X1 oscillation clock, set the oscillator and start oscillation by using the operation speed mode control register (OSMC), clock operation mode control register (CMC), and clock operation status control register (CSC) and wait for oscillation to stabilize by using the oscillation stabilization time counter status register (OSTC). After the oscillation stabilizes, set the X1 oscillation clock to f_{CLK} by using the system clock control register (CKC).

Set the frequency of the internal oscillation clock to be supplied immediately after releasing reset by using the option byte.

[Option byte setting]

Set address 000C1H to FBH.

Option byte (000C1H)

7	6	5	4	3	2	1	0
					FRQSEL2	FRQSEL1	LVIOFF
1	1	1	1	1	0	1	1

LVIOFF bit: Set this bit to 0 to turn on the LVI by default when releasing the power-on-reset.

FRQSEL2 and FRQSEL1 bits: Set the FRQSEL2 and FRQSEL1 bits to 1 and 0, respectively, to set the internal oscillation clock frequency to 1 MHz.

[Register settings] Set the register in the order of <1> to <5> below.

<1> Use the OSMC register to set the frequency of the CPU/peripheral hardware.

OSMC

7	6	5	4	3	2	1	0
RTCLPC[Note]						FLPC	FSEL
0	0	0	0	0	0	0	1

FSEL bit: Set this bit to 0 if the CPU/peripheral hardware clock is 10 MHz or less.

RTCLPC bit[Note]: Set this bit to 1 to operate only the watch in sub-HALT mode (ultra-low current consumption).

Note RTCLPC bit is not provided in the 78K0R/KC3-L (40-pin). In the 78K0R/KC3-L (40-pin), be sure to clear RTCLPC bit to 0.

<2> Set (1) the OSCSEL bit of the CMC register to operate the X1 oscillator.

CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL		OSCSELS[Note]		AMPHS1	AMPHS0	AMPH
0	1	0	0	0	0	0	1

AMPH bit: Set this bit to 0 if the X1 oscillation clock is 10 MHz or less.

OSCSELS bit[Note]: Set this bit to 1 to set P122 and P123 to XT1 oscillation mode.

AMPHS0 and AMPHS1 bits: These bits are used to specify the oscillation mode of the XT1 oscillator.

Note OSCSELS bit is not provided in the 78K0R/KC3-L (40-pin).

<3> Clear (0) the MSTOP bit of the CSC register to start oscillating the X1 oscillator.

CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP[Note]						HIOSTOP
0	1	0	0	0	0	0	0

XTSTOP bit[Note]: Set this bit to 0 to oscillate the XT1 oscillator.

Note XTSTOP bit is not provided in the 78K0R/KC3-L (40-pin).

Table 7-4 shows transition of the CPU clock and examples of setting the SFR registers.

Table 7-4. CPU Clock Transition and SFR Register Setting Examples (1/6)

(1) CPU operating with internal high-speed oscillation clock (B) after reset release (A)

Status Transition	SFR Register Setting
(A) → (B)	SFR registers do not have to be set (default status after reset release).

(2) CPU operating with high-speed system clock (C) after reset release (A)

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note 1			CSC Register	OSMC Register	OSTC Register	CKC Register
	EXCLK	OSCSEL	AMPH	MSTOP	FSEL		MCM0
(A) → (B) → (C) (X1 clock: 2 MHz ≤ fx ≤ 10 MHz)	0	1	0	0	0	Must be checked	1
(A) → (B) → (C) (X1 clock: 10 MHz < fx ≤ 20 MHz)	0	1	1	0	1 Note 2	Must be checked	1
(A) → (B) → (C) (external main clock)	1	1	×	0	0/1 Note 2	Must not be checked	1

Notes 1. The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

2. FSEL = 1 when f_{CLK} > 10 MHz
If a divided clock is selected and f_{CLK} ≤ 10 MHz, use with FSEL = 0 is possible even if fx > 10 MHz.

Caution Set the clock after the supply voltage has reached the operable voltage of the clock to be set (see CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)).

Remark ×: don't care

(3) CPU operating with subsystem clock (D) after reset release (A) (products other than 78K0R/KC3-L (40-pin))

(The CPU operates with the internal high-speed oscillation clock immediately after a reset release (B).)

(Setting sequence of SFR registers) →

Setting Flag of SFR Register / Status Transition	CMC Register Note			CSC Register	Waiting for Oscillation Stabilization	CKC Register
	OSCSELS	AMPHS1	AMPHS0	XTSTOP		CSS
(A) → (B) → (D)	1	0/1	0/1	0	Necessary	1

Note The clock operation mode control register (CMC) can be written only once by an 8-bit memory manipulation instruction after reset release.

Remark (A) to (K) in Table 7-4 correspond to (A) to (K) in Figure 7-19.

Figure 8-29. Format of Port Mode Registers 0, 1, 5 (PM0, PM1, PM5) (78K0R/KE3-L)

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	1	1	1	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

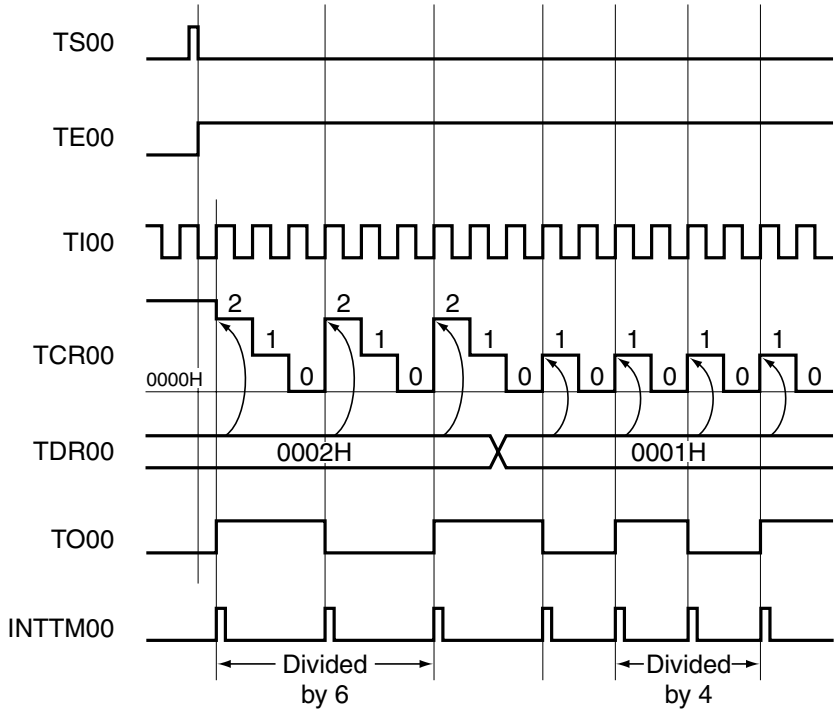
Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	1	1	PM53	PM52	PM51	PM50

PMmn	Pmn pin I/O mode selection (m = 0, 1, 5; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode registers 0, 1, and 5 of the 78K0R/KE3-L product. See below for the format of the port mode register of other products.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: 5.3 (1) Port mode registers (PMxx).
78K0R/KF3-L, 78K0R/KG3-L: 6.3 (1) Port mode registers (PMxx).

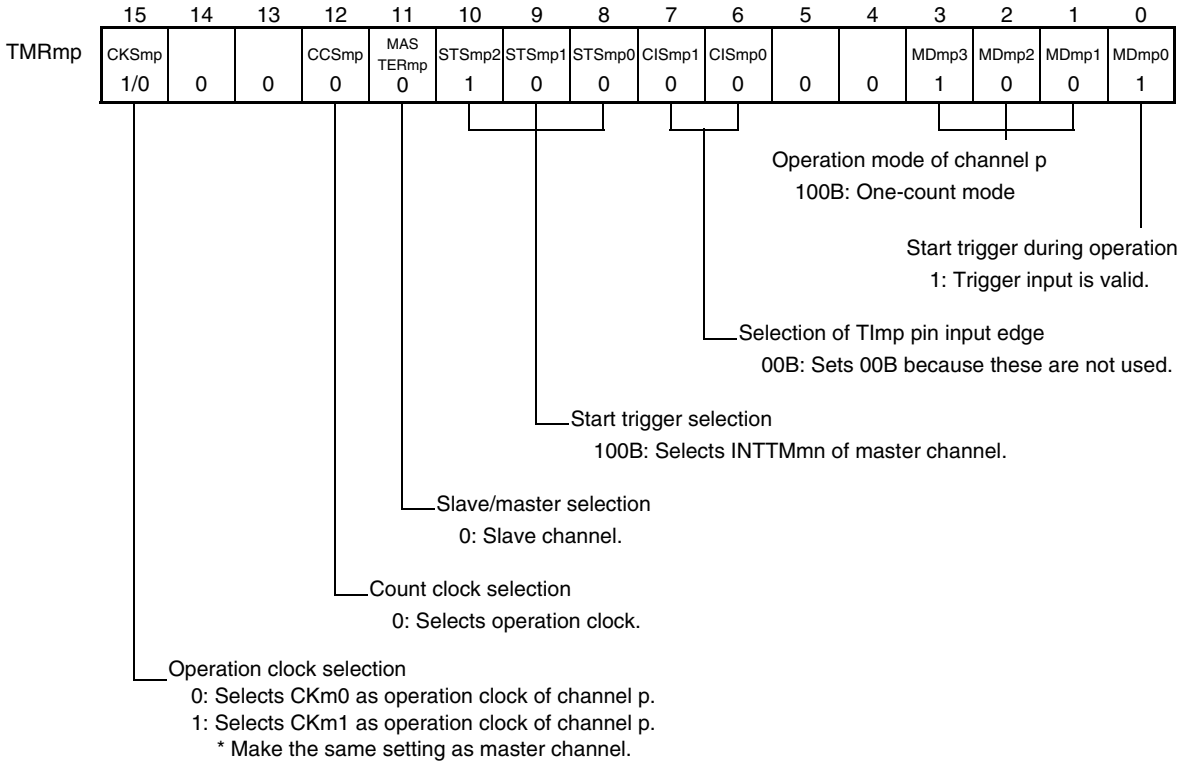
Figure 8-50. Example of Basic Timing of Operation as Frequency Divider (MD000 = 1)



Remark TS00: Bit n of timer channel start register 0 (TS0)
TE00: Bit n of timer channel enable status register 0 (TE0)
TI00: TI00 pin input signal
TCR00: Timer/counter register 00 (TCR00)
TDR00: Timer data register 00 (TDR00)
TO00: TO00 pin output signal

Figure 8-69. Example of Set Contents of Registers When PWM Function (Slave Channel) Is Used

(a) Timer mode register mp (TMRmp)



(b) Timer output register m (TOm)

	Bit p	
TOm	TOmp 1/0	0: Outputs 0 from TOmp. 1: Outputs 1 from TOmp.

(c) Timer output enable register m (TOEm)

	Bit p	
TOEm	TOEmp 1/0	0: Stops the TOmp output operation by counting operation. 1: Enables the TOmp output operation by counting operation.

(d) Timer output level register m (TOLm)

	Bit p	
TOLm	TOLmp 1/0	0: Positive logic output (active-high) 1: Inverted output (active-low)

(e) Timer output mode register m (TOMm)

	Bit p	
TOMm	TOMmp 1	1: Sets the slave channel output mode.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: n < p ≤ 7
When m = 1: n < p ≤ 3

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 8-70. Operation Procedure When PWM Function Is Used (2/2)

	Software Operation	Hardware Status
Operation start	Sets the TOEmp bit (slave) to 1 (only when operation is resumed). The TSmn (master) and TSmp (slave) bits of timer channel start register m (TSm) are set to 1 at the same time. The TSmn and TSmp bits automatically return to 0 because they are trigger bits.	TEmn = 1, TEmp = 1 When the master channel starts counting, INTTMmn is generated. Triggered by this interrupt, the slave channel also starts counting.
During operation	Set values of the TMRmn and TMRmp registers, TOMmn, TOMmp, TOLmn, and TOLmp bits cannot be changed. Set values of the TDRmn and TDRmp registers can be changed after INTTMmn of the master channel is generated. The TCRmn and TCRmp registers can always be read. The TSRmn and TSRmp registers are not used. Set values of the TOm and TOEm registers can be changed.	The counter of the master channel loads the TDRmn register value to timer/counter register mn (TCRmn), and counts down. When the count value reaches TCRmn = 0000H, INTTMmn output is generated. At the same time, the value of the TDRmn register is loaded to the TCRmn register, and the counter starts counting down again. At the slave channel, the value of the TDRmp register is loaded to the TCRmp register, triggered by INTTMmn of the master channel, and the counter starts counting down. The output level of TOmp becomes active one count clock after generation of the INTTMmn output from the master channel. It becomes inactive when TCRmp = 0000H, and the counting operation is stopped. After that, the above operation is repeated.
Operation stop	The TTmn (master) and TTmp (slave) bits are set to 1 at the same time. The TTmn and TTmp bits automatically return to 0 because they are trigger bits.	TEmn, TEmp = 0, and count operation stops. The TCRmn and TCRmp registers hold count value and stop. The TOmp output is not initialized but holds current status.
	The TOEmp bit of slave channel is cleared to 0 and value is set to the TOmp bit.	The TOmp pin outputs the TOmp set level.
TAU stop	To hold the TOmp pin output level Clears the TOmp bit to 0 after the value to be held is set to the port register.	The TOmp pin output level is held by port function.
	When holding the TOmp pin output level is not necessary Switches the port mode register to input mode.	The TOmp pin output level goes into Hi-Z output state.
	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0.[Note]	Power-off status All circuits are initialized and SFR of each channel is also initialized. (The TOmp bit is cleared to 0 and the TOmp pin is set to port mode.)

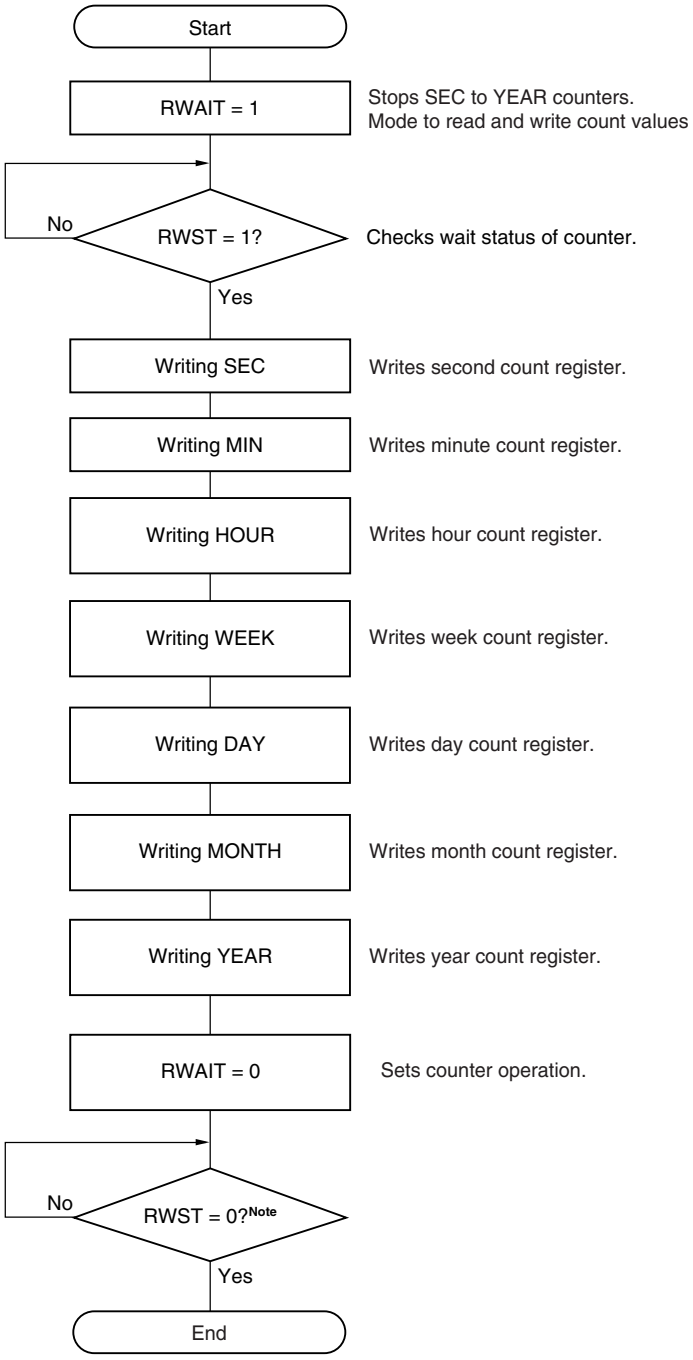
Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00, 02, 04, 06
78K0R/KF3-L, 78K0R/KG3-L: mn = 00, 02, 04, 06, 10, 12
p: Slave channel number[Note]
When m = 0: $n < p \leq 7$
When m = 1: $n < p \leq 3$

Note Since there is no function of timer I/O, the channel 1 in the 78K0R/KC3-L (40-pin) can not be used as the slave channel.

Figure 9-21. Procedure for Writing Real-Time Counter



Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations of setting the RWAIT bit to 1 to clearing the RWAIT bit to 0 within 1 second.

Remark The second count register (SEC), minute count register (MIN), hour count register (HOUR), week count register (WEEK), day count register (DAY), month count register (MONTH), and year count register (YEAR) may be written in any sequence.
All the registers do not have to be set and only some registers may be written.

Table 18-1. Interrupt Source List (2/3)

Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
		Name	Trigger										
Maskable	20	INTTM00	End of timer channel 0 count or capture	Internal	002CH	(A)	√	√	√	√	√	√	√
	21	INTTM01	End of timer channel 1 count or capture		002EH		√	√	√	√	√	√	√
	22	INTTM02	End of timer channel 2 count or capture		0030H		√	√	√	√	√	√	√
	23	INTTM03	End of timer channel 3 count or capture		0032H		√	√	√	√	√	√	√
	24	INTAD	End of A/D conversion		0034H		√	√	√	√	√	√	√
	25	INTRTC	Fixed-cycle signal of real-time counter/alarm match detection		0036H		–	√	√	√	√	√	√
	26	INTRTCI	Interval signal detection of real-time counter		0038H		–	√	√	√	√	√	√
	27	INTKR	Key return signal detection	External	003AH	(C)	√	√	√	√	√	√	√
	28	INTST2 /INTCSI20 /INTIIC20	UART2 transmission transfer end or buffer empty interrupt/CSI20 transfer end or buffer empty interrupt/IIC20 transfer end	Internal	003CH	(A)	–	–	–	–	–	√	√
	29	INTP6	Pin input edge detection	External	003EH	(B)	–	–	–	–	–	√	√
	30	INTTM13	End of timer channel 13 count or capture	Internal	0040H	(A)	–	–	–	–	–	√	√
		INTMD	End of division operation				√	√	√	√	√	–	–
	31	INTTM04	End of timer channel 4 count or capture		0042H		√	√	√	√	√	√	√
	32	INTTM05	End of timer channel 5 count or capture		0044H		√	√	√	√	√	√	√
	33	INTTM06	End of timer channel 6 count or capture		0046H		√	√	√	√	√	√	√
	34	INTTM07	End of timer channel 7 count or capture		0048H		√	√	√	√	√	√	√
	35	INTSR2	UART2 reception transfer end		004AH		–	–	–	–	–	√	√
		INTP6	Pin input edge detection	External		(B)	√	√	√	√	√	–	–
	36	INTP7			004CH		–	√	√	√	√	√	√
	37	INTP8			004EH		–	–	–	–	–	√	√
	38	INTP9			0050H		–	–	–	–	–	√	√
	39	INTP10			0052H		–	–	–	–	–	√	√
	40	INTSRE4 Note 3	UART4 reception communication error occurrence	Internal	0054H	(A)	–	–	–	–	–	Note 3	Note 3
		INTP11	Pin input edge detection	External		(B)	–	–	–	–	–	√	√

Notes 1. The default priority determines the sequence of interrupts if two or more maskable interrupts occur simultaneously. Zero indicates the highest priority and 47 indicate the lowest priority.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 18-1.

3. INTSRE4 is only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

Table 26-1. Wiring Between 78K0R/Kx3-L and Dedicated Flash Memory Programmer

Pin Configuration of Dedicated Flash Memory Programmer			Pin Name	Pin No.									
				KC3-L 40-pin	KC3-L 44-pin	KC3-L 48-pin	KD3-L	KE3-L		KF3-L	KG3-L		
Signal Name	I/O	Pin Function		WQFN (6x6) Note 1	LQFP (10x10)	TQFP (7x7), WQFN (7x7) Note 1	LQFP (10x10)	LQFP (12x12), LQFP (10x10), TQFP (7x7)	FBGA (5x5), FBGA (4x4)	LQFP (12x12), LQFP (14x14)	LQFP (14x20)	LQFP (14x14)	FBGA (6x6) Note 4
SI/RxD Notes 2, 3	Input	Receive signal	TOOL0/ P40	3	2	39	4	5	D6	9	89	12	D8
SO/TxD Note 3	Output	Transmit signal											
SCK	Output	Transfer clock	–	–	–	–	–	–	–	–	–	–	–
CLK	Output	Clock output	–	–	–	–	–	–	–	–	–	–	–
/RESET	Output	Reset signal	$\overline{\text{RESET}}$	4	3	40	5	6	E7	10	90	13	G9
FLMD0	Output	Mode signal	FLMD0	5	6	43	8	9	E8	13	93	16	F9
V_{DD}	I/O	V_{DD} voltage generation/ power monitoring	V_{DD}	10	11	48	13	15	B7	19	99	22	C9
			EV_{DD}	–	–	–	–	16	A8	–	–	–	–
			EV_{DD0}	–	–	–	–	–	–	20	100	23	C10
			EV_{DD1}	–	–	–	–	–	–	–	30	53	C1
			AV_{REF}	29	32	23	38	47	G1	59	50	73	H1
GND	–	Ground	V_{SS}	9	10	47	12	13	C7	17	97	20	F10
			EV_{SS}	–	–	–	–	14	B8	–	–	–	–
			EV_{SS0}	–	–	–	–	–	–	18	98	21	D9
			EV_{SS1}	–	–	–	–	–	–	–	20	43	A3
			AV_{SS}	30	33	24	39	48	H1	60	51	74	H2

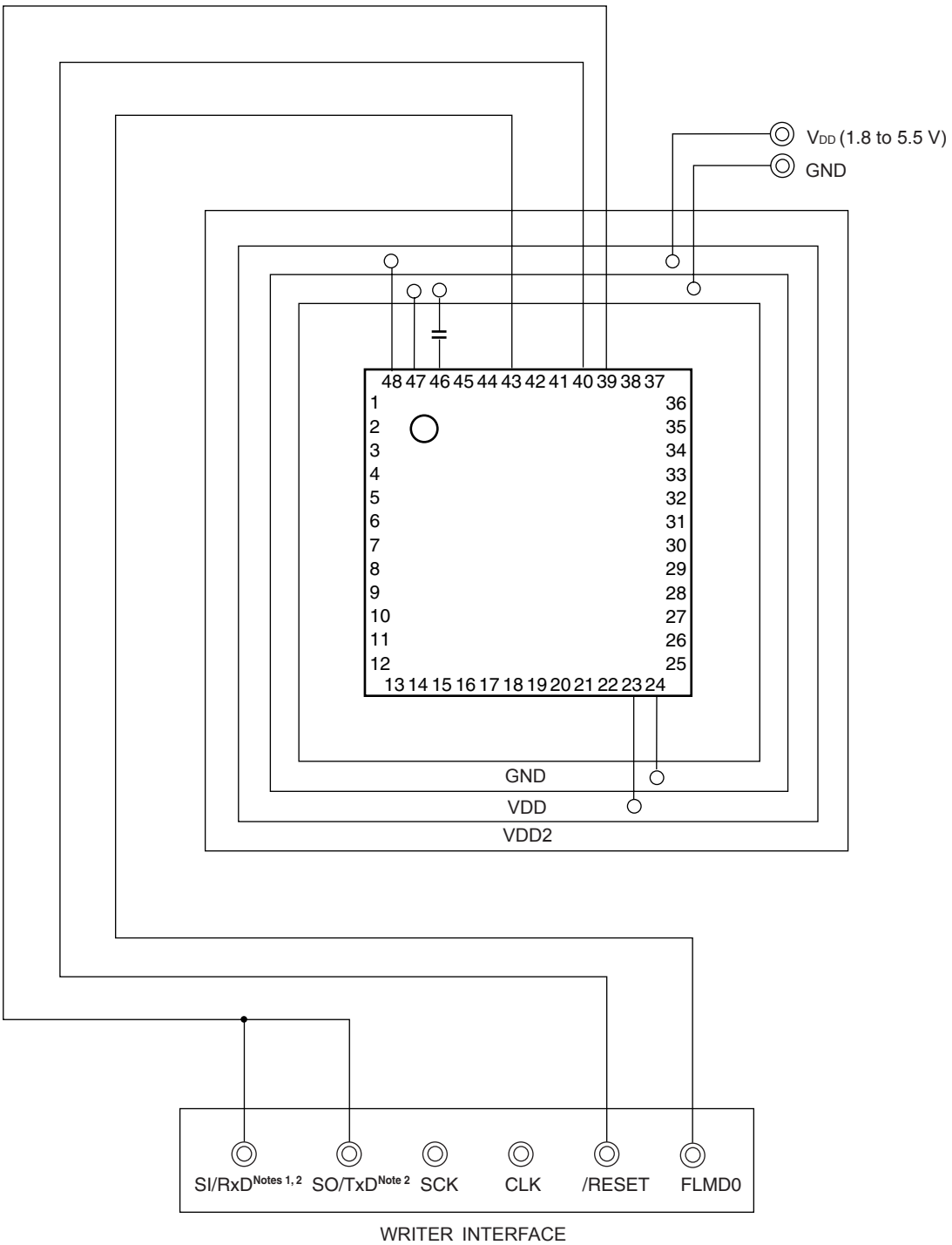
Notes 1. Under development

2. This pin is not required to be connected when using PG-FP5 or FL-PR5.

3. Connect SI/RxD or SO/TxD when using QB-MINI2.

4. μPD78F1013 and μPD78F1014 only

Figure 26-3. Example of Wiring Adapter for Flash Memory Writing (48-pin products of 78K0R/KC3-L)



Notes 1. This pin is not required to be connected when using PG-FP5 or FL-PR5.

2. Connect SI/RxD or SO/TxD when using QB-MINI2.

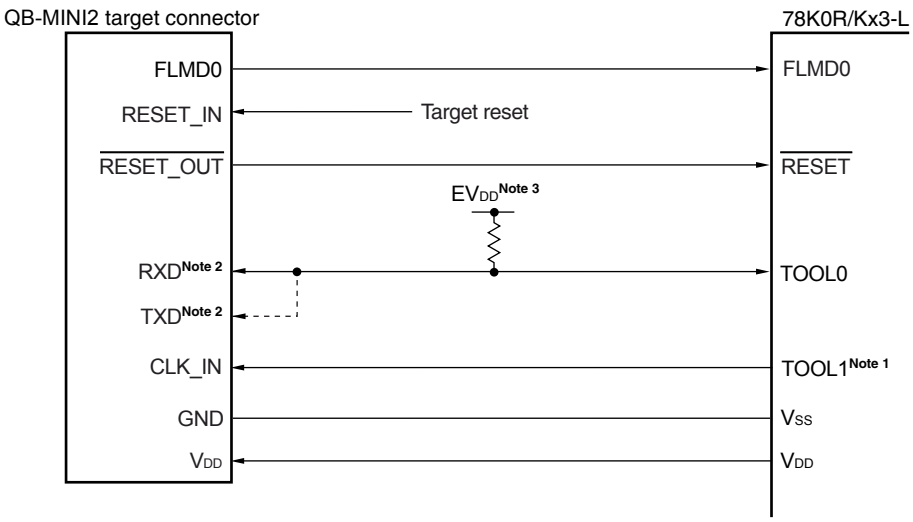
CHAPTER 27 ON-CHIP DEBUG FUNCTION

27.1 Connecting QB-MINI2 to 78K0R/Kx3-L

The 78K0R/Kx3-L uses the V_{DD}, FLMD0, $\overline{RESET}$, TOOL0, TOOL1[Note 1], and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2).

Caution The 78K0R/Kx3-L has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 27-1. Connection Example of QB-MINI2 and 78K0R/Kx3-L



Notes 1. Connection is not required for communication in 1-line mode but required for communication in 2-line mode. At this time, perform necessary connections according to Table 2-3 Connection of Unused Pins (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) or Table 3-3 Connection of Unused Pins (78K0R/KF3-L, 78K0R/KG3-L) since TOOL1 is an unused pin when QB-MINI2 is unconnected.

2. Connecting the dotted line is not necessary since RXD and TXD are shorted within QB-MIN2. When using the other flash memory programmer, RXD and TXD may not be shorted within the programmer. In this case, they must be shorted on the target system.

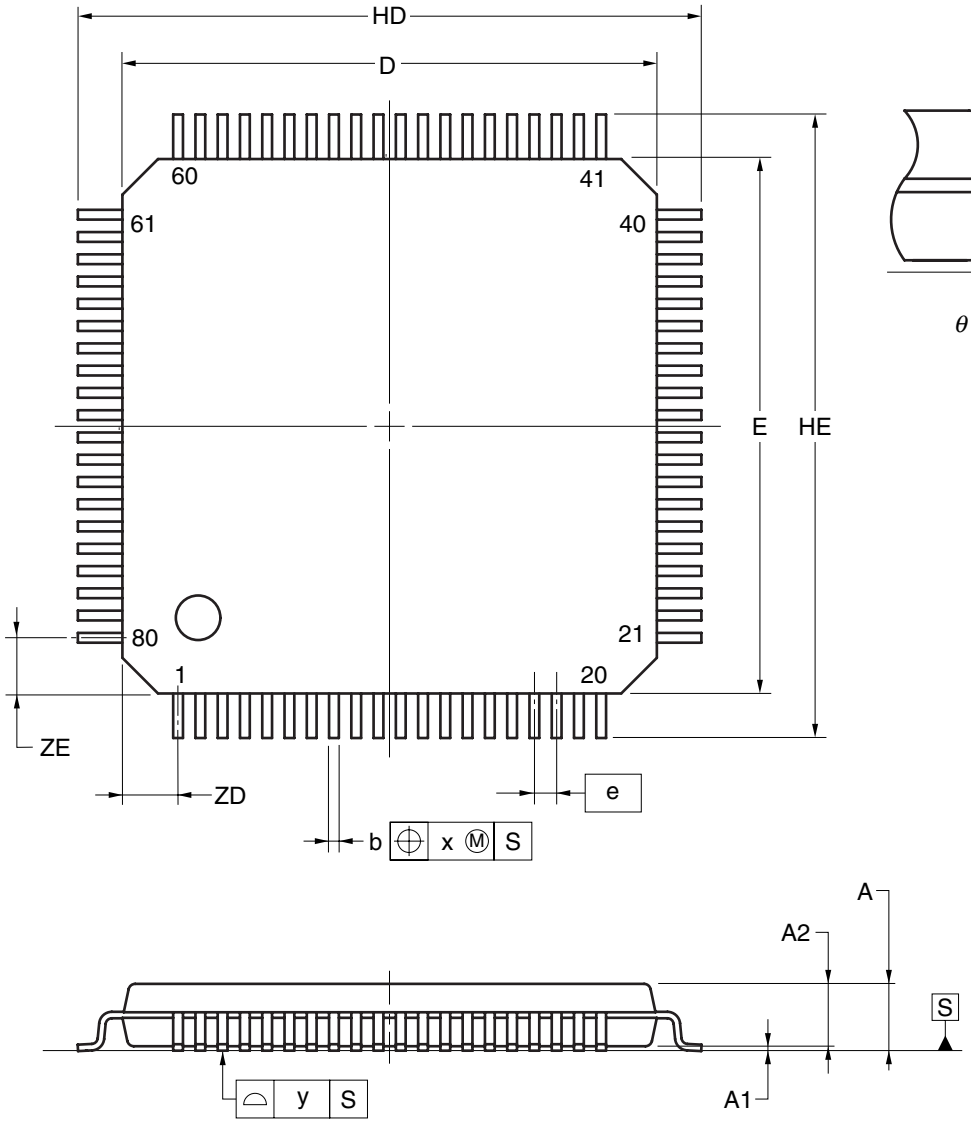
3. When using the 78K0R/KG3-L, read EV_{DD} as EV_{DD0} and EV_{DD1}.

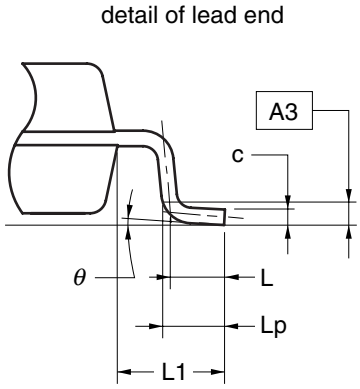
Caution When communicating in 2-line mode, a clock with a frequency of half that of the CPU clock frequency is output from the TOOL1 pin. A resistor or ferrite bead can be used as a countermeasure against fluctuation of the power supply caused by that clock.

Remark The FLMD0 pin is recommended to be open for self-programming in on-chip debugging. To pull down externally, use a resistor of 100 kΩ or more.

μPD78F1010GK-GAK-AX, 78F1011GK-GAK-AX, 78F1012GK-GAK-AX, 78F1027GK-GAK-AX, 78F1028GK-GAK-AX

80-PIN PLASTIC LQFP (FINE PITCH) (12x12)





(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.20^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

P80GK-50-GAK

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.