Renesas Electronics America Inc - UPD78F1008GK-GAJ-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1008gk-gaj-ax

(2) Non-port functions (1/3): 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI11				P150 to P153
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P50/$\overline{\text{SCK40}}$[Note]
INTP2				P51/SI40[Note]/RxD4[Note]
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP6				P140/PCLBUZ0
INTP7				P55/PCLBUZ1/SO41[Note]
INTP8 to INTP11				P74/KR4 to P77/KR7
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73
KR4 to KR7				P74/INTP8 to P77/INTP11
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140/INTP6
PCLBUZ1				P55/INTP7
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: target).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD2	Input	Serial data input to UART2	Input port	P143/SI20/SDA20
RxD3	Input	Serial data input to UART3	Input port	P14
RxD4[Note]	Input	Serial data input to UART4	Input port	P51/INTP2/SI40[Note]
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P10
$\overline{\text{SCK01}}$				P43
$\overline{\text{SCK10}}$				P04/SCL10
$\overline{\text{SCK20}}$				P142/SCL20
$\overline{\text{SCK40}}$				P50/INTP1
$\overline{\text{SCK41}}$				P53/TI00
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SCL20				P142/$\overline{\text{SCK20}}$

Note $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TI03

This is a pin for inputting an external count clock/capture trigger to 16-bit timer 03.

(c) TO03

This is a timer output pin from 16-bit timer 03.

(d) RTC1HZ

This is a real-time counter correction clock (1 Hz) output pin.

3.2.5 P40 to P47 (port 4)

P40 to P47 function as an I/O port. These pins also function as external interrupt request input, serial interface data I/O, clock I/O, data I/O for a flash memory programmer/debugger, clock output, and timer I/O.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P40/TOOL0	√	√
P41/TOOL1	√	√
P42/TI04/TO04	√	√
P43/$\overline{\text{SCK01}}$	√	√
P44/SI01	√	√
P45/SO01	√	√
P46/INTP1/TI05/TO05	P46 Note 1	√
P47/INTP2	P47 Note 2	√

Notes 1. INTP1 and TI05/TO05 are shared with P50 and P05, respectively, in the 78K0R/KF3-L.

2. INTP2 is shared with P51, in the 78K0R/KF3-L.

The following operation modes can be specified in 1-bit units.

(1) Port mode

P40 to P47 function as an I/O port. P40 to P47 can be set to input or output port in 1-bit units using port mode register 4 (PM4). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 4 (PU4).

Be sure to connect an external pull-up resistor to P40 when on-chip debugging is enabled (by using an option byte).

(2) Control mode

P40 to P47 function as serial interface data I/O, clock I/O, external interrupt request input, data I/O for a flash memory programmer/debugger, clock output, and timer I/O.

5.2.6 Port 5

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P50/TI06/TO06	√		√	√	P50[Note]
P51/TI07/TO07	√		√	√	P51[Note]
P52/RTC1HZ/ SLTI/SLTO	–	√	√	√	√
P53	–		–	–	√

Note TI06/TO06 and TI07/TO07 are shared only in the 78K0R/KC3-L and 78K0R/KD3-L. The 78K0R/KE3-L does not have a sharing function.

Remark √: Mounted

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units using port mode register 5 (PM5). When the P50 to P53 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

This port can also be used for real-time counter correction clock output and timer I/O.

Reset signal generation sets port 5 to input mode.

Figures 5-11 to 5-13 show block diagrams of port 5.

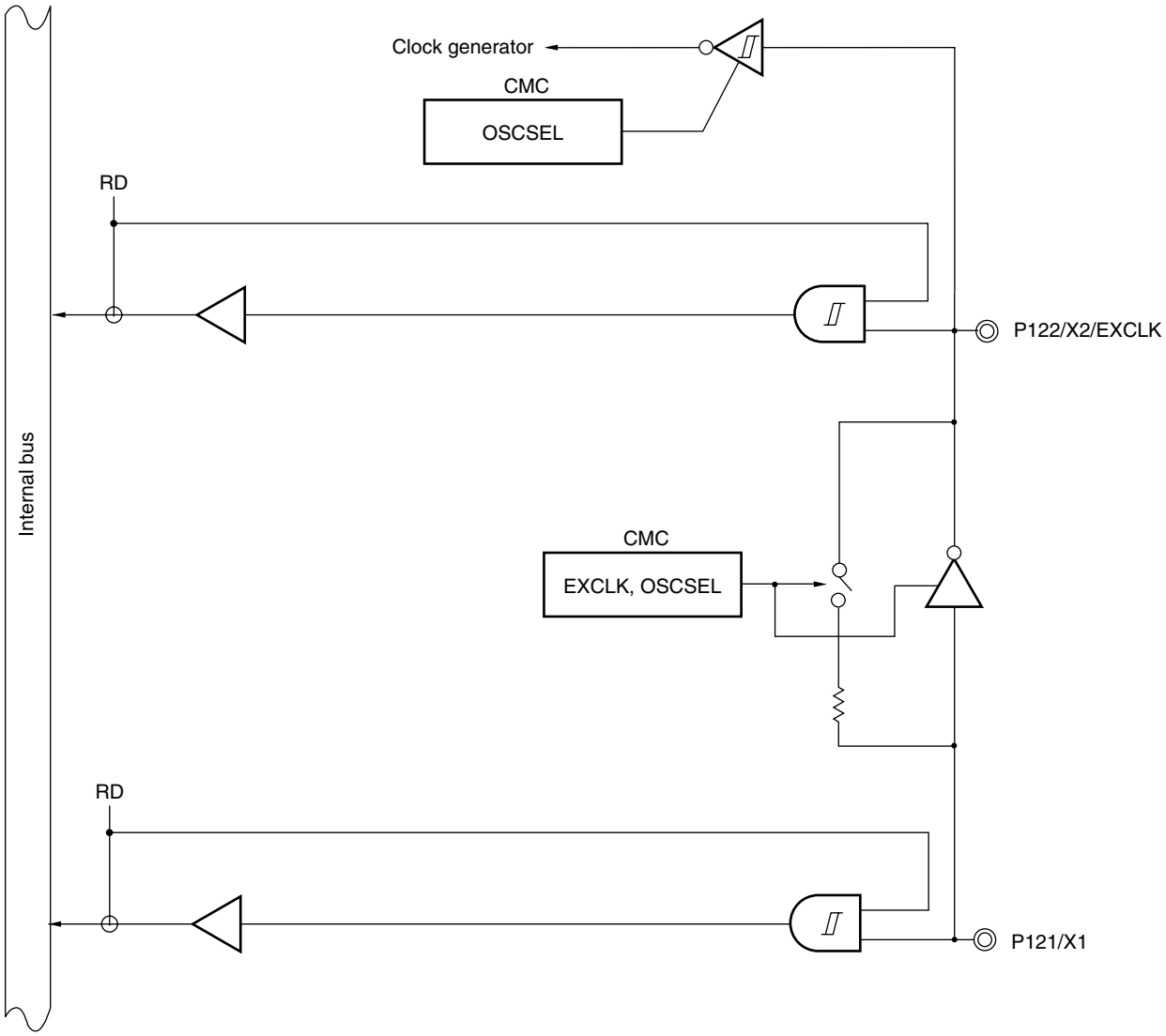
Caution 1. To use P50/TI06/TO06 and P51/TI07/TO07 as a general-purpose port, set bits 6 and 7 (TO06 and TO07) of timer output register 0 (TO0) and bits 6 and 7 (TOE06 and TOE07) of timer output enable register 0 (TOE0) to "0", which is the same as their default status setting.

2. To use P52/RTC1HZ/SLTI/SLTO as a general-purpose port, check which timer I/O pin of which channel n is selected in the input switching control register (ISC) setting. Also, set bit n (TO0n) of timer output register 0 (TO0) and bit n (TOE0n) of timer output enable register 0 (TOE0) to "0", which is the same setting as in the initial state of each.

3. In the case of the 78K0R/KC3-L (40-pin), be sure to clear bit2 of the PM5 register to "0" after the reset release.

Remark n = 0, 1

Figure 5-23. Block Diagram of P121 and P122



CMC: Clock operation mode control register
RD: Read signal

Figure 6-52. Format of Port Mode Register (78K0R/KF3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	1	1	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	1	PM31	PM30	FFF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM9	1	1	1	1	1	1	PM91	PM90	FFF29H	FFH	R/W
PM11	1	1	1	1	1	1	PM111	PM110	FFF2BH	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM14	1	1	1	PM144	PM143	PM142	1	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	1	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 7, 9, 11, 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 0, 1 and 7 of the PM0 register, bits 2 to 7 of the PM3 register, bits 6 and 7 of the PM5 register, bits 2 to 7 of the PM9 register, bits 2 to 7 of the PM11 register, bits 1 to 7 of the PM12 register, bits 1 and 5 to 7 of the PM14 register, and bits 4 to 7 of the PM15 register to "1".

Figure 7-10. Format of Peripheral Enable Registers 0, 1, 2 (PER0, PER1, PER2)
(78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L) (2/2)

Address: F00F0H After reset: 00H R/W

Symbol	<7>	6	<5>	<4>	3	<2>	1	0
PER0	RTCEN Note 1	0	ADCEN	IICAEN Note 2	0	SAU0EN	0	0

Address: F00F1H After reset: 00H R/W

Symbol	7	6	5	4	<3>	2	1	0
PER1	0	0	0	0	OACMPEN	0	0	0

Address: F00F2H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
PER2	0	0	0	0	0	0	0	TAU0EN

Bit 2 (PER0)

SAU0EN	Control of serial array unit 0 input clock supply
0	Stops input clock supply. • SFR used by the serial array unit 0 cannot be written. • The serial array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by the serial array unit 0 can be read and written.

Bit 3 (PER1)

OACMPEN	Control of comparator and programmable gain amplifier input clock supply
0	Stops input clock supply. • SFR used by the comparator and programmable gain amplifier cannot be written. • The comparator and programmable gain amplifier is in the reset status.
1	Enables input clock supply. • SFR used by the comparator and programmable gain amplifier can be read and written.

Bit 0 (PER2)

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply. • SFR used by timer array unit 0 cannot be written. • Timer array unit 0 is in the reset status.
1	Enables input clock supply. • SFR used by timer array unit 0 can be read and written.

Notes 1. This is not mounted onto 40-pin product of the 78K0R/KC3-L.

2. This is not mounted onto 40-pin and 44-pin products of the 78K0R/KC3-L.

Caution Be sure to clear bits 0, 1, 3, and 6 (40-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, 6, and 7, 44-pin product of the 78K0R/KC3-L: bits 0, 1, 3, 4, and 6) of the PER0 register, bits 0 to 2 and 4 to 7 of the PER1 register, and bits 1 to 7 of the PER2 register to 0.

Figure 8-11. Format of Timer Mode Register mn (TMRmn) (2/3)

Address: F0190H, F0191H (TMR00) to F019EH, F019FH (TMR07) After reset: 0000H R/W
F01C8H, F01C9H (TMR10) to F01CEH, F01CFH (TMR13)

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TMRmn	CKSmn	0	0	CCSmn	MASTERmn	STSmn2	STSmn1	STSmn0	CISmn1	CISmn0	0	0	MDmn3	MDmn2	MDmn1	MDmn0

MASTERmn	Selection between using channel n independently or simultaneously with another channel(as a slave or master)
0	Operates in independent channel operation function or as slave channel in simultaneous channel operation function.
1	Operates as master channel in simultaneous channel operation function.
Only the even channel can be set as a master channel (MASTERmn = 1). Be sure to use odd-numbered channels as slave channels (MASTERmn = 0). Clear the MASTERmn bit to 0 for a channel that is used with the independent channel operation function.	

STSmn2	STSmn1	STSmn0	Setting of start trigger or capture trigger of channel n
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TImn pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TImn pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

CISmn1	CISmn0	Selection of TImn pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge
If both the edges are specified when the value of the STSmn2 to STSmn0 bits is other than 010B, set the CISmn1 to CISmn0 bits to 10B.		

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-60. Operation Procedure When Input Signal High-/Low-Level Width Measurement Function Is Used

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode register mn (TMRmn) (determines operation mode of channel). Clears the TOEmn bit to 0 and stops operation of TOmn.	Channel stops operating. (Clock is supplied and some power is consumed.)
Operation start	Sets the TSmn bit to 1. → The TSmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 1, and the TImn pin start edge detection wait status is set.
	Detects the TImn pin input count start valid edge. →	Clears timer/counter register mn (TCRmn) to 0000H and starts counting up.
During operation	Set value of the TDRmn register can be changed. The TCRmn register can always be read. The TSRmn register is not used. Set values of the TMRmn register, TOMmn, TOLmn, TOmn, and TOEmn bits cannot be changed.	When the TImn pin start edge is detected, the counter (TCRmn) counts up from 0000H. If a capture edge of the TImn pin is detected, the count value is transferred to timer data register mn (TDRmn) and INTTMmn is generated. If an overflow occurs at this time, the OVF bit of timer status register mn (TSRmn) is set; if an overflow does not occur, the OVF bit is cleared. The TCRmn register stops the count operation until the next TImn pin start edge is detected.
Operation stop	The TTmn bit is set to 1. → The TTmn bit automatically returns to 0 because it is a trigger bit.	TEmn = 0, and count operation stops. The TCRmn register holds count value and stops. The OVF bit of the TSRmn register is also held.
TAU stop	The TAU0EN and TAU1EN bits of the PER0 and PER2 registers are cleared to 0. Note →	Power-off status All circuits are initialized and SFR of each channel is also initialized.

Operation is resumed.

Note 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: TAU0EN bit of the PER2 register
78K0R/KF3-L, 78K0R/KG3-L: TAU0EN or TAU1EN bit of the PER0 register

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn) and the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-75. Operation Procedure When Multiple PWM Output Function Is Used (1/3)

	Software Operation	Hardware Status
TAU default setting		Power-off status (Clock supply is stopped and writing to each register is disabled.)
	Sets the TAU0EN and TAU1EN bits of peripheral enable registers 0, 2 (PER0, PER2) to 1. Note →	Power-on status. Each channel stops operating. (Clock supply is started and writing to each register is enabled.)
	Sets timer clock select register m (TPSm). Determines clock frequencies of CKm0 and CKm1.	
Channel default setting	Sets timer mode registers mn, mp, mq (TMRmn, TMRmp, TMRmq) of each channel to be used (determines operation mode of channels). An interval (period) value is set to timer data register mn (TDRmn) of the master channel, and a duty factor is set to the TDRmp and TDRmq registers of the slave channels.	Channel stops operating. (Clock is supplied and some power is consumed.)
	Sets slave channels. The TOMmp and TOMmq bits of timer output mode register m (TOMm) are set to 1 (slave channel output mode). Clears the TOLmp and TOLmq bits to 0. Sets the TOmp and TOmq bits and determines default level of the TOmp and TOmq outputs. →	The TOmp and TOmq pins go into Hi-Z output state. The TOmp and TOmq default setting levels are output when the port mode register is in output mode and the port register is 0.
	Sets the TOEmp and TOEmq bits to 1 and enables operation of TOmp and TOmq. →	TOmp and TOmq do not change because channels stop operating.
	Clears the port register and port mode register to 0. →	The TOmp and TOmq pins output the TOmp and TOmq set levels.

(**Note** and **Remark** are listed on the next page.)

(3) Real-time counter control register 1 (RTCC1)

The RTCC1 register is an 8-bit register that is used to control the alarm interrupt function and the wait time of the counter.

The RTCC1 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-4. Format of Real-Time Counter Control Register 1 (RTCC1) (1/2)

Address: FFF9EH After reset: 00H R/W

Symbol	<7>	<6>	5	<4>	<3>	2	<1>	<0>
RTCC1	WALE	WALIE	0	WAFG	RIFG	0	RWST	RWAIT

WALE	Alarm operation control
0	Match operation is invalid.
1	Match operation is valid.
When setting a value to the WALE bit while the counter operates (RTCE = 1) and WALIE = 1, rewrite the WALE bit after disabling interrupt servicing INTRTC by using the interrupt mask flag register. Furthermore, clear the WAFG and RTCIF flags after rewriting the WALE bit. When setting each alarm register (WALIE flag of real-time counter control register 1 (RTCC1), the alarm minute register (ALARMWM), the alarm hour register (ALARMWH), and the alarm week register (ALARMWW)), set match operation to be invalid (“0”) for the WALE bit.	

WALIE	Control of alarm interrupt (INTRTC) function operation
0	Does not generate interrupt on matching of alarm.
1	Generates interrupt on matching of alarm.

WAFG	Alarm detection status flag
0	Alarm mismatch
1	Detection of matching of alarm
This is a status flag that indicates detection of matching with the alarm. It is valid only when WALE = 1 and is set to “1” one clock (32.768 kHz) after matching of the alarm is detected. This flag is cleared when “0” is written to it. Writing “1” to it is invalid.	

(7) Minute count register (MIN)

The MIN register is an 8-bit register that takes a value of 0 to 59 (decimal) and indicates the count value of minutes.

It counts up when the second counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the second count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Set a decimal value of 00 to 59 to this register in BCD code. If a value outside the range is set, the register value returns to the normal value after 1 period.

The MIN register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 9-8. Format of Minute Count Register (MIN)

Address: FFF93H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MIN	0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1

(8) Hour count register (HOUR)

The HOUR register is an 8-bit register that takes a value of 00 to 23 or 01 to 12 and 21 to 32 (decimal) and indicates the count value of hours.

It counts up when the minute counter overflows.

When data is written to this register, it is written to a buffer and then to the counter up to 2 clocks (32.768 kHz) later.

Even if the minute count register overflows while this register is being written, this register ignores the overflow and is set to the value written. Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time counter control register 0 (RTCC0).

If the AMPM bit value is changed, the values of the HOUR register change according to the specified time system.

If a value outside the range is set, the register value returns to the normal value after 1 period.

The HOUR register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 12H.

However, the value of this register is 00H if the AMPM bit (bit 3 of the RTCC0 register) is set to 1 after reset.

Figure 9-9. Format of Hour Count Register (HOUR)

Address: FFF94H After reset: 12H R/W

Symbol	7	6	5	4	3	2	1	0
HOUR	0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1

Caution Bit 5 (HOUR20) of the HOUR register indicates AM(0)/PM(1) if AMPM = 0 (if the 12-hour system is selected).

(3) Serial mode register mn (SMRmn)

The SMRmn register is a register that sets an operation mode of channel n. It is also used to select an operation clock (f_{MCK}), specify whether the serial clock (f_{SCK}) may be input or not, set a start trigger, an operation mode (CSI, UART, or I^2C), and an interrupt source. This register is also used to invert the level of the receive data only in the UART mode.

Rewriting the SMRmn register is prohibited when the register is in operation (when SEmn = 1). However, the MDmn0 bit can be rewritten during operation.

The SMRmn register can be set by a 16-bit memory manipulation instruction.

Reset signal generation sets the SMRmn register to 0020H.

Figure 14-7. Format of Serial Mode Register mn (SMRmn) (1/3)

Address: F0110H, F0111H (SMR00) to F0116H, F0117H (SMR03), F0150H, F0151H (SMR10) to F0156H, F0157H (SMR13), F0208H, F0209H (SMR20) , F020AH, F020BH (SMR21) After reset: 0020H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SMRmn	CKS mn	CCS mn	0	0	0	0	0	STS mn	0	SIS mn0	1	0	0	MD mn2	MD mn1	MD mn0

CKS mn	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CKm0 set by the SPSm register
1	Operation clock CKm1 set by the SPSm register
Operation clock (f_{MCK}) is used by the edge detector. In addition, depending on the setting of the CCSmn bit and the higher 7 bits of the SDRmn register, a transfer clock (f_{TCLK}) is generated.	

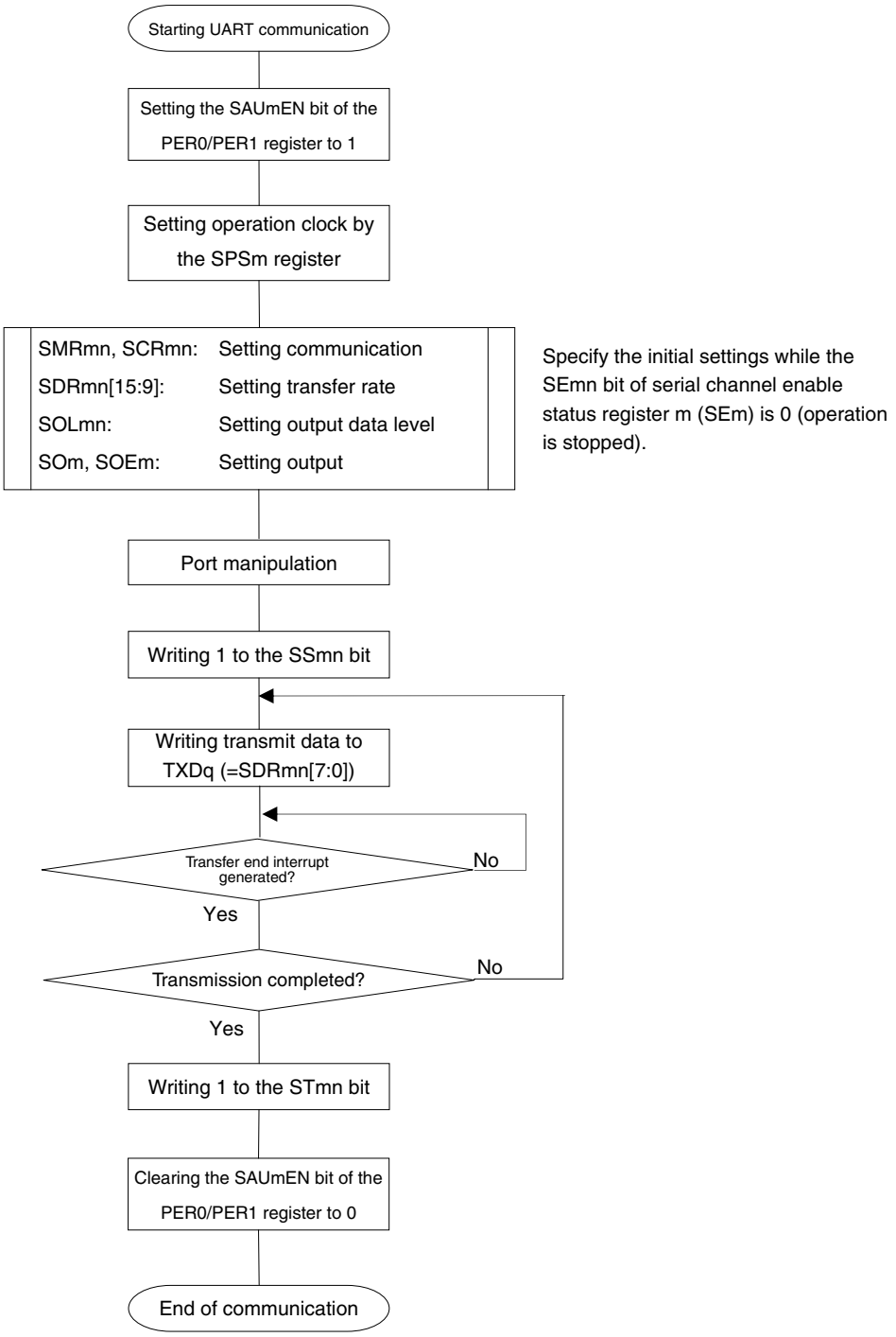
CCS mn	Selection of transfer clock (f_{TCLK}) of channel n
0	Divided operation clock f_{MCK} specified by the CKSmn bit
1	Clock input f_{SCK} from the $\overline{SCKp}$ pin (slave transfer in CSI mode)
Transfer clock f_{TCLK} is used for the shift register, communication controller, output controller, interrupt controller, and error controller. When CCSmn = 0, the division ratio of operation clock (f_{MCK}) is set by the higher 7 bits of the SDRmn register.	

STS mn	Selection of start trigger source
0	Only software trigger is valid (selected for CSI, UART transmission, and simplified I^2C).
1	Valid edge of the RxDq pin (selected for UART reception)
Transfer is started when the above source is satisfied after 1 is set to the SSm register.	

Caution Be sure to clear bits 13 to 9, 7, 4, and 3 to "0". Be sure to set bit 5 to "1".

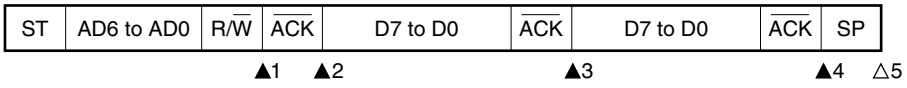
(**Remark** is listed on the next page.)

Figure 14-80. Flowchart of UART Transmission (in Single-Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

(ii) When WTIM = 1



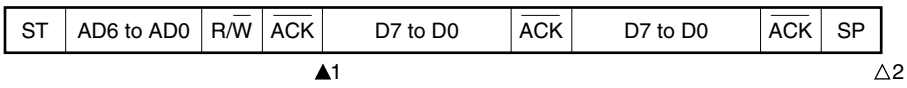
▲1: IICS = 0110×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIM = 1)



▲1: IICS = 01000110B
△2: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1

The meanings of <7> to <15> in (3) Data ~ data ~ stop condition in Figure 15-32 are explained below.

<R> <7> After data transfer is completed, because of ACKE = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<9> The master device writes the data to transmit to the IICA shift register (IICA) and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WREL = 1). The master device then starts transferring data to the slave device.

<R> <11> When data transfer is complete, the slave device (ACKE =1) sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<12> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<13> The slave device reads the received data and releases the wait status (WREL = 1).

<R> <14> By the master device setting a stop condition trigger (SPT = 1), the bus data line is cleared (SDA0 = 0) and the bus clock line is set (SCL0 = 1). After the stop condition setup time has elapsed, by setting the bus data line (SDA0 = 1), the stop condition is then generated (i.e. SCL0 =1 changes SDA0 from 0 to 1).

<R> <15> When a stop condition is generated, the slave device detects the stop condition and issues an interrupt (INTIICA: stop condition).

Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

17.5 Example of Setting of DMA Controller

17.5.1 CSI consecutive transmission

A flowchart showing an example of setting for CSI consecutive transmission is shown below.

- Consecutive transmission of CSI10 (256 bytes)
- DMA channel 0 is used for DMA transfer.
- DMA start source: INTCSI10 (software trigger (STG0) only for the first start source)
- Interrupt of CSI10 is specified by IFC03 to IFC00 = 1000B.
- Transfers FFB00H to FFBFFH (256 bytes) of RAM to FFF44H of the data register (SIO10) of CSI.

Remark IFC03 to IFC00: Bits 3 to 0 of DMA mode control registers 0 (DMC0)

Figure 23-2. Format of Low-Voltage Detection Register (LVIM)

Address: FFFA9H After reset: 00H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	<2>	<1>	<0>
LVIM	LVION	0	0	0	0	LVISEL	LVIMD	LVIF

LVION[Notes 3, 4]	Enables low-voltage detection operation
0	Disables operation
1	Enables operation

LVISEL[Note 3]	Voltage detection selection
0	Detects level of supply voltage (V_{DD})
1	Detects level of input voltage from the external input pin (EXLVI)

LVIMD	Low-voltage detection operation mode (interrupt/reset) selection
0	• LVISEL = 0: Generates an internal interrupt signal when the supply voltage (V_{DD}) drops lower than the detection voltage (V_{LVI}) ($V_{DD} < V_{LVI}$) or when V_{DD} becomes V_{LVI} or higher ($V_{DD} \geq V_{LVI}$). • LVISEL = 1: Generates an interrupt signal when the input voltage from an external input pin (EXLVI) drops lower than the detection voltage (V_{EXLVI}) (EXLVI < V_{EXLVI}) or when EXLVI becomes V_{EXLVI} or higher (EXLVI ≥ V_{EXLVI}).
1	• LVISEL = 0: Generates an internal reset signal when the supply voltage (V_{DD}) < detection voltage (V_{LVI}) and releases the reset signal when $V_{DD} \geq V_{LVI}$. • LVISEL = 1: Generates an internal reset signal when the input voltage from an external input pin (EXLVI) < detection voltage (V_{EXLVI}) and releases the reset signal when EXLVI ≥ V_{EXLVI}.

LVIF	Low-voltage detection flag
0	• LVISEL = 0: Supply voltage (V_{DD}) ≥ detection voltage (V_{LVI}), or when LVI operation is disabled • LVISEL = 1: Input voltage from the external input pin (EXLVI) ≥ detection voltage (V_{EXLVI}), or when LVI operation is disabled
1	• LVISEL = 0: Supply voltage (V_{DD}) < detection voltage (V_{LVI}) • LVISEL = 1: Input voltage from the external input pin (EXLVI) < detection voltage (V_{EXLVI})

Notes 1. The reset value changes depending on the reset source and the setting of the option byte.
This register is not cleared (00H) by LVI reset.
It is set to “82H” when a reset signal other than LVI is applied if option byte LVIOFF = 0, and to “00H” if option byte LVIOFF = 1.

2. Bit 0 is read-only.

3. The LVION, LVIMD, and LVISEL bits are cleared to 0 in the case of a reset other than an LVI reset. These are not cleared to 0 in the case of an LVI reset.

Caution 2. A wait is required to change the operation speed mode control register (OSMC) after changing the regulator mode control register (RMC). Wait for 3.5 ms by software when setting to low consumption current mode and 10 μs when setting to normal current mode, as described in the procedure shown below.

• When setting to low consumption current mode

<1> Select a frequency of 1 MHz for f_{CLK}.
<2> Set the RMC register to 5AH (set the regulator to low consumption current mode).
<3> Wait for 3.5 ms.
<4> Set the FLPC and FSEL bits of the OSMC register to 1 and 0, respectively.

• When setting to normal current mode

<1> Set the RMC register to 00H (set the regulator to normal current mode).
<2> Wait for 10 μs.
<3> Change the FLPC and FSEL bits of the OSMC register.
<4> Change the f_{CLK} frequency.

Table 24-1. Regulator Output Voltage Conditions

Mode	Output Voltage	Condition
Low consumption current mode	1.8 V	In STOP mode (except during OCD mode)
		When both the high-speed system clock (f_{MX}), the high-speed internal oscillation clock (f_{IH}), and the 20 MHz internal high-speed oscillation clock (f_{IH20}) are stopped during CPU operation with the subsystem clock (f_{XT})[Note]
		When both the high-speed system clock (f_{MX}), the high-speed internal oscillation clock (f_{IH}), and the 20 MHz internal high-speed oscillation clock (f_{IH20}) are stopped during the HALT mode when the CPU operation with the subsystem clock (f_{XT}) has been set[Note]
Normal current mode	2.4 V	Other than above

Note The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock. These conditions apply to products other than the 78K0R/KC3-L (40-pin).

Remarks 1. The QB-78K0RKX3C and QB-78F1030 are supplied with a USB interface cable, integrated debugger ID78K0R-QB and on-chip debug emulator with programming function QB-MINI2.

2. The packed contents differ depending on the part number, as follows.

Packed Contents / Part Number	In-Circuit Emulator	Emulation Probe	Exchange Adapter	YQ Connector	Target Connector
QB-78K0RKX3C-ZZZ	QB-78K0RKX3C	None			
QB-78F1030-ZZZ	QB-78F1030				
QB-78K0RKX3C-T80GC	QB-78K0RKX3C	QB-80-EP-01T	QB-80GC-EA-10T	QB-80GC-YQ-01T	QB-80GC-NQ-01T
QB-78K0RKX3C-T80GK			QB-80GK-EA-09T	QB-80GK-YQ-01T	QB-80GK-NQ-01T
QB-78K0RKX3C-T80GC	QB-78F1030		QB-80GC-EA-10T	QB-80GC-YQ-01T	QB-80GC-NQ-01T
QB-78K0RKX3C-T80GK			QB-80GK-EA-09T	QB-80GK-YQ-01T	QB-80GK-NQ-01T
QB-78K0RKX3C-T100GC	QB-78K0RKX3C		QB-100GC-EA-07T	QB-100GC-YQ-01T	QB-100GC-NQ-01T
QB-78K0RKX3C-T100GF			QB-100GF-EA-05T	QB-100GF-YQ-01T	QB-100GF-NQ-01T
QB-78K0RKX3C-T100F1			QB-100F1-EA-01T	None	QB-100F1-NQ-01T
QB-78K0RKX3C-T100GC	QB-78F1030		QB-100GC-EA-07T	QB-100GC-YQ-01T	QB-100GC-NQ-01T
QB-78K0RKX3C-T100GF			QB-100GF-EA-05T	QB-100GF-YQ-01T	QB-100GF-NQ-01T