Renesas Electronics America Inc - UPD78F1010GC-GAD-AX Datasheet

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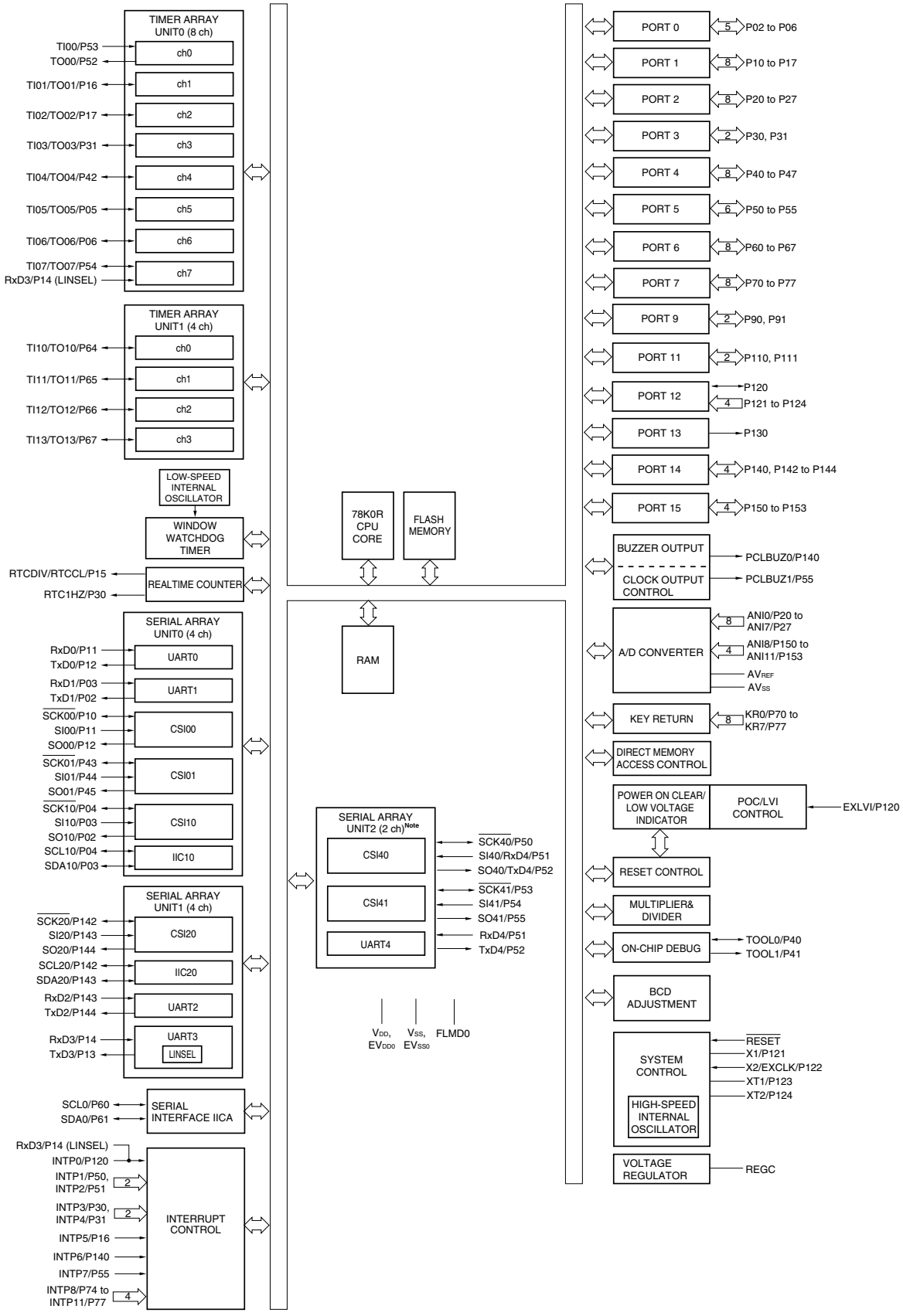
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1010gc-gad-ax

1.6.4 78K0R/KF3-L



Note Serial array unit 2 is only mounted in the μPD78F1027 and 78F1028.

(2/2)

Item		78K0R/KF3-L					78K0R/KG3-L			
		μPD78F1010	μPD78F1011	μPD78F1012	μPD78F1027	μPD78F1028	μPD78F1013	μPD78F1014	μPD78F1029 Note 1	μPD78F1030 Note 1
Clock output/buzzer output		2								
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
10-bit resolution A/D converter (AV_{REF} = 1.8 to 5.5 V)		12 channels					16 channels			
Comparators		–								
Programmable gain amplifiers		–								
Serial interface		• CSI: 2 channels/UART: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART supporting LIN-bus: 1 channel • CSI: 2 channels/UART: 1 channel (μPD78F1027, 78F1028, 78F1029, 78F1030)								
	I^2C bus	1 channel								
Multiplier/divider		• 16 bits × 16 bits = 32 bits (multiplication) • 32 bits ÷ 32 bits = 32 bits (division)								
DMA controller		2 channels								
Vectored interrupt sources	Internal	33			35		33			35
	External	13								
Key interrupt		8 channels (KR0 to KR7)								
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by a reset processing check error								
Power-on-clear circuit		• Power-on-reset: 1.61 ±0.09 V • Power-down-reset: 1.59 ±0.09 V								
Low-voltage detector		1.91 V to 4.22 V (16 stages)								
On-chip debug function		Provided								
Power supply voltage		V_{DD} = 1.8 to 5.5 V								
Operating ambient temperature		T_A = −40 to +85 °C								

Notes 1. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.2.4 P30 to P33 (port 3)

P30 to P33 function as an I/O port. These pins also function as serial interface data I/O, clock I/O, and external interrupt request input.

Input to the P30 and P31 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units, using port input mode register 3 (PIM3).

Output from the P30 to P32 pins can be specified as normal CMOS output or N-ch open-drain output (V_{DD} tolerance) in 1-bit units, using port output mode register 3 (POM3).

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P30/SO10/TxD1	√		√	√	√
P31/SI10/RxD1/ SDA10/INTP1	√		√	√	√
P32/$\overline{\text{SCK10}}$/ SCL10/INTP2	√		√	√	√
P33	–		–	–	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P33 function as an I/O port. P30 to P33 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P33 function as serial interface data I/O, clock I/O, and external interrupt request input.

(a) SI10

This is a serial data input pin of serial interface CSI10.

(b) SO10

This is a serial data output pin of serial interface CSI10.

(c) $\overline{\text{SCK10}}$

This is a serial clock I/O pin of serial interface CSI10.

(d) TxD1

This is a serial data output pin of serial interface UART1.

(e) RxD1

This is a serial data input pin of serial interface UART1.

(2) Non-port functions (1/3): 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
ANI0 to ANI7	Input	A/D converter analog input	Digital input port	P20 to P27
ANI8 to ANI11				P150 to P153
EXLVI	Input	Potential input for external low-voltage detection	Input port	P120/INTP0
INTP0	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input port	P120/EXLVI
INTP1				P50/$\overline{\text{SCK40}}$[Note]
INTP2				P51/SI40[Note]/RxD4[Note]
INTP3				P30/RTC1HZ
INTP4				P31/TI03/TO03
INTP5				P16/TI01/TO01
INTP6				P140/PCLBUZ0
INTP7				P55/PCLBUZ1/SO41[Note]
INTP8 to INTP11				P74/KR4 to P77/KR7
KR0 to KR3	Input	Key interrupt input	Input port	P70 to P73
KR4 to KR7				P74/INTP8 to P77/INTP11
PCLBUZ0	Output	Clock output/buzzer output	Input port	P140/INTP6
PCLBUZ1				P55/INTP7
REGC	–	Connecting regulator output (2.4 V) stabilization capacitance for internal operation. Connect to V_{SS} via a capacitor (0.47 to 1 μF: target).	–	–
RTCDIV	Output	Real-time counter clock (32 kHz divided frequency) output	Input port	P15/RTCCL
RTCCL	Output	Real-time counter clock (32 kHz original oscillation) output	Input port	P15/RTCDIV
RTC1HZ	Output	Real-time counter correction clock (1 Hz) output	Input port	P30/INTP3
$\overline{\text{RESET}}$	Input	System reset input	–	–
RxD0	Input	Serial data input to UART0	Input port	P11/SI00
RxD1	Input	Serial data input to UART1	Input port	P03/SI10/SDA10
RxD2	Input	Serial data input to UART2	Input port	P143/SI20/SDA20
RxD3	Input	Serial data input to UART3	Input port	P14
RxD4[Note]	Input	Serial data input to UART4	Input port	P51/INTP2/SI40[Note]
$\overline{\text{SCK00}}$	I/O	Clock input/output for CSI00, CSI01, CSI10, CSI20, CSI40, and CSI41	Input port	P10
$\overline{\text{SCK01}}$				P43
$\overline{\text{SCK10}}$				P04/SCL10
$\overline{\text{SCK20}}$				P142/SCL20
$\overline{\text{SCK40}}$				P50/INTP1
$\overline{\text{SCK41}}$				P53/TI00
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P04/$\overline{\text{SCK10}}$
SCL20				P142/$\overline{\text{SCK20}}$

Note $\overline{\text{SCK40}}$, $\overline{\text{SCK41}}$, SI40, SI41, SO40, SO41, TxD4, RxD4 are only mounted in the μPD78F1027 and 78F1028.

4.2.4 Special function registers (SFRs)

Unlike a general-purpose register, each SFR has a special function.

SFRs are allocated to the FFF00H to FFFFFH area.

SFRs can be manipulated like general-purpose registers, using operation, transfer, and bit manipulation instructions. The manipulable bit units, 1, 8, and 16, depend on the SFR type.

Each manipulation bit unit can be specified as follows.

- 1-bit manipulation
  Describe the symbol reserved by the assembler for the 1-bit manipulation instruction operand (sfr.bit). This manipulation can also be specified with an address.
- 8-bit manipulation
  Describe the symbol reserved by the assembler for the 8-bit manipulation instruction operand (sfr). This manipulation can also be specified with an address.
- 16-bit manipulation
  Describe the symbol reserved by the assembler for the 16-bit manipulation instruction operand (sfrp). When specifying an address, describe an even address.

Table 4-5 gives a list of the SFRs. The meanings of items in the table are as follows.

- Symbol
  Symbol indicating the address of a special function register. It is a reserved word in the RA78K0R, and is defined as an sfr variable using the #pragma sfr directive in the CC78K0R. When using the RA78K0R, ID78K0R-QB, and SM+ for 78K0R, symbols can be written as an instruction operand.
- R/W
  Indicates whether the corresponding SFR can be read or written.
  R/W: Read/write enable
  R: Read only
  W: Write only
- Manipulable bit units
  "√" indicates the manipulable bit unit (1, 8, or 16). "–" indicates a bit unit for which manipulation is not possible.
- After reset
  Indicates each register status upon reset signal generation.

Caution Do not access addresses to which extended SFRs are not assigned.

Remark For extended SFRs (2nd SFRs), see **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

(6) 20 MHz internal high-speed oscillation control register (DSCCTL)

This register controls the 20 MHz internal high-speed oscillation clock (DSC) function.

This register can be used to control oscillation of the 20 MHz internal high-speed oscillation clock (f_{IH20}) and select the 20 MHz internal high-speed oscillation clock (f_{IH20}) as the CPU/peripheral hardware clock.

The DSCCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 7-9. Format of 20 MHz Internal High-Speed Oscillation Control Register (DSCCTL)

Address: F00F6H After reset: 00H R/W[Note]

Symbol	7	6	5	4	<3>	<2>	1	<0>
DSCCTL	0	0	0	0	DSCS	SELDSC	0	DSCON

DSCS	20 MHz internal high-speed oscillation supply status flag
0	Not supplied
1	Supplied (The CPU/peripheral hardware clock (f_{CLK}) operates on the 20 MHz internal high-speed oscillation clock.)

SELDSC	Selection of 20 MHz internal high-speed oscillation for CPU/peripheral hardware clock (f_{CLK})
0	Does not select 20 MHz internal high-speed oscillation (clock selected by the system clock control register (CKC) is supplied to f_{CLK})
1	Selects 20 MHz internal high-speed oscillation (20 MHz internal high-speed oscillation is supplied to f_{CLK})

DSCON	Operating or stopping 20 MHz internal high-speed oscillation clock (f_{IH20})
0	Stopped
1	Operated

Note Bit 3 is read-only.

Cautions 1. 20 MHz internal oscillation can only be used if $V_{DD} \geq 2.7$ V.

2. Set the SELDSC bit when 100 μs have elapsed after the DSCON bit has been set with $V_{DD} \geq 2.7$ V.

3. The internal high-speed oscillator must be operated (HIOSTOP = 0) when DSCON = 1.

4. If 1 MHz internal oscillation is selected by using the option byte, 20 MHz internal high-speed oscillation cannot be used. Do not set (1) the DSCON bit.

11.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by the clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by the clock output select register 1 (CKS1).

11.4.1 Operation as output pin

The PCLBUZn pin is output as the following procedure.

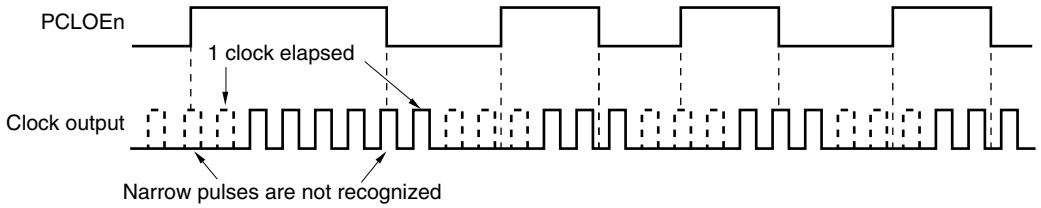
<1> Select the output frequency with bits 0 to 3 (CCSn0 to CCSn2, CSELn) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled status).

<2> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

Remarks 1. The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output. Figure 11-4 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

2. n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

Figure 11-4. Remote Control Output Application Example



(11) Serial output enable register m (SOEm)

The SOEm register is a register that is used to enable or stop output of the serial communication operation of each channel.

Channel n that enables serial output cannot rewrite by software the value of the SOmn bit of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial data output pin.

For channel n, whose serial output is stopped, the SOmn bit value of the SOm register can be set by software, and that value can be output from the serial data output pin. In this way, any waveform of the start condition and stop condition can be created by software.

The SOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the SOEm register can be set with an 1-bit or 8-bit memory manipulation instruction with SOEmL.

Reset signal generation clears the SOEm register to 0000H.

Figure 14-15. Format of Serial Output Enable Register m (SOEm)

Address: F012AH, F012BH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE02	SOE01	SOE00

Address: F016AH, F016BH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE1	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE12	0	SOE10

Address: F021AH, F021BH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOE2 Note	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SOE21	SOE20

SOEmn	Serial output enable/stop of channel n
0	Stops output by serial communication operation.
1	Enables output by serial communication operation.

Note SOE2 register is only mounted in the 78K0R/KF3-L (μ PD78F1027, 78F1028) and 78K0R/KG3-L (μ PD78F1029, 78F1030).

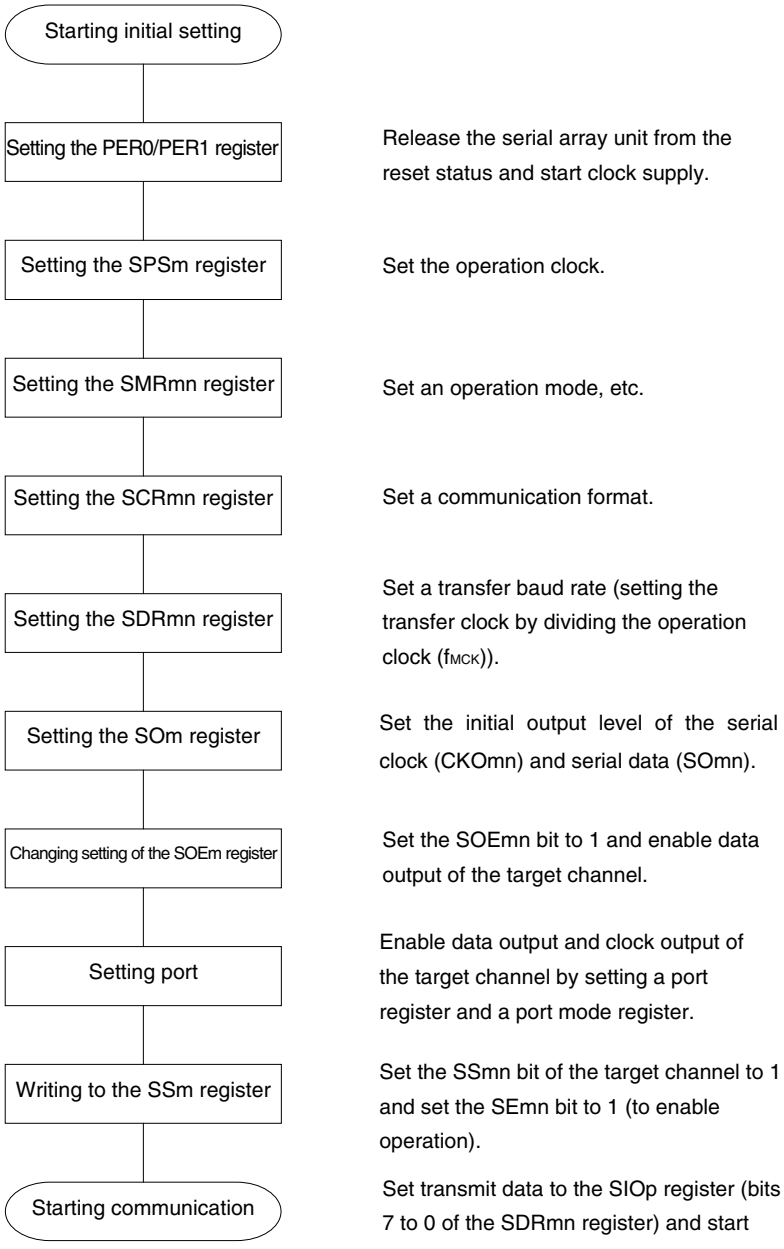
Caution Be sure to clear bits 15 to 3 of the SOE0 register, bits 1 and 15 to 3 of the SOE1 register, and bits 15 to 2 of the SOE2 registers to "0".

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L□μ PD78F1010, 78F1011, 78F1012□: mn = 00 to 02, 10, 12
78K0R/KF3-L□μ PD78F1027, 78F1028□: mn = 00 to 02, 10, 12, 20, 21
78K0R/KG3-L□μ PD78F1013, 78F1014□: mn = 00 to 02, 10, 12
78K0R/KG3-L□μ PD78F1029, 78F1030□: mn = 00 to 02, 10, 12, 20, 21

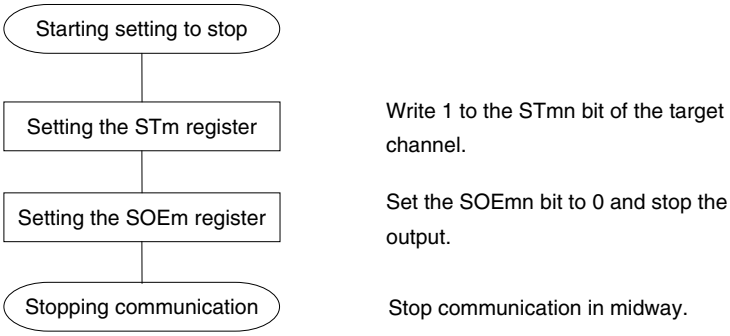
(2) Operation procedure

Figure 14-29. Initial Setting Procedure for Master Transmission



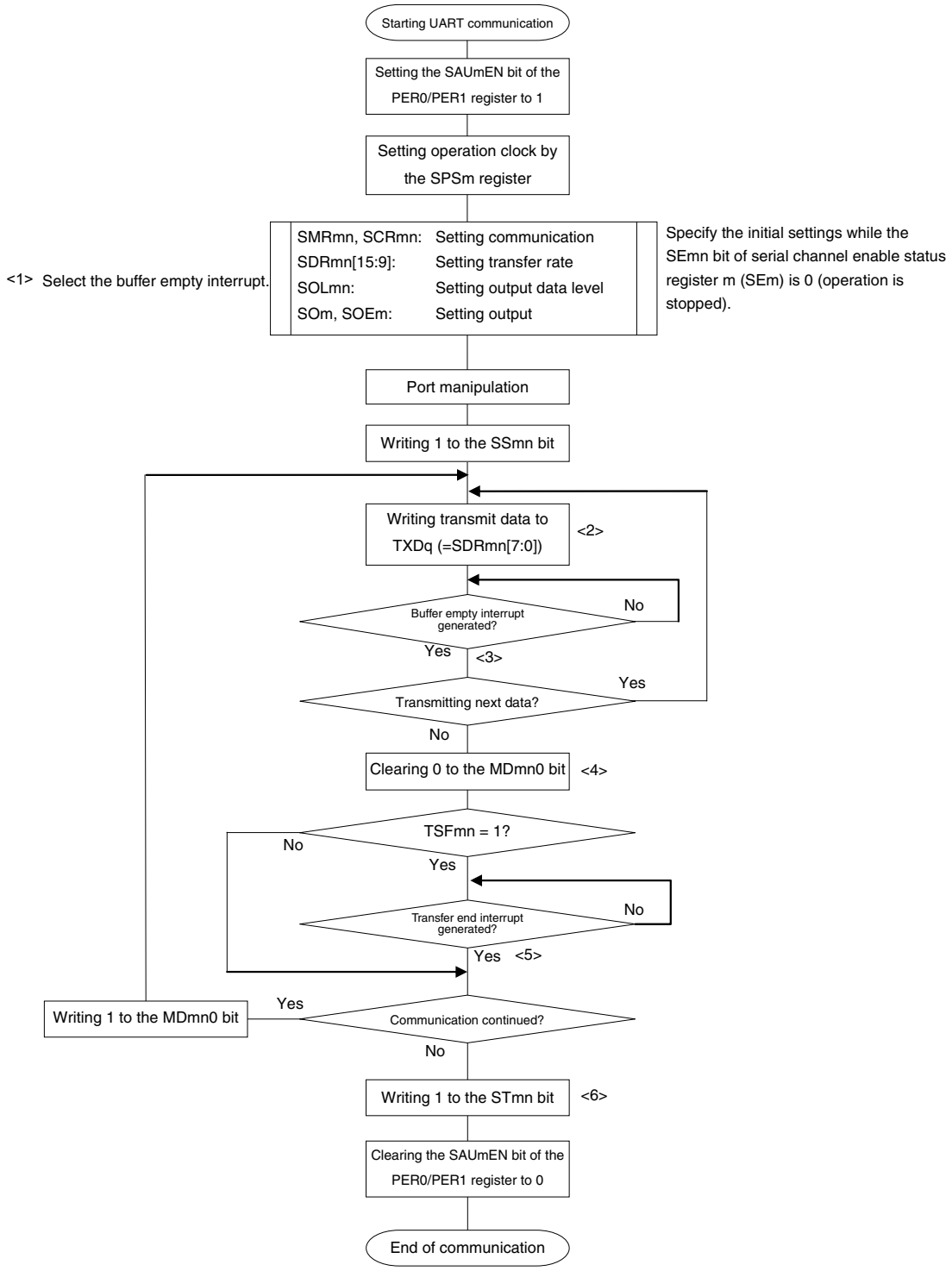
Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Figure 14-77. Procedure for Stopping UART Transmission



Remark Even after communication is stopped, the pin level is retained. To resume the operation, re-set serial output register m (SOm) (see **Figure 14-78 Procedure for Resuming UART Transmission**).

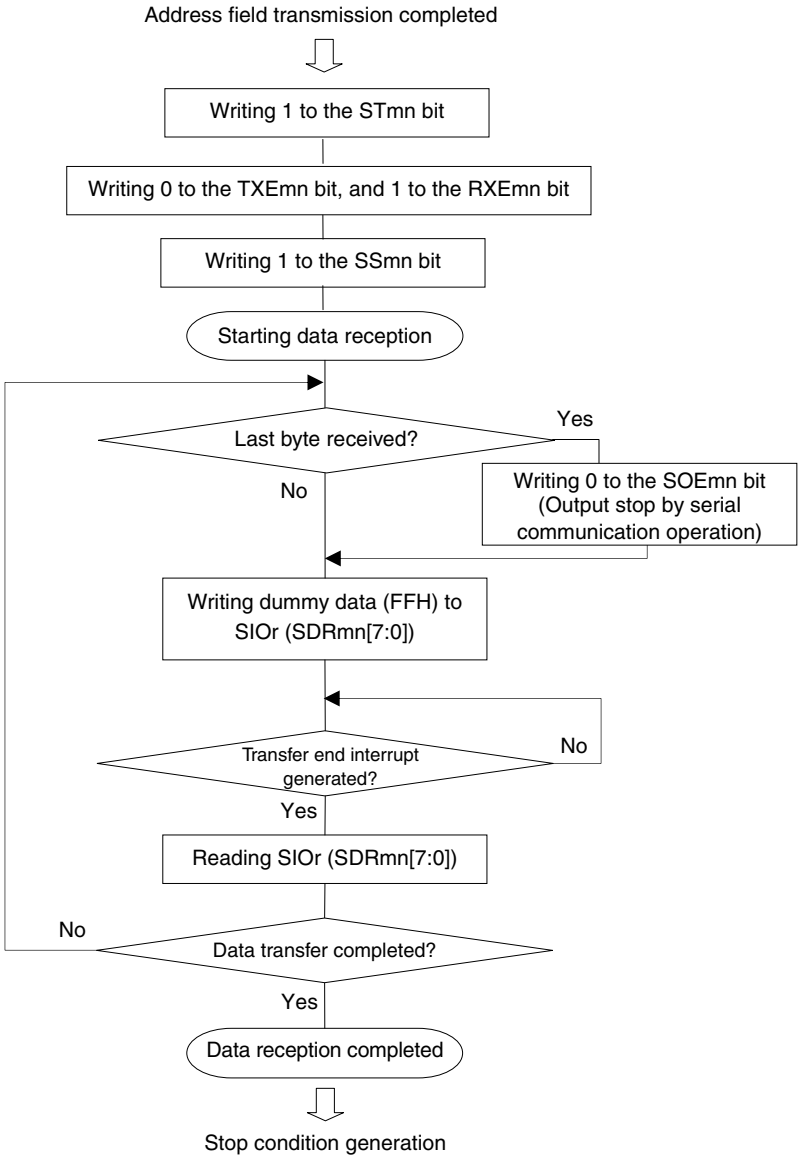
Figure 14-82. Flowchart of UART Transmission (in Continuous Transmission Mode)



Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more f_{CLK} clocks have elapsed.

Remark <1> to <6> in the figure correspond to <1> to <6> in **Figure 14-81 Timing Chart of UART Transmission (in Continuous Transmission Mode)**.

Figure 14-107. Flowchart of Data Reception



Caution ACK is not output when the last data is received (NACK). Communication is then completed by setting "1" to the STmn bit of serial channel stop register m (STm) to stop operation and generating a stop condition.

Table 14-17. Relationship between register settings and pins (Channel 0 of unit 2: CSI40, UART4 transmission)

(μPD78F1027, 78F1028, 78F1029, 78F1030 only)

SE 20 Note 1	MD 202	MD 201	SOE 20	SO 20	CKO 20	TXE 20	RXE 20	PM 50	P50	PM 51 Note 2	P51 Note 2	PM 52	P52	Operation mode	Pin Function		
															$\overline{\text{SCK40}}$/ INTP1/ P50	SI40/ RxD4/ INTP2/ P51 Note 2	SO40/ TxD4/ TO00/P52
0	0	0	0	1	1	0	0	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	× Note 3	Operation stop mode	INTP1/ P50	INTP2/ P51	TO00/P52
	0	1														INTP2/ P51/RxD4	
1	0	0	0	1	1	0	1	1	×	1	×	× Note 3	× Note 3	Slave CSI40 reception	$\overline{\text{SCK40}}$ (input)	SI40	TO00/P52
			1	0/1 Note 4	1	1	0	1	×	× Note 3	× Note 3	0	1	Slave CSI40 transmission	$\overline{\text{SCK40}}$ (input)	INTP2/P51	SO40
			1	0/1 Note 4	1	1	1	1	×	1	×	0	1	Slave CSI40 transmission/ reception	$\overline{\text{SCK40}}$ (input)	SI40	SO40
			0	1	0/1 Note 4	0	1	0	1	1	×	× Note 3	× Note 3	Master CSI40 reception	$\overline{\text{SCK40}}$ (output)	SI40	TO00/P52
			1	0/1 Note 4	0/1 Note 4	1	0	0	1	× Note 3	× Note 3	0	1	Master CSI40 transmission	$\overline{\text{SCK40}}$ (output)	INTP2/P51	SO40
			1	0/1 Note 4	0/1 Note 4	1	1	0	1	1	×	0	1	Master CSI40 transmission/ reception	$\overline{\text{SCK40}}$ (output)	SI40	SO40
	0	1	1	0/1 Note 4	1	1	0	× Note 3	× Note 3	× Note 3	× Note 3	0	1	UART4 transmission Note 5	INTP1/ P50	INTP2/ P51/RxD4	TxD4

Notes 1. Serial channel enable register 2 (SE2) is a read-only status register which is set using serial channel start register 2 (SS2) and serial channel stop register 2 (ST2).

2. When channel 1 of unit 2 is set to UART4 reception, this pin becomes an RxD4 function pin (refer to **Table 14-18**). In this case, operation stop mode or UART4 transmission must be selected for channel 0 of unit 2.

3. This pin can be set as a port function pin.

4. This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

5. When using UART4 transmission and reception in a pair, set channel 1 of unit 2 to UART4 reception (refer to **Table 14-18**).

Remark X: Don't care

Figure 15-7. Format of IICA Status Register (IICS) (3/3)

ACKD	Detection of acknowledge ($\overline{ACK}$)
0	Acknowledge was not detected.
1	Acknowledge was detected.

Condition for clearing (ACKD = 0)	Condition for setting (ACKD = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• After the SDA0 line is set to low level at the rising edge of SCL0 line's ninth clock

STD	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect.

Condition for clearing (STD = 0)	Condition for setting (STD = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LREL = 1 (exit from communications) • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When a start condition is detected

SPD	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPD = 0)	Condition for setting (SPD = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When the IICE bit changes from 1 to 0 (operation stop) • Reset	• When a stop condition is detected

Remark LREL: Bit 6 of IICA control register 0 (IICCTL0)
IICE: Bit 7 of IICA control register 0 (IICCTL0)

(4) IICA flag register (IICF)

This register sets the operation mode of I^2C and indicates the status of the I^2C bus.

The IICF register can be set by a 1-bit or 8-bit memory manipulation instruction. However, the STT clear flag (STCF) and I^2C bus status flag (IICBSY) bits are read-only.

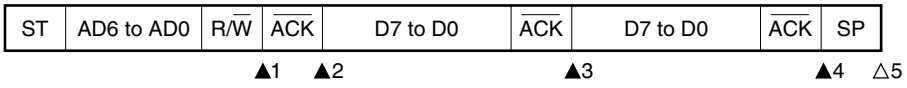
The IICRSV bit can be used to enable/disable the communication reservation function.

The STCEN bit can be used to set the initial value of the IICBSY bit.

The IICRSV and STCEN bits can be written only when the operation of I^2C is disabled (bit 7 (IICE) of IICA control register 0 (IICCTL0) = 0). When operation is enabled, the IICF register can be read.

Reset signal generation clears this register to 00H.

(ii) When WTIM = 1



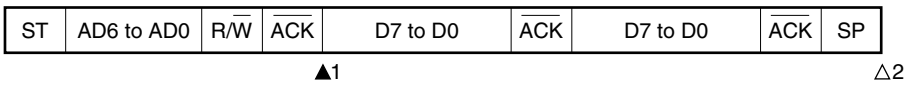
▲1: IICS = 0110×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(6) Operation when arbitration loss occurs (no communication after arbitration loss)

When the device is used as a master in a multi-master system, read the MSTS bit each time interrupt request signal INTIICA has occurred to check the arbitration result.

(a) When arbitration loss occurs during transmission of slave address data (when WTIM = 1)



▲1: IICS = 01000110B
△2: IICS = 00000001B

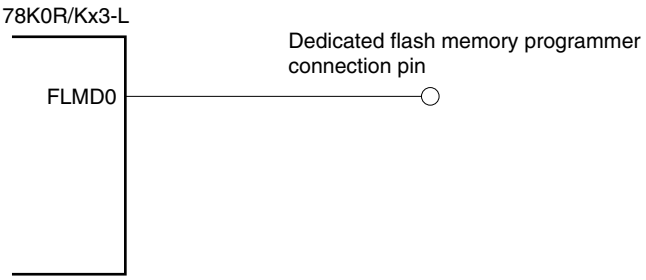
Remark ▲: Always generated
△: Generated only when SPIE = 1

(3) In self programming mode

It is recommended to leave this pin open when using the self programming function. To pull it down externally, use a resistor of 100 kΩ to 200 kΩ.

In the self programming mode, the setting is switched to pull up in the self programming library.

Figure 26-11. FLMD0 Pin Connection Example



26.4.2 TOOL0 pin

In the flash memory programming mode, connect this pin directly to the dedicated flash memory programmer or pull it up by connecting it to EV_{DD} via an external resistor.

When on-chip debugging is enabled in the normal operation mode, pull this pin up by connecting it to EV_{DD} via an external resistor, and be sure to keep inputting the V_{DD} level to the TOOL0 pin before reset is released (pulling down this pin is prohibited).

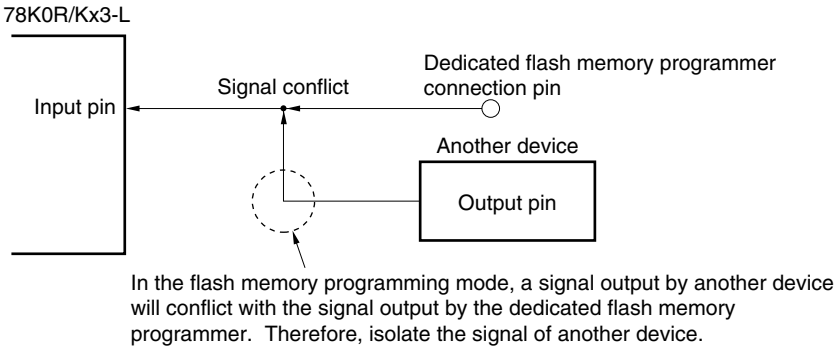
Remark The SAU and IICA pins are not used for communication between the 78K0R/Kx3-L and dedicated flash memory programmer, because single-line UART is used.

26.4.3 $\overline{\text{RESET}}$ pin

Signal conflict will occur if the reset signal of the dedicated flash memory programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board. To prevent this conflict, isolate the connection with the reset signal generator.

The flash memory will not be correctly programmed if the reset signal is input from the user system while the flash memory programming mode is set . Do not input any signal other than the reset signal of the dedicated flash memory programmer.

Figure 26-12. Signal Conflict ($\overline{\text{RESET}}$ Pin)



26.6.3 Selecting communication mode

Communication mode of the 78K0R/Kx3-L as follows.

Table 26-5. Communication Modes

Communication Mode	Standard Setting[Note 1]				Pins Used
	Port	Speed [Note 2]	Frequency	Multiply Rate	
1-line mode (dedicated single-line UART)	UART	115200 bps, 250000 bps, 500000 bps, 1 Mbps [Note 3]	–	–	TOOL0

Notes 1. Selection items for Standard settings on GUI of the flash memory programmer.

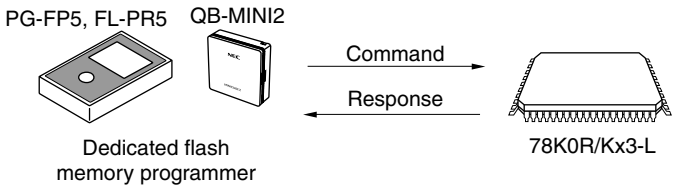
2. Because factors other than the baud rate error, such as the signal waveform slew, also affect UART communication, thoroughly evaluate the slew as well as the baud rate error.

3. When using a transfer rate of 1 Mbps, do not use the wide voltage mode.

26.6.4 Communication commands

The 78K0R/Kx3-L communicates with the dedicated flash memory programmer by using commands. The signals sent from the flash memory programmer to the 78K0R/Kx3-L are called commands, and the signals sent from the 78K0R/Kx3-L to the dedicated flash memory programmer are called response.

Figure 26-16. Communication Commands



The flash memory control commands of the 78K0R/Kx3-L are listed in the table below. All these commands are issued from the programmer and the 78K0R/Kx3-L perform processing corresponding to the respective commands.

Table 26-6. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Verify	Compares the contents of a specified area of the flash memory with data transmitted from the programmer.
Erase	Chip Erase	Erases the entire flash memory.
	Block Erase	Erases a specified area in the flash memory.
Blank check	Block Blank Check	Checks if a specified block in the flash memory has been correctly erased.
Write	Programming	Writes data to a specified area in the flash memory.
Getting information	Silicon Signature	Gets the 78K0R/Kx3-L information (such as the part number and flash memory configuration).
	Version Get	Gets the 78K0R/Kx3-L firmware version.
	Checksum	Gets the checksum data for a specified area.
Security	Security Set	Sets security information.
Others	Reset	Used to detect synchronization status of communication.
	Baud Rate Set	Sets baud rate when UART communication mode is selected.

The 78K0R/Kx3-L returns a response for the command issued by the dedicated flash memory programmer. The response names sent from the 78K0R/Kx3-L are listed below.

Table 26-7. Response Names

Response Name	Function
ACK	Acknowledges command/data.
NAK	Acknowledges illegal command/data.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, low	V_{IL1}	P01, P02, P12, P13, P15, P41, P45, P52, P56, P57, P80 to P87, P90, P91, P111, P123, P124, P144		0		0.3V_{DD}	V
	V_{IL2}	P00, P03 to P06, P10, P11, P14, P16, P17, P30, P31, P40, P42 to P44, P46, P47, P50, P51, P53 to P55, P64 to P67, P70 to P77, P110, P120 to P122, P131, P140 to P143, P145, EXCLK, $\overline{\text{RESET}}$	Normal input buffer	0		0.2V_{DD}	V
	V_{IL3}	P03, P04, P10, P11, P142, P143	TTL input buffer 4.0 V ≤ V_{DD} ≤ 5.5 V	0		0.8	V
			TTL input buffer 2.7 V ≤ V_{DD} < 4.0 V	0		0.5	V
			TTL input buffer 1.8 V ≤ V_{DD} < 2.7 V	0		0.2	V
	V_{IL4}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}	0		0.3AV_{REF}	V
	V_{IL5}	P60 to P63		0		0.3V_{DD}	V
	V_{IL6}	FLMD0 [Note]		0		0.1V_{DD}	V

Note When disabling writing of the flash memory, connect the FLMD0 pin processing directly to V_{SS}, and maintain a voltage less than 0.1V_{DD}.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Supply current	I_{DD2} Note 1	HALT mode	f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +50 °C	V_{DD} = 5.0 V		1.0	3.7	μA
				V_{DD} = 3.0 V		1.0	3.7	μA
				V_{DD} = 2.0 V		1.0	3.7	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +70 °C	V_{DD} = 5.0 V		1.0	6.1	μA
				V_{DD} = 3.0 V		1.0	6.1	μA
				V_{DD} = 2.0 V		1.0	6.1	μA
			f_{SUB} = 32.768 kHz Note 2, T_A = –40 to +85 °C	V_{DD} = 5.0 V		1.0	8.9	μA
				V_{DD} = 3.0 V		1.0	8.9	μA
				V_{DD} = 2.0 V		1.0	8.9	μA
	I_{DD3} Note 3	STOP mode	T_A = –40 to +50 °C			0.37	2.8	μA
			T_A = –40 to +70 °C			0.37	5.2	μA
			T_A = –40 to +85 °C			0.37	7.9	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value include the peripheral operation current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. During HALT instruction execution by flash memory.

2. When operating real-time counter (RTC) and setting ultra-low current consumption (AMPHS1 (bit2 of CMC register) = 1, OSMC = 82H). When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped. When watchdog timer is stopped. When RTCLPC = 1 (stops supply of subsystem clock to peripheral functions other than real-time counter). When output function of RTC is stopped.

3. Total current flowing into V_{DD}, EV_{DD0}, EV_{DD1}, and AV_{REF}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The maximum value includes the peripheral operation current and STOP leakage current. However, not including the current flowing into the A/D converter, LVI circuit, I/O port, and on-chip pull-up/pull-down resistors. When subsystem clock is stopped. When watchdog timer is stopped.

Remarks 1. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

2. RTCLPC: bit 7 of the operation speed mode control register (OSMC)

3. Temperature condition of the TYP. value is T_A = 25°C