Renesas Electronics America Inc - UPD78F1010GK-GAK-AX Datasheet

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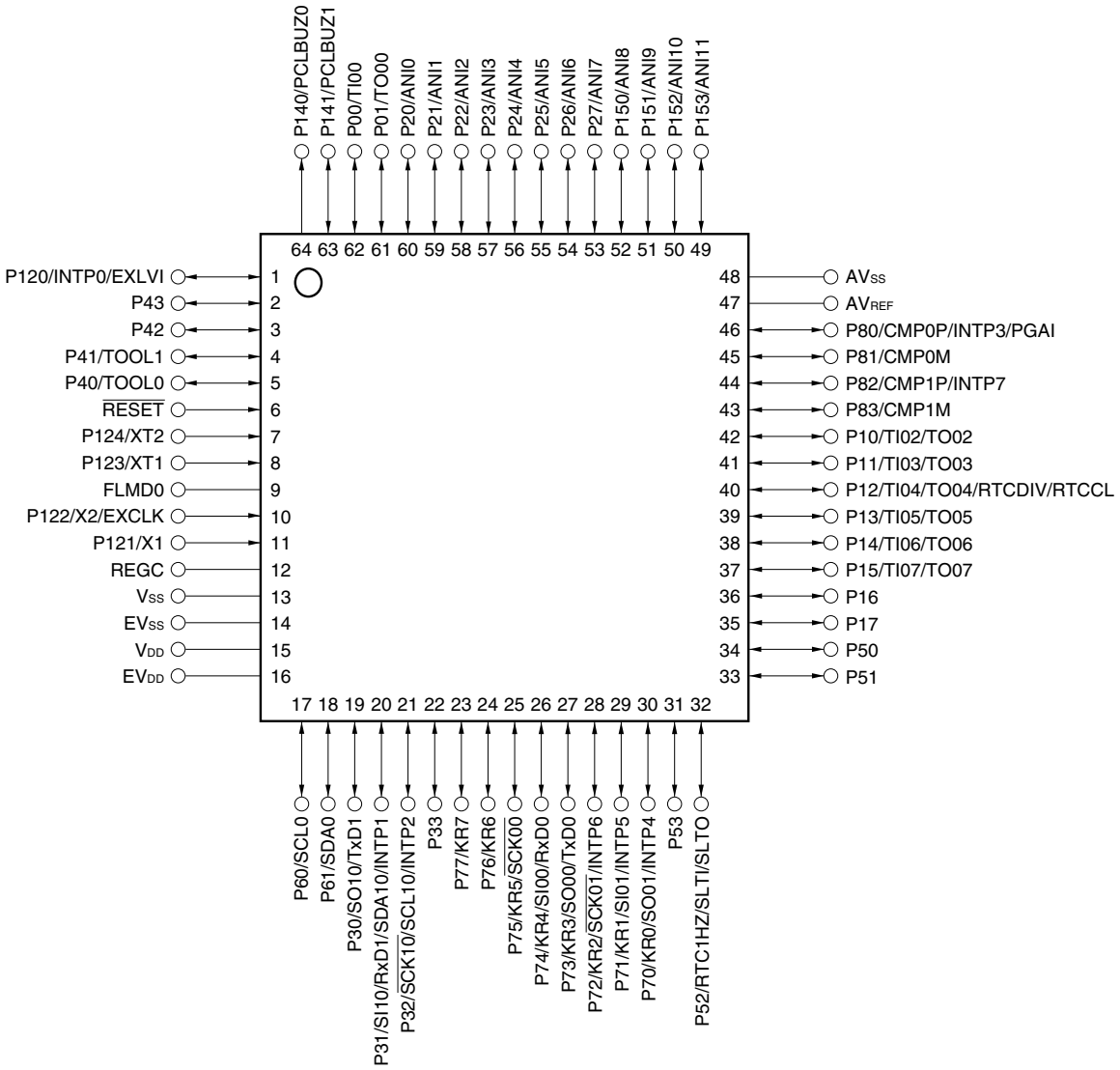
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	66
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1010gk-gak-ax

1.4.3 78K0R/KE3-L

- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)
- 64-pin plastic TQFP (fine pitch) (7 × 7)



Cautions 1. Make AVSS and EVSS the same potential as VSS.

2. Make EVDD the same potential as VDD.

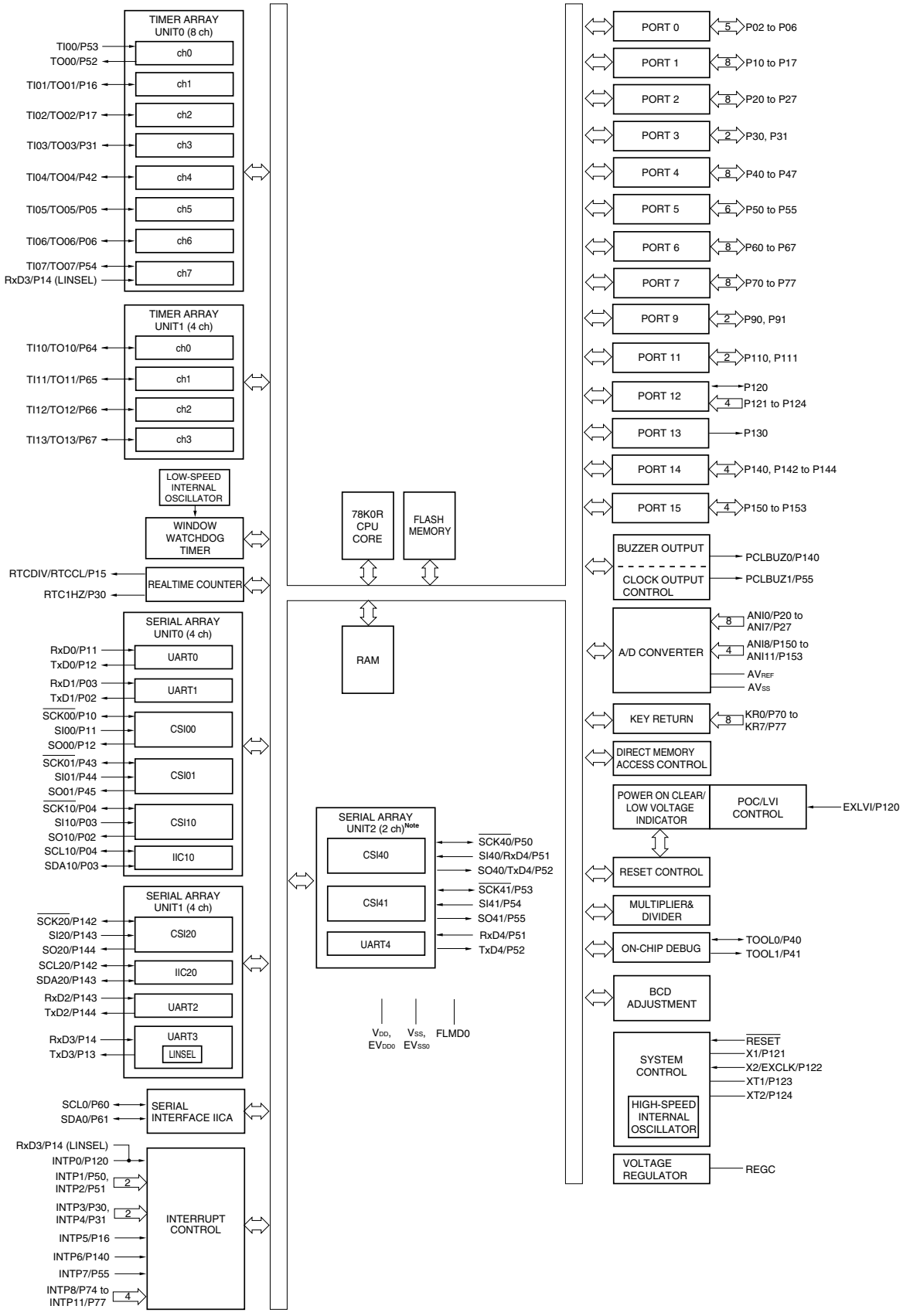
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

4. P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 are set as analog inputs in the order of P153/ANI11, …, P150/ANI8, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P150/ANI8 to P153/ANI11 as analog inputs, start designing from P153/ANI11 (see 13.3 (6) A/D port configuration register (ADPC) for details).

Remarks 1. For pin identification, see **1.5 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD pins and connect the VSS and EVSS pins to separate ground lines.

1.6.4 78K0R/KF3-L



Note Serial array unit 2 is only mounted in the μPD78F1027 and 78F1028.

2.1.2 78K0R/KC3-L (44-pin and 48-pin products)

(1) Port functions (1/2): 78K0R/KC3-L (44-pin and 48-pin products)

Function Name	I/O	Function	After Reset	Alternate Function
P10	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04/ RTCDIV/RTCCL
P13				TI05/TO05
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/ INTP1
P32				$\overline{SCK10}$/SCL10/ INTP2
P40 Note 1	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P50	I/O	Port 5. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06
P51				TI07/TO07
P52				RTC1HZ/SLTI/ SLTO
P60 Note 2	I/O	Port 6. 2-bit I/O port. Output of P60 and P61 is N-ch open-drain output (6 V tolerance). Input/output can be specified in 1-bit units.	Input port	SCL0 Note 2
P61 Note 2				SDA0 Note 2
P70	I/O	Port 7. 6-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{SCK01}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{SCK00}$

Notes 1. If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

2. 48-pin products only.

(2) Non-port functions (3/3) : 78K0R/KF3-L

Function Name	I/O	Function	After Reset	Alternate Function
TxD0	Output	Serial data output from UART0	Input port	P12/SO00
TxD1		Serial data output from UART1		P02/SO10
TxD2		Serial data output from UART2		P144/SO20
TxD3		Serial data output from UART3		P13
TxD4[Note]		Serial data output from UART4		P52/SO40[Note]/TO00
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
EXCLK	Input	External clock input for main system clock	Input port	P122/X2
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
V_{DD}	–	Positive power supply (P121 to P124 and other than ports (excluding $\overline{\text{RESET}}$ and FLMD0 pins))	–	–
EV_{DD0}	–	Positive power supply for ports (other than P20 to P27, P121 to P124, P150 to P153), and $\overline{\text{RESET}}$ and FLMD0 pins	–	–
AV_{REF}	–	• A/D converter reference voltage input • Positive power supply for P20 to P27, P150 to P153, and A/D converter	–	–
V_{SS}	–	Ground potential (P121 to P124 and other than ports (excluding $\overline{\text{RESET}}$ and FLMD0 pins))	–	–
EV_{SS0}	–	Ground potential for ports (other than P20 to P27, P121 to P124, and P150 to P153), and $\overline{\text{RESET}}$ and FLMD0 pins	–	–
AV_{SS}	–	Ground potential for A/D converter, P20 to P27, and P150 to P153. Use this pin with the same potential as EV_{SS0} and V_{SS}.	–	–
FLMD0	–	Flash memory programming mode setting	–	–
TOOL0	I/O	Data I/O for flash memory programmer/debugger	Input port	P40
TOOL1	Output	Clock output for debugger	Input port	P41

Note SO40 and RxD4 are only mounted in the μPD78F1027 and 78F1028.

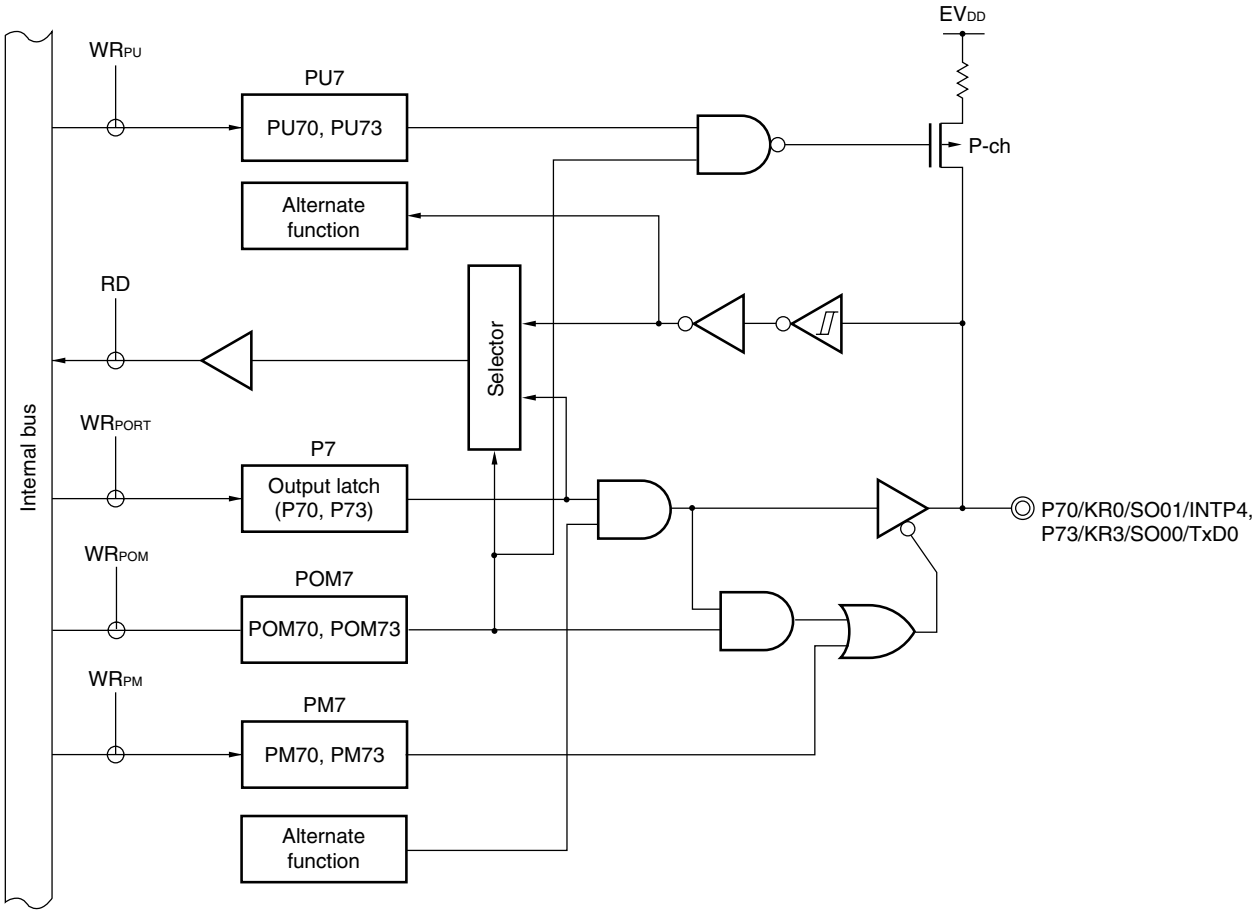
Table 4-6. Extended SFR (2nd SFR) List (8/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F0218H	Serial output register 2	SO2		R/W	–	–	√	0303H	–	–	–	–	–	Note	Note
F0219H									–	–	–	–	–	Note	Note
F021AH	Serial output enable register 2	SOE2L	SOE2	R/W	√	√	√	0000H	–	–	–	–	–	Note	Note
F021BH		–			–	–			–	–	–	–	–	Note	Note
F0220H	Serial output level register 2	SOL2L	SOL2	R/W	√	√	√	0000H	–	–	–	–	–	Note	Note
F0221H		–			–	–			–	–	–	–	–	Note	Note
F0230H	IICA control register 0	IICCTL0		R/W	√	√	–	00H	–	–	√	√	√	√	√
F0231H	IICA control register 1	IICCTL1		R/W	√	√	–	00H	–	–	√	√	√	√	√
F0232H	IICA low-level width setting register	IICWL		R/W	–	√	–	FFH	–	–	√	√	√	√	√
F0233H	IICA high-level width setting register	IICWH		R/W	–	√	–	FFH	–	–	√	√	√	√	√
F0234H	Slave address register	SVA		R/W	–	√	–	00H	–	√	√	√	√	√	√
F0240H	Programmable gain amplifier control register	OAM		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0241H	Comparator 0 control register	C0CTL		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0242H	Comparator 0 internal reference voltage setting register	C0RVM		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0243H	Comparator 1 control register	C1CTL		R/W	√	√	–	00H	√	√	√	√	√	–	–
F0244H	Comparator 1 internal reference voltage setting register	C1RVM		R/W	√	√	–	00H	√	√	√	√	√	–	–

Note Those are only mounted in the 78K0R/KF3-L (μ PD78F1027 and 78F1028) and the 78K0R/KG3-L (μ PD78F1029 and 78F1030).

Remark For SFRs in the SFR area, see **Table 4-5 SFR List**.

Figure 5-15. Block Diagram of P70 and P73



P7: Port register 7
PU7: Pull-up resistor option register 7
POM7: Port output mode register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

Remark With products not provided with an EV_{DD} or EV_{SS} pin, replace EV_{DD} with V_{DD}, or replace EV_{SS} with V_{SS}.

5.2.12 Port 15

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P150/ANI8	√		√	√	√
P151/ANI9	√		√	√	√
P152/ANI10	–		√	√	√
P153/ANI11	–		–	–	√

Remark √: Mounted

Port 15 is an I/O port with an output latch. Port 15 can be set to the input mode or output mode in 1-bit units using port mode register 15 (PM15).

This port can also be used for A/D converter analog input.

To use P150/ANI8 to P153/ANI11 as digital input pins, set them in the digital I/O mode by using the A/D port configuration register (ADPC) and in the input mode by using the PM15 register. Use these pins starting from the lower bit.

To use P150/ANI8 to P153/ANI11 as digital output pins, set them in the digital I/O mode by using the ADPC register and in the output mode by using the PM15 register.

Table 5-6. Setting Functions of P150/ANI8 to P153/ANI11 Pins

ADPC Register	PM15 Register	ADS Register	P150/ANI8 to P153/ANI11 Pins
Digital I/O selection	Input mode	–	Digital input
	Output mode	–	Digital output
Analog input selection	Input mode	Selects ANI.	Analog input (to be converted)
		Does not select ANI.	Analog input (not to be converted)
	Output mode	Selects ANI.	Setting prohibited
		Does not select ANI.	

All P150/ANI8 to P153/ANI11 are set in the digital input mode when the reset signal is generated.

Figure 5-27 shows block diagram of port 15.

Caution Make the AV_{REF} pin the same potential as the V_{DD} pin when port 15 is used as a digital port.

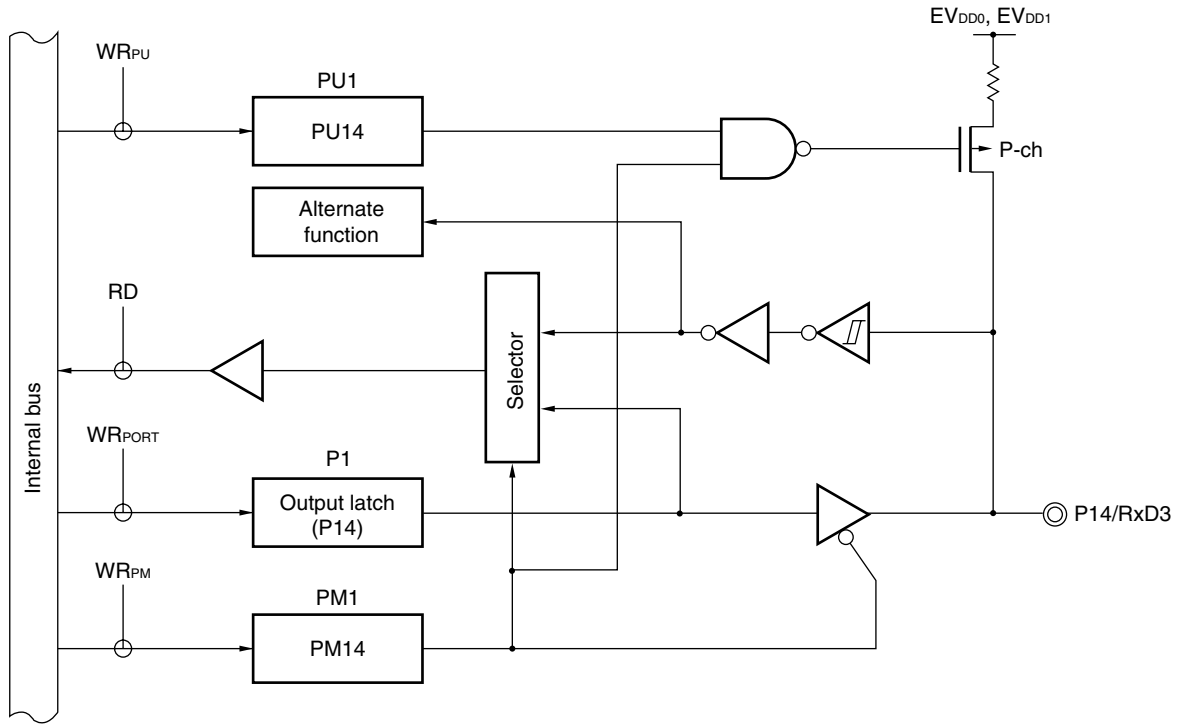
Figure 5-34. Format of Port Register (78K0R/KD3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P0	0	0	0	0	0	0	P01	P00	FFF00H	00H (output latch)	R/W
P1	0	0	0	0	P13	P12	P11	P10	FFF01H	00H (output latch)	R/W
P2	P27	P26	P25	P24	P23	P22	P21	P20	FFF02H	00H (output latch)	R/W
P3	0	0	0	0	0	P32	P31	P30	FFF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	P41	P40	FFF04H	00H (output latch)	R/W
P5	0	0	0	0	0	P52	P51	P50	FFF05H	00H (output latch)	R/W
P6	0	0	0	0	0	0	P61	P60	FFF06H	00H (output latch)	R/W
P7	P77	P76	P75	P74	P73	P72	P71	P70	FFF07H	00H (output latch)	R/W
P8	0	0	0	0	P83	P82	P81	P80	FFF08H	00H (output latch)	R/W
P12	0	0	0	P124	P123	P122	P121	P120	FFF0CH	Undefined	R/W[Note]
P14	0	0	0	0	0	0	0	P140	FFF0EH	00H (output latch)	R/W
P15	0	0	0	0	0	P152	P151	P150	FFF0FH	00H (output latch)	R/W

Pmn	m = 0 to 8, 12, 14, 15 ; n = 0 to 7	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

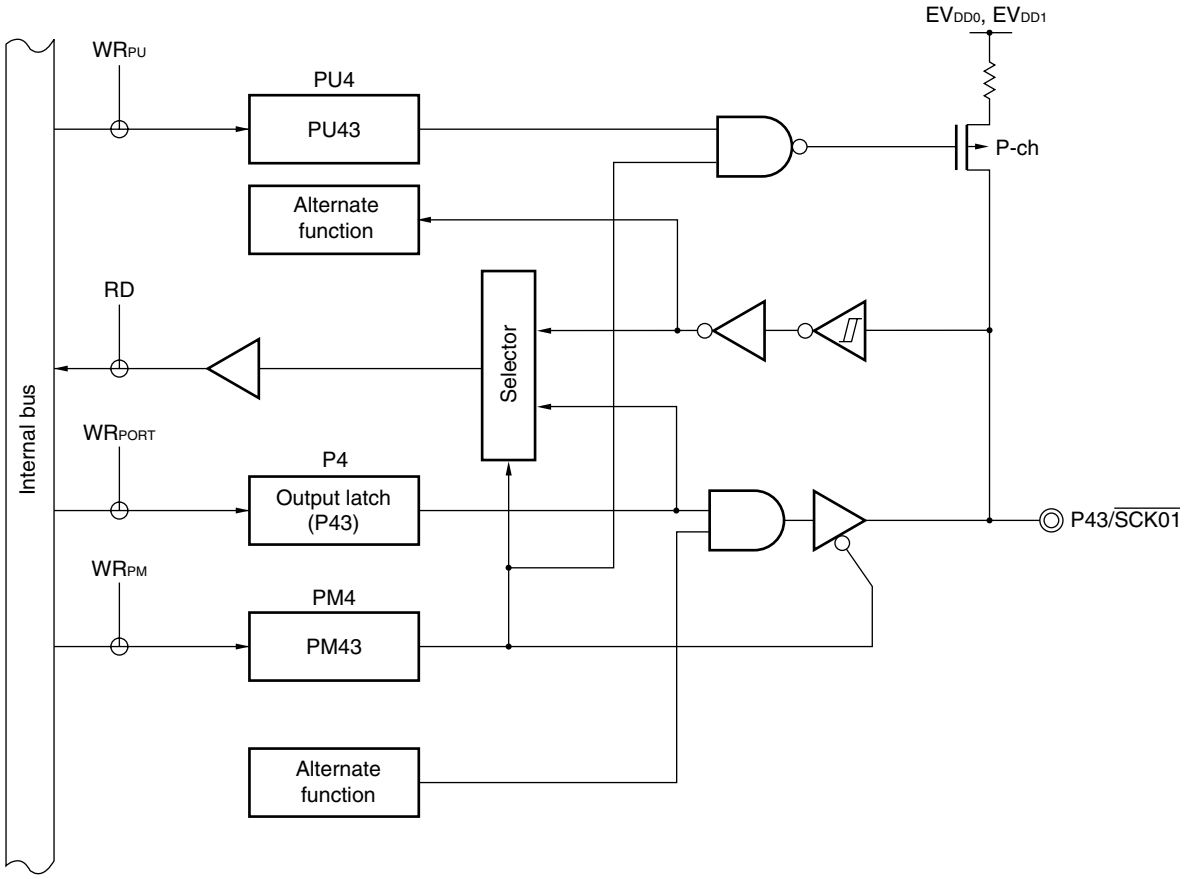
Note P121 to P124 are read-only.

Figure 6-10. Block Diagram of P14



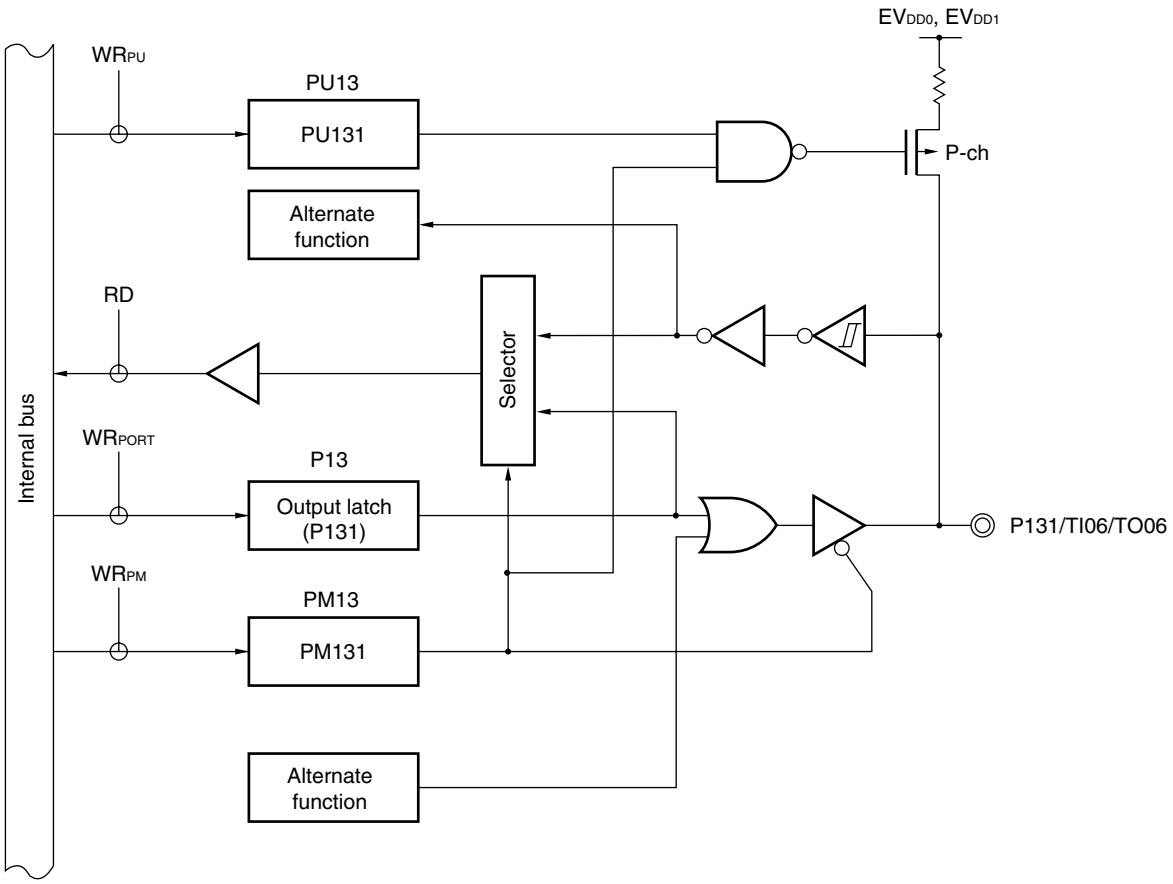
P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 6-18. Block Diagram of P43



P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

Figure 6-46. Block Diagram of P131



P13: Port register 13
PU13: Pull-up resistor option register 13
PM13: Port mode register 13
RD: Read signal
WR××: Write signal

(7) Timer channel stop register m (TTm)

The TTm register is a trigger register that is used to clear timer/counter register mn (TCRmn) and start the counting operation of each channel.

When a bit (TTmn) of this register is set to 1, the corresponding bit (TEmn) of timer channel enable status register m (TEm) is cleared to 0. The TTmn bit is immediately cleared when operation is stopped (TEmn = 0), because it is a trigger bit.

The TTm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TTm register can be set with a 1-bit or 8-bit memory manipulation instruction with TTmL.

Reset signal generation clears this register to 0000H.

Figure 8-20. Format of Timer Channel Stop register m (TTm)

Address: F01B4H, F01B5H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT0	0	0	0	0	0	0	0	0	TT07	TT06	TT05	TT04	TT03	TT02	TT01	TT00

Address: F01DCH, F01DDH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TT1	0	0	0	0	0	0	0	0	0	0	0	0	TT13	TT12	TT11	TT10

TTmn	Operation stop trigger of channel n
0	No trigger operation
1	Operation is stopped (stop trigger is generated).

Caution Be sure to clear bits 15 to 8 of the TT0 register and bits 15 to 4 of the TT1 register to "0".

Remarks 1. When the TTm register is read, 0 is always read.

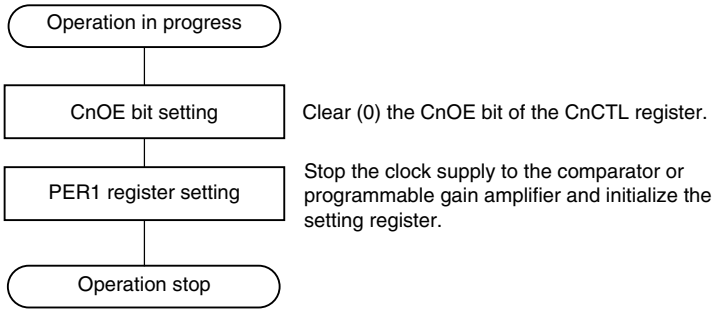
2. m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

10.4.2 Stopping comparator and programmable gain amplifier operation

The procedures for stopping the operation of a comparator and a programmable gain amplifier are described below, separately for each use method.

- ○ Using only a comparator (Figure 10-14)
- ○ Using the programmable gain amplifier output voltage as the comparator compare voltage input (Figure 10-15)
- ○ Using the programmable gain amplifier output voltage as the A/D converter analog input (Figure 10-16)

Figure 10-14. Using Only a Comparator



Remark n = 0 and 1 (78K0R/KC3-L (40-pin): n = 0).

(7) Port input mode register 8 (PIM8) (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only)

This register enables or disables the digital input of port 8 in 1-bit units.

Disable the digital input (used as analog input) to use the PGAI pin as the analog input. Enable the digital input to use the port function, or the external interrupt and timer Hi-Z control functions, because the digital input is disabled (used as analog input) in the initial state.

The PIM8 register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Figure 13-10. Format of Port Input Mode Register 8 (PIM8)

Address: F0048H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PIM8	0	0	0	0	PIM83	PIM82 Note	PIM81	PIM80

PIM8n	Selection of enabling or disabling P8n pin digital input (n = 0 to 3)
0	Disables digital input (used as analog input)
1	Enables digital input

Note PIM82 bit is not provided in the 78K0R/KC3-L (40-pin).

14.2 Configuration of Serial Array Unit

The serial array unit includes the following hardware.

Table 14-1. Configuration of Serial Array Unit (1/2) (78K0R/KC3-L, KD3-L, KE3-L)

Item	Configuration
	78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L
Shift register	8 bits
Buffer register	Lower 8 bits of serial data register mn (SDRmn)[Note]
Serial clock I/O	$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$ pins (for 3-wire serial I/O), SCL10 pin (for simplified I^2C)
Serial data input	SI00, SI01, SI10 pins (for 3-wire serial I/O), RxD0 pin (for UART supporting LIN-bus), RxD1 pin (for UART)
Serial data output	SO00, SO01, SO10 pins (for 3-wire serial I/O), TxD0 pin (for UART supporting LIN-bus), TxD1 pin (for UART), output controller
Serial data I/O	SDA10 pin (for simplified I^2C)
Control registers	<Registers of unit setting block> • Peripheral enable register 0 (PER0) • Serial clock select register 0 (SPS0) • Serial channel enable status register 0 (SE0) • Serial channel start register 0 (SS0) • Serial channel stop register 0 (ST0) • Serial output enable register 0 (SOE0) • Serial output register 0 (SO0) • Serial output level register 0 (SOL0) • Input switch control register (ISC) • Noise filter enable register 0 (NFEN0)
	<Registers of each channel> • Serial data register 0n (SDR0n) • Serial mode register 0n (SMR0n) • Serial communication operation setting register 0n (SCR0n) • Serial status register 0n (SSR0n) • Serial flag clear trigger register 0n (SIR0n)
	• Port input mode registers 3, 7 (PIM3, PIM7) • Port output mode registers 3, 7 (POM3, POM7) • Port mode registers 3, 7 (PM3, PM7) • Port registers 3, 7 (P3, P7)

Note The lower 8 bits of serial data register 0n (SDR0n) can be read or written as the following SFR, depending on the communication mode.

- CSIp communication … SIOp (CSIp data register)
- UARTq reception … RXDq (UARTq receive data register)
- UARTq transmission … TXDq (UARTq transmit data register)
- IIC10 communication … SIO10 (IIC10 data register)

Remark n: Channel number (n = 0 to 3), p: CSI number (p = 00, 01, 10),
q: UART number (q = 0, 1)

The meanings of <3> to <10> in (2) Address ~ data ~ data in Figure 15-32 are explained below.

<R> <3> In the slave device if the address received matches the address (SVA value) of a slave device[Note], that slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<R> <4> The master device issues an interrupt (INTIICA: end of address transmission) at the falling edge of the 9th clock. The slave device whose address matched the transmitted slave address sets a wait status (SCL0 = 0) and issues an interrupt (INTIICA: address match)[Note].

<5> The master device writes the data to transmit to the IICA shift register (IICA) and releases the wait status that it set by the master device.

<6> If the slave device releases the wait status (WREL = 1), the master device starts transferring data to the slave device.

<R> <7> After data transfer is completed, because of ACKE = 1, the slave device sends an ACK by hardware to the master device. The ACK is detected by the master device (ACKD = 1) at the rising edge of the 9th clock.

<8> The master device and slave device set a wait status (SCL0 = 0) at the falling edge of the 9th clock, and both the master device and slave device issue an interrupt (INTIICA: end of transfer).

<9> The master device writes the data to transmit to the IICA register and releases the wait status that it set by the master device.

<10> The slave device reads the received data and releases the wait status (WREL = 1). The master device then starts transferring data to the slave device.

Note If the transmitted address does not match the address of the slave device, the slave device does not return an ACK to the master device (NACK: SDA0 = 1). The slave device also does not issue the INTIICA interrupt (address match) and does not set a wait status. The master device, however, issues the INTIICA interrupt (end of address transmission) regardless of whether it receives an ACK or NACK.

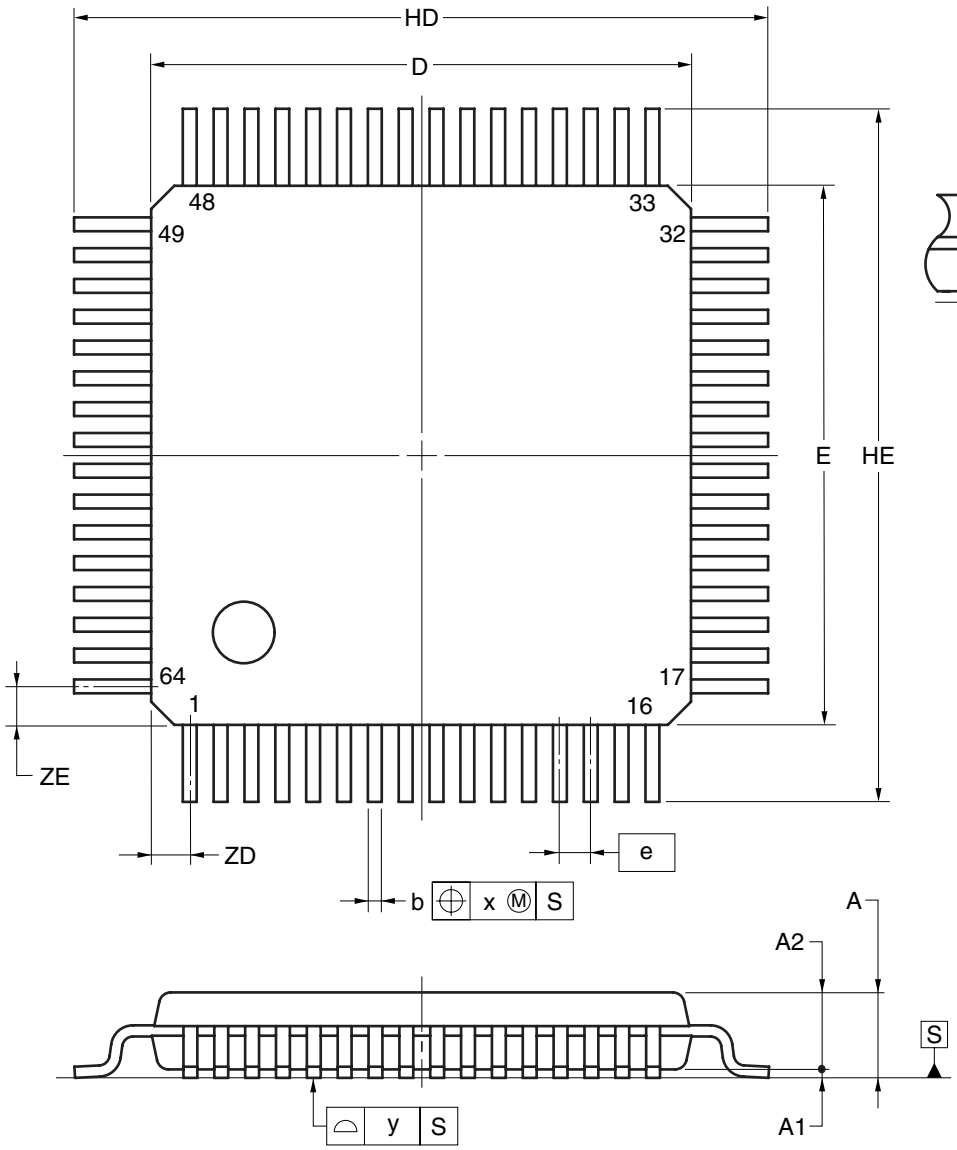
Remark <1> to <15> in Figure 15-32 represent the entire procedure for communicating data using the I^2C bus. Figure 15-32 (1) Start condition ~ address ~ data shows the processing from <1> to <6>, Figure 15-32 (2) Address ~ data ~ data shows the processing from <3> to <10>, and Figure 15-32 (3) Data ~ data ~ stop condition shows the processing from <7> to <15>.

30.1.2 Non-port functions

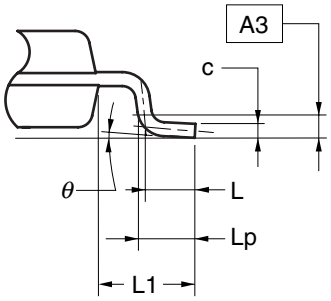
Function Name		78K0R/KC3-L			78K0R/KD3-L	78K0R/KE3-L
		40-pin	44-pin	48-pin	52-pin	64-pin
Power supply, ground		V_{DD}, AV_{REF}, V_{SS}, AV_{SS}				V_{DD}, EV_{DD}, AV_{REF}, V_{SS}, EV_{SS}, AV_{SS}
Regulator		REGC				
Reset		$\overline{\text{RESET}}$				
Clock oscillation		X1, X2, EXCLK	X1, X2, XT1, XT2, EXCLK			
Writing to flash memory		FLMD0				
Interrupt		INTP0 to INTP6	INTP0 to INTP7			
Timer		TI02 to TI07, TO02-TO07	SLTI, SLTO, TI02 to TI07, TO02 to TO07		SLTI, SLTO, TI00, TI02 to TI07, TO00, TO02 to TO07	
Real time counter		–	RTCDIV, RTCCL, RTC1HZ			
Comparator		CMP0M, CMP0P, CMP1M	CMP0M, CMP0P, CMP1M, CMP1P			
Programmable gain amplifier		PGAI				
Serial interface	UART0	RxD0, TxD0				
	UART1	RxD1, TxD1				
	CSI00	SCK00, SI00, SO00				
	CSI01	SCK01, SI01, SO01				
	CSI10	SCK10, SI10, SO10				
	IIC10	SCL10, SDA10				
	IICA	–		SCL0, SDA0		
A/D converter		ANI0 to ANI9		ANI0 to ANI10		ANI0 to ANI11
Clock Output/Buzzer Output		–		PCLBUZ0		PCLBUZ0, PCLBUZ1
Key Interrupt		KR0 to KR5			KR0 to KR7	
Low-voltage detector (LVI)		EXLVI				
On-chip debug function		TOOL0, TOOL1				

μPD78F1007GA-HAB-AX, 78F1008GA-HAB-AX, 78F1009GA-HAB-AX

64-PIN PLASTIC TQFP (FINE PITCH) (7x7)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.20 MAX.
A1	0.10±0.05
A2	1.00±0.05
A3	0.25
b	$0.16^{+0.07}_{-0.03}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.40
x	0.07
y	0.08
ZD	0.50
ZE	0.50

P64GA-40-HAB

NOTE
Each lead centerline is located within 0.07mm of its true position at maximum material condition.

A.1 Software Package

SP78K0R 78K0R Series software package	Development tools (software) common to the 78K0R microcontrollers are combined in this package.
	Part number: μS××××SP78K0R

Remark ×××× in the part number differs depending on the host machine and OS used.

μS××××SP78K0R

××××	Host Machine	OS	Supply Medium
AB17	PC-9800 series, IBM PC/AT compatibles	Windows (Japanese version)	CD-ROM
BB17		Windows (English version)	

A.2 Language Processing Software

RA78K0R Assembler package	This assembler converts programs written in mnemonics into object codes executable with a microcontroller. This assembler is also provided with functions capable of automatically creating symbol tables and branch instruction optimization. This assembler should be used in combination with a device file (DF781014/DF781030[Note1]). **<Precaution when using RA78K0R in PC environment>** This assembler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××RA78K0R
CC78K0R C compiler package	This compiler converts programs written in C language into object codes executable with a microcontroller. This compiler should be used in combination with an assembler package and device file (both sold separately). **<Precaution when using CC78K0R in PC environment>** This C compiler package is a DOS-based application. It can also be used in Windows, however, by using the Project Manager (included in assembler package) on Windows.
	Part number: μS××××CC78K0R
DF781014/DF781030[Notes 1, 2] Device file	This file contains information peculiar to the device. This device file should be used in combination with a tool (RA78K0R, CC78K0R, SM+ for 78K0R, and ID78K0R-QB) (all sold separately). The corresponding OS and host machine differ depending on the tool to be used.
	Part number: μS××××DF781014, μS××××DF781030

Notes 1. 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L, 78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012),
78K0R/KG3-L (μ PD78F1013, 78F1014) : DF781014
78K0R/KF3-L (μ PD78F1027, 78F1028),
78K0R/KG3-L (μ PD78F1029, 78F1030) : DF781030

2. The DF781014 and DF781030 can be used in common with the RA78K0R, CC78K0R, SM+ for 78K0R, and ID78K0R-QB. Download the DF781009 and DF781014 from the download site for development tools (http://www2.renesas.com/micro/en/ods/).