# Renesas Electronics America Inc - UPD78F1012GC-GAD-AX Datasheet

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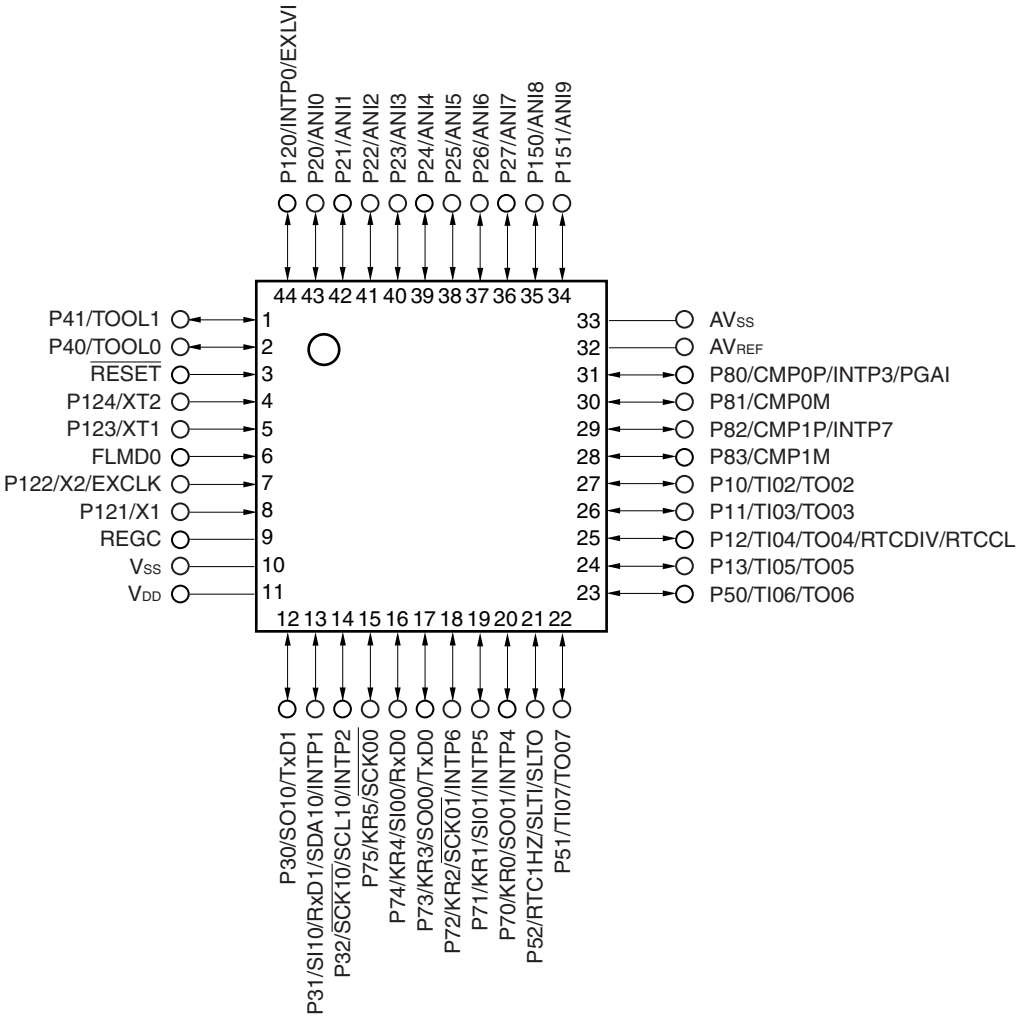
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0R |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | 3-Wire SIO, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 66 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 12x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1012gc-gad-ax |

- 44-pin plastic LQFP (10 × 10)



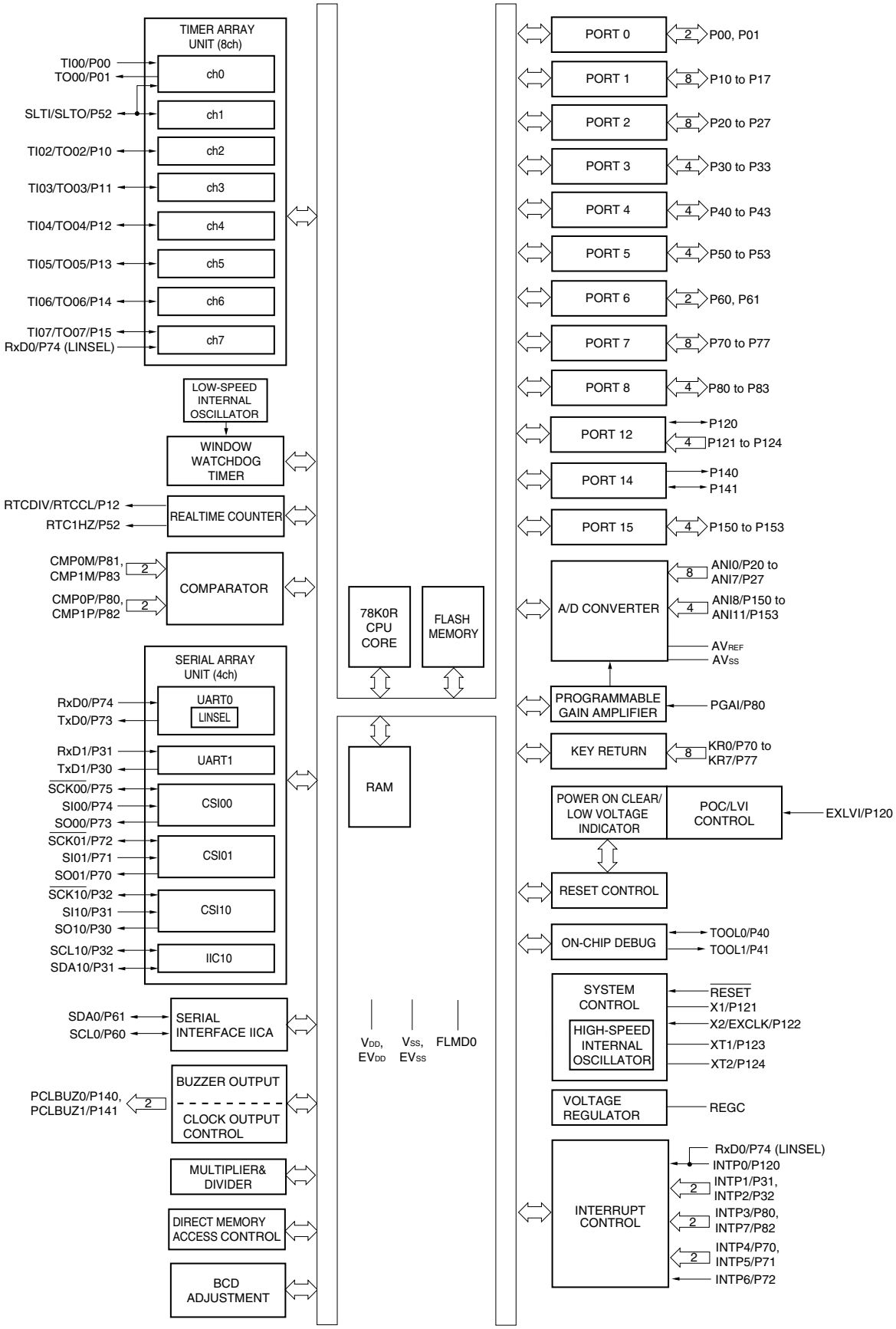

**Cautions 1. Make AVSS the same potential as VSS.**

**2. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**3. P20/ANI0 to P27/ANI7 and P151/ANI9 are set as analog inputs in the order of P151/ANI9, …, P27/ANI7, …, P20/ANI0 by the A/D port configuration register (ADPC). When using P20/ANI0 to P27/ANI7 and P151/ANI9 as analog inputs, start designing from P151/ANI9 (see 13.3 (6) A/D port configuration register (ADPC) for details).**

**Remark** For pin identification, see **1.5 Pin Identification**.

### 1.6.3 78K0R/KE3-L



## 2.2 Description of Pin Functions

**Remark** The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **2.1 Pin Function List**.

### 2.2.1 P00, P01 (port 0)

P00 and P01 function as an I/O port. These pins also function as timer I/O.

| | 78K0R/KC3-L (μPD78F100y: y = 0 to 3) | | 78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3) | 78K0R/KD3-L (μPD78F100y: y = 4 to 6) | 78K0R/KE3-L (μPD78F100y: y = 7 to 9) |
|---|---|---|---|---|---|
| | 40-pin | 44-pin | | | |
| P00/ TI00 | – | | – | √ | √ |
| P11/TO00 | – | | – | √ | √ |

**Remark** √: Mounted

The following operation modes can be specified in 1-bit units.

**(1) Port mode**

P00 and P01 function as an I/O port. P00 and P01 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

**(2) Control mode**

P00 and P01 function as timer I/O.

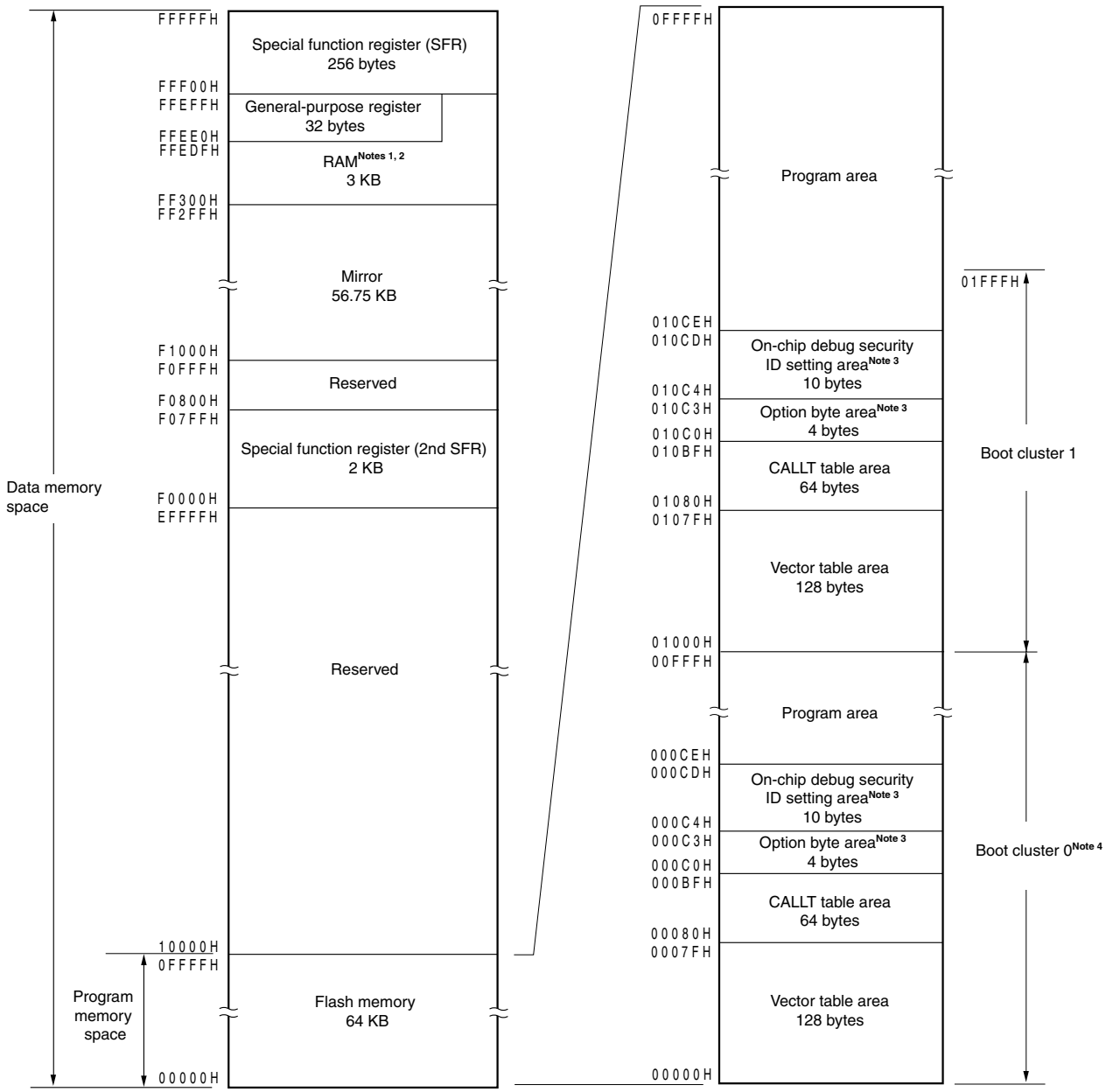
**(a) TI00**

This is the pin for inputting an external count clock/capture trigger to 16-bit timer 00.

**(b) TO00**

This is the timer output pin of 16-bit timer 00.

**Figure 4-4. Memory Map (μPD78F1003, 78F1006, 78F1009)**




**Notes 1.** While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009.

**2.** Instructions can be executed from the RAM area excluding the general-purpose register area.

**3.** When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

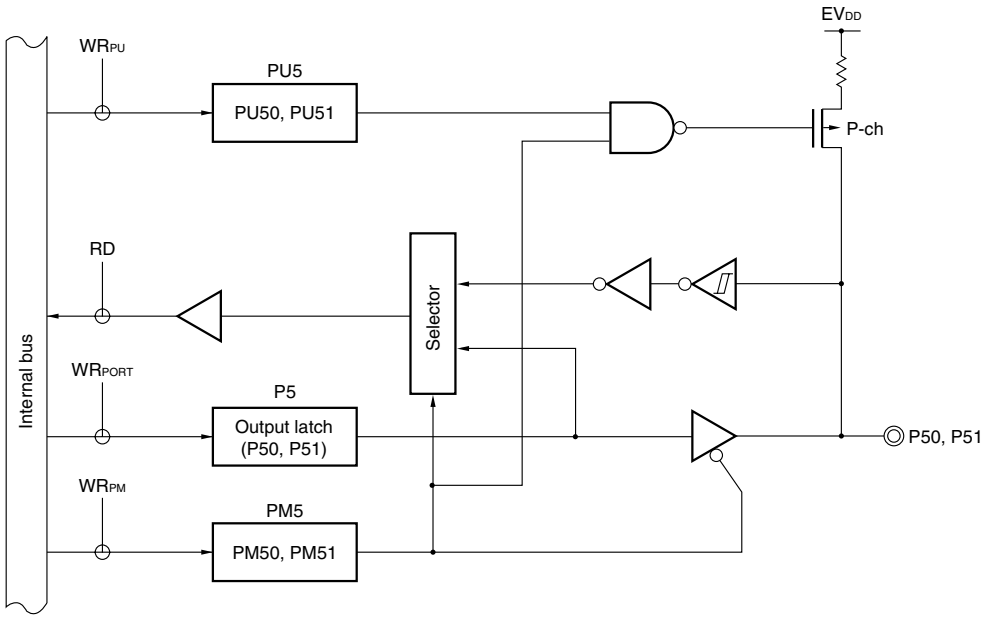
**4.** Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

**Table 4-3. Vector Table (1/2)**

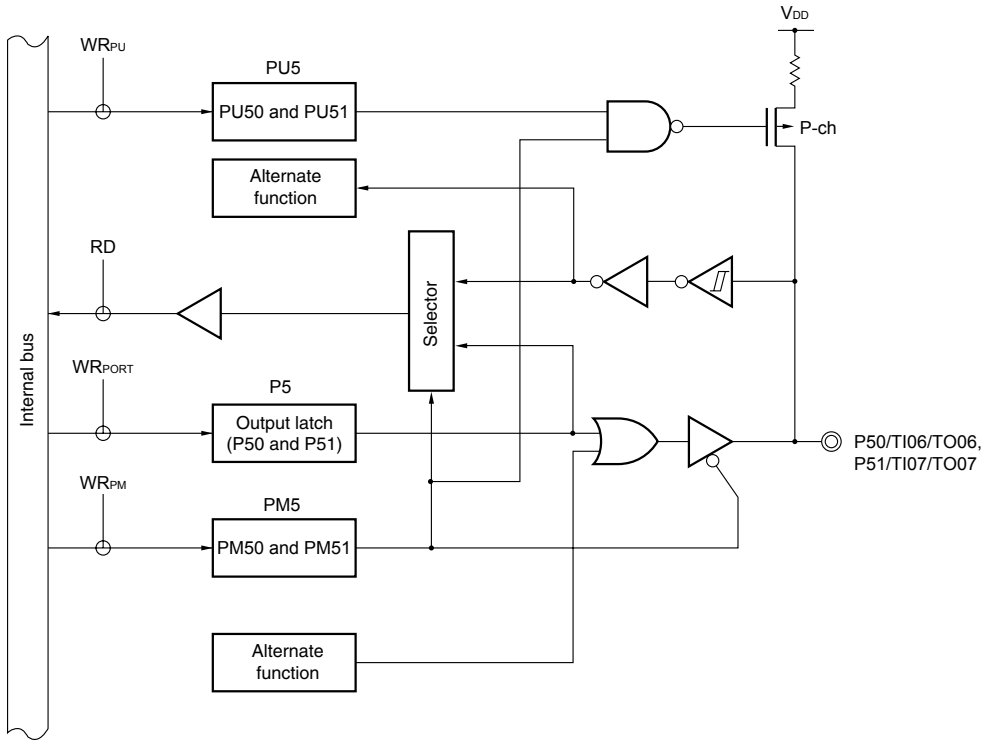
| Vector Table Address | Interrupt Source | KC3-L (40pin) | KC3-L (44-pin) | KC3-L (48-pin) | KD3-L | KE3-L | KF3-L | KG3-L |
|---|---|---|---|---|---|---|---|---|
| 00000H | $\overline{\text{RESET}}$ input, POC, LVI, WDT, TRAP | √ | √ | √ | √ | √ | √ | √ |
| 00004H | INTWDTI | √ | √ | √ | √ | √ | √ | √ |
| 00006H | INTLVI | √ | √ | √ | √ | √ | √ | √ |
| 00008H | INTP0 | √ | √ | √ | √ | √ | √ | √ |
| 0000AH | INTP1 | √ | √ | √ | √ | √ | √ | √ |
| 0000CH | INTP2 | √ | √ | √ | √ | √ | √ | √ |
| 0000EH | INTP3 | √ | √ | √ | √ | √ | √ | √ |
| 00010H | INTP4 | √ | √ | √ | √ | √ | √ | √ |
| 00012H | INTP5 | √ | √ | √ | √ | √ | √ | √ |
| 00014H | INTST3 | – | – | – | – | – | √ | √ |
| 00016H | INTSR3 | – | – | – | – | – | √ | √ |
| | INTCMP0 | √ | √ | √ | √ | √ | – | – |
| 00018H | INTSRE3 | – | – | – | – | – | √ | √ |
| | INTCMP1 | √ | √ | √ | √ | √ | – | – |
| 0001AH | INTDMA0 | √ | √ | √ | √ | √ | √ | √ |
| 0001CH | INTDMA1 | √ | √ | √ | √ | √ | √ | √ |
| 0001EH | INTST0/INTCSI00 | √ | √ | √ | √ | √ | √ | √ |
| 00020H | INTSR0/INTCSI01 | √ | √ | √ | √ | √ | √ | √ |
| 00022H | INTSRE0 | √ | √ | √ | √ | √ | √ | √ |
| 00024H | INTST1/INTCSI10/INTIIC10 | √ | √ | √ | √ | √ | √ | √ |
| 00026H | INTSR1 | √ | √ | √ | √ | √ | √ | √ |
| 00028H | INTSRE1 | √ | √ | √ | √ | √ | √ | √ |
| 0002AH | INTIICA | – | – | √ | √ | √ | √ | √ |
| 0002CH | INTTM00 | √ | √ | √ | √ | √ | √ | √ |
| 0002EH | INTTM01 | √ | √ | √ | √ | √ | √ | √ |
| 00030H | INTTM02 | √ | √ | √ | √ | √ | √ | √ |
| 00032H | INTTM03 | √ | √ | √ | √ | √ | √ | √ |

**Figure 5-11. Block Diagram of P50 and P51**

**(1) 78K0R/KE3-L**

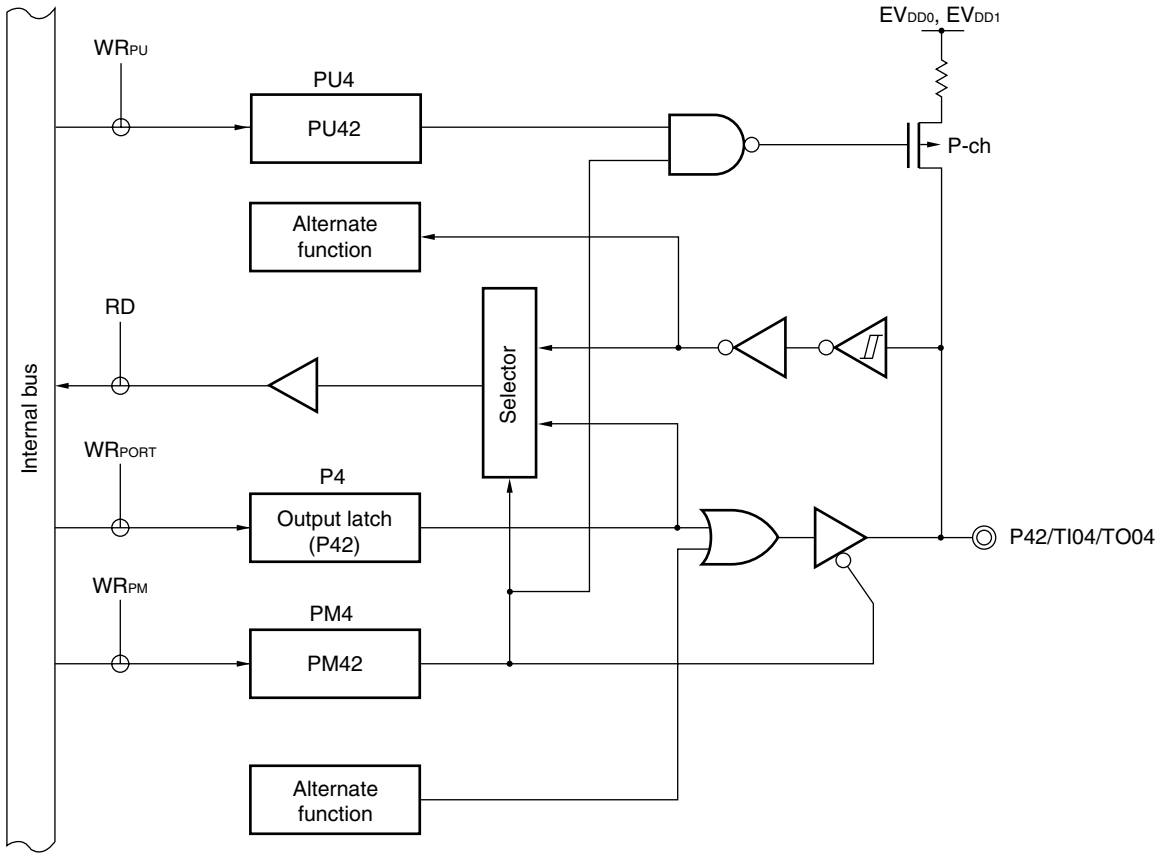



**(2) Products other than 78K0R/KE3-L**




P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

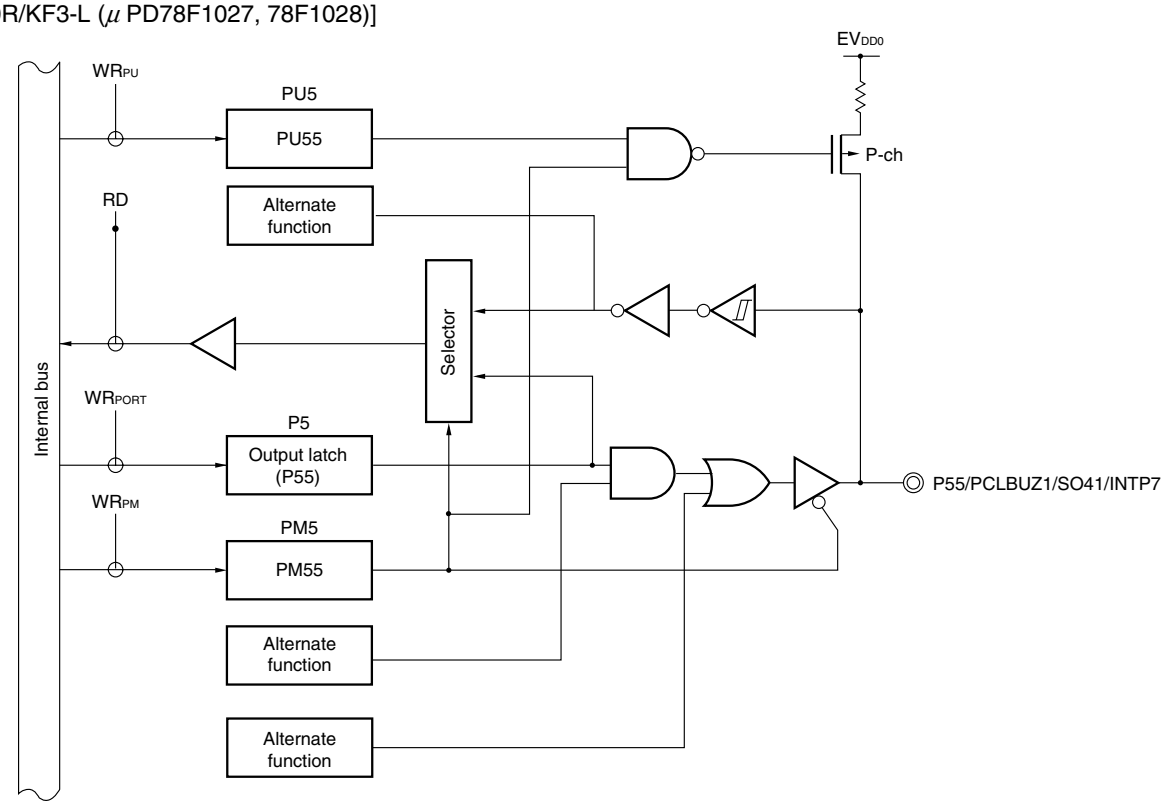
**Figure 6-17. Block Diagram of P42**



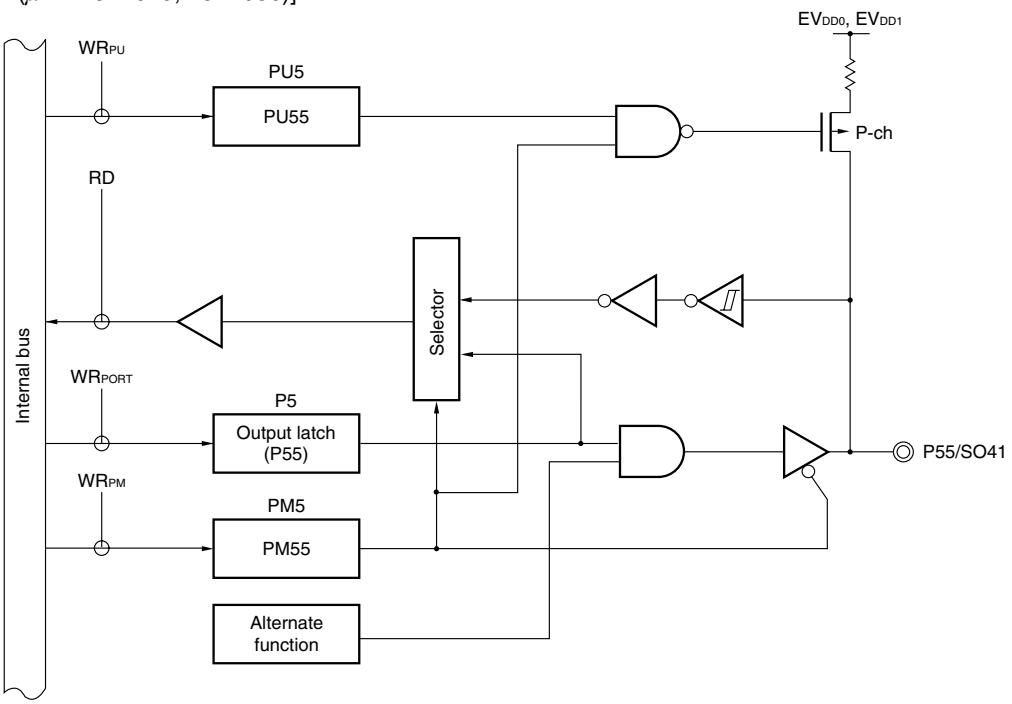

P4: Port register 4
PU4: Pull-up resistor option register 4
PM4: Port mode register 4
RD: Read signal
WR××: Write signal

**Figure 6-31. Block Diagram of P55**

[78K0R/KF3-L ($\mu$PD78F1027, 78F1028)]




[78K0R/KG3-L ($\mu$PD78F1029, 78F1030)]




P5: Port register 5
PU5: Pull-up resistor option register 5
PM5: Port mode register 5
RD: Read signal
WR××: Write signal

**(5) Full-scale error**

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (Full-scale – 3/2LSB) when the digital output changes from 1.....110 to 1.....111.

**(6) Integral linearity error**

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

**(7) Differential linearity error**

While the ideal width of code output is 1LSB, this indicates the difference between the actual measurement value and the ideal value.

**Figure 13-18. Zero-Scale Error**

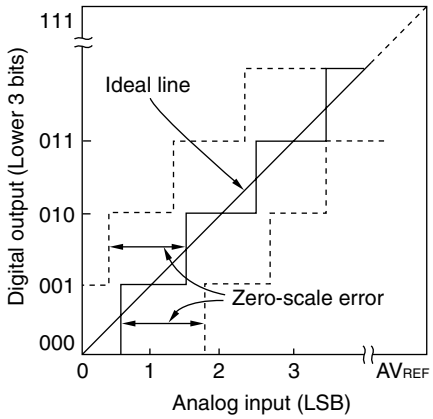



**Figure 13-19. Full-Scale Error**

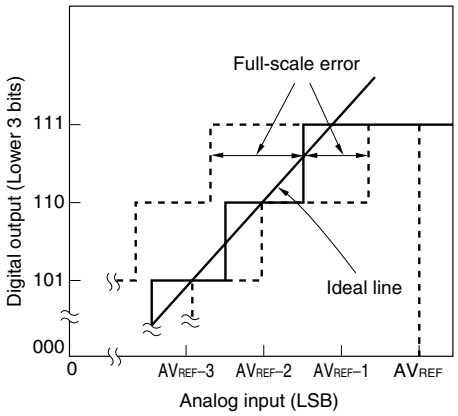



**Figure 13-20. Integral Linearity Error**

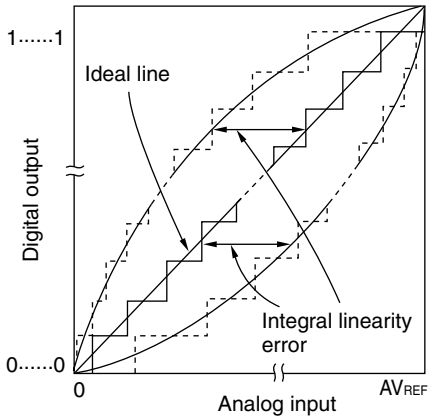
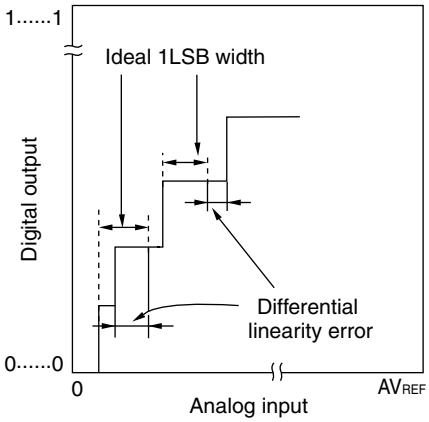



**Figure 13-21. Differential Linearity Error**




**(8) Conversion time**

This expresses the time from the start of sampling to when the digital output is obtained.

The sampling time is included in the conversion time in the characteristics table.

**(9) Sampling time**

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.

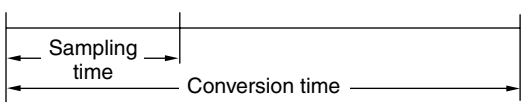


**Figure 14-44. Example of Contents of Registers for Master Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)**

**(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOEm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm2<br>0/1<br>Note 1 | SOEm1<br>0/1<br>Note 2 | SOEm0<br>0/1 |

**(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.**

<R>

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SSm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm3<br>× | SSm2<br>0/1<br>Note 2 | SSm1<br>0/1 | SSm0<br>0/1 |

**Notes 1.** Those bits are invalid while operating serial allay unit 1.

**2.** Those bits are invalid while operating serial allay unit 2.

**Remarks 1.** m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

**2.** ☐ : Setting is fixed in the CSI master transmission/reception mode

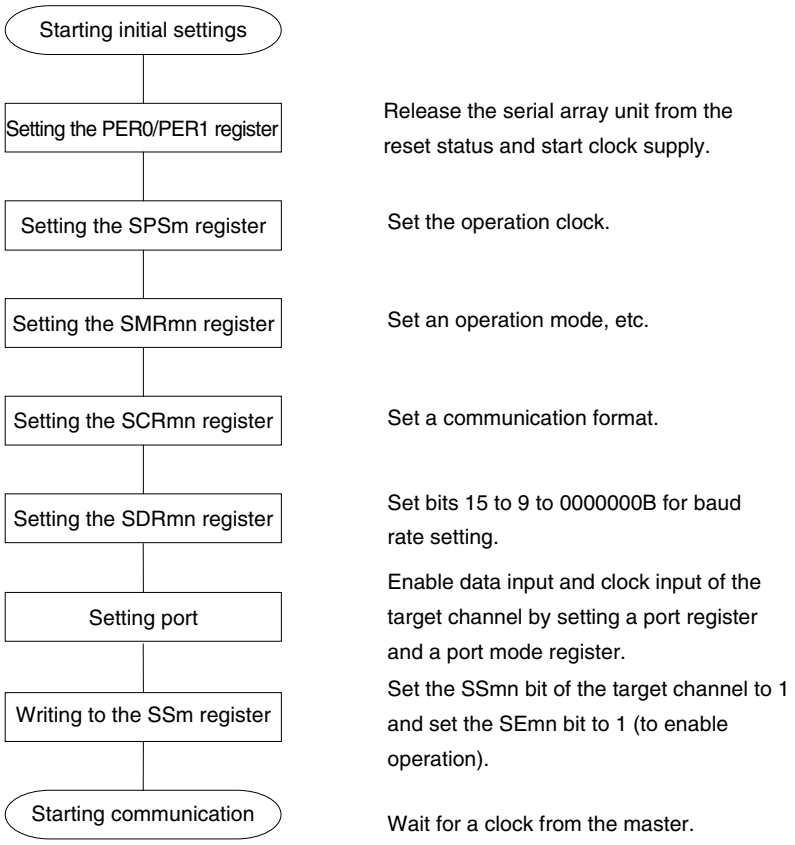
■ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

### (2) Operation procedure

**Figure 14-61. Initial Setting Procedure for Slave Reception**




**Caution After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more $f_{CLK}$ clocks have elapsed.**

**Figure 14-62. Procedure for Stopping Slave Reception**

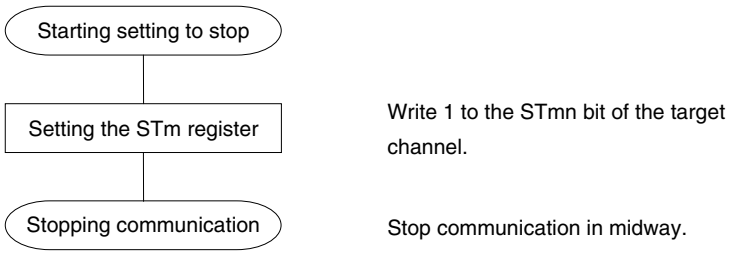
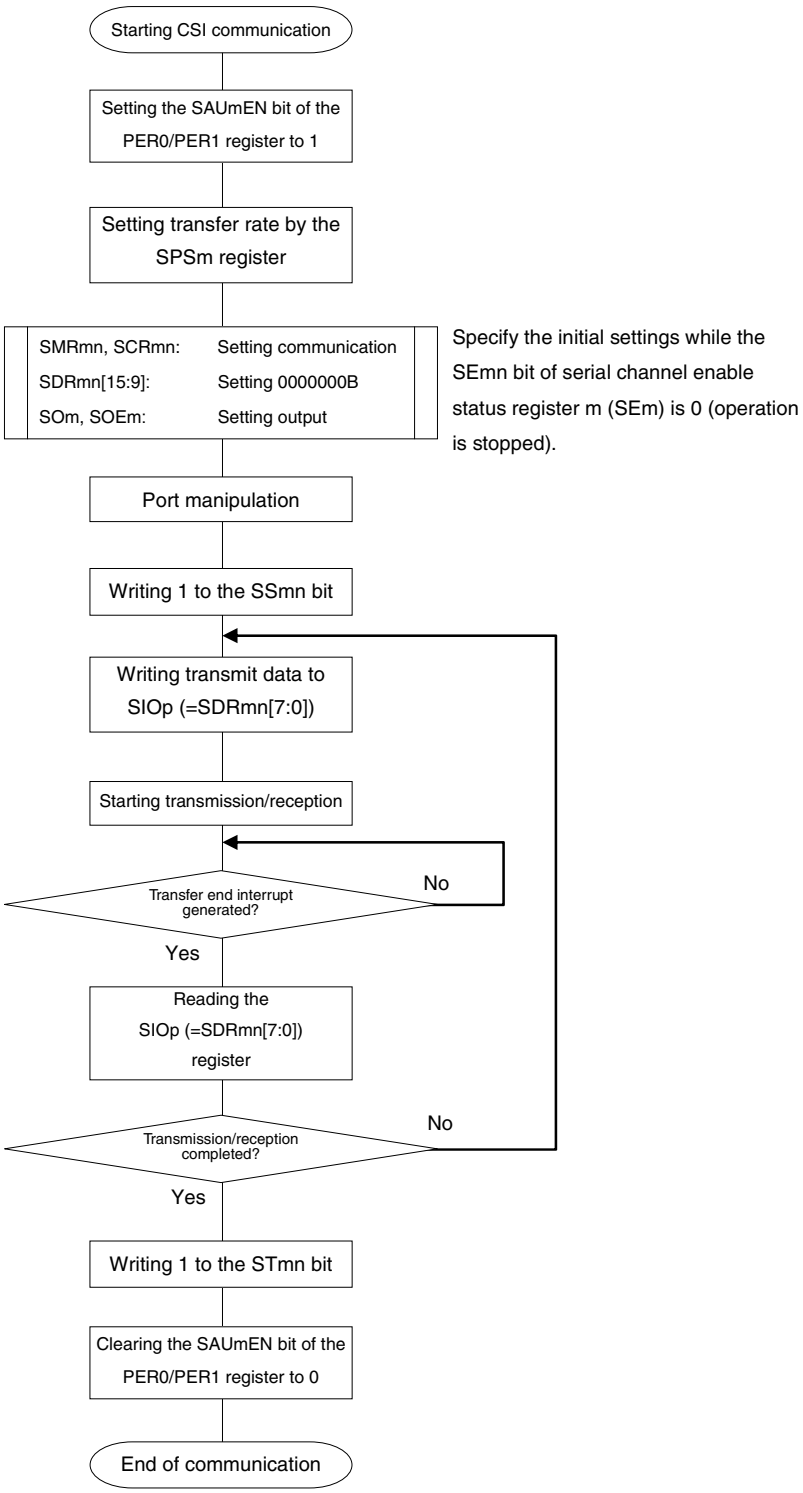


**Figure 14-71. Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)**




**Cautions 1. After setting the SAUmEN bit of peripheral enable register 0/1 (PER0/PER1) to 1, be sure to set serial clock select register m (SPSm) after 4 or more $f_{CLK}$ clocks have elapsed.**

**2. Be sure to set transmit data to the SIOp register before the clock from the master is started.**

**Table 14-17. Relationship between register settings and pins (Channel 0 of unit 2: CSI40, UART4 transmission)**

**(μPD78F1027, 78F1028, 78F1029, 78F1030 only)**

| SE 20 Note 1 | MD 202 | MD 201 | SOE 20 | SO 20 | CKO 20 | TXE 20 | RXE 20 | PM 50 | P50 | PM 51 Note 2 | P51 Note 2 | PM 52 | P52 | Operation mode | Pin Function | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | $\overline{\text{SCK40}}$/ INTP1/ P50 | SI40/ RxD4/ INTP2/ P51 Note 2 | SO40/ TxD4/ TO00/P52 |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | Operation stop mode | INTP1/ P50 | INTP2/ P51 | TO00/P52 |
| | 0 | 1 | | | | | | | | | | | | | | INTP2/ P51/RxD4 | |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | × | 1 | × | × Note 3 | × Note 3 | Slave CSI40 reception | $\overline{\text{SCK40}}$ (input) | SI40 | TO00/P52 |
| | | | 1 | 0/1 Note 4 | 1 | 1 | 0 | 1 | × | × Note 3 | × Note 3 | 0 | 1 | Slave CSI40 transmission | $\overline{\text{SCK40}}$ (input) | INTP2/P51 | SO40 |
| | | | 1 | 0/1 Note 4 | 1 | 1 | 1 | 1 | × | 1 | × | 0 | 1 | Slave CSI40 transmission/ reception | $\overline{\text{SCK40}}$ (input) | SI40 | SO40 |
| | | | 0 | 1 | 0/1 Note 4 | 0 | 1 | 0 | 1 | 1 | × | × Note 3 | × Note 3 | Master CSI40 reception | $\overline{\text{SCK40}}$ (output) | SI40 | TO00/P52 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 0 | 0 | 1 | × Note 3 | × Note 3 | 0 | 1 | Master CSI40 transmission | $\overline{\text{SCK40}}$ (output) | INTP2/P51 | SO40 |
| | | | 1 | 0/1 Note 4 | 0/1 Note 4 | 1 | 1 | 0 | 1 | 1 | × | 0 | 1 | Master CSI40 transmission/ reception | $\overline{\text{SCK40}}$ (output) | SI40 | SO40 |
| | 0 | 1 | 1 | 0/1 Note 4 | 1 | 1 | 0 | × Note 3 | × Note 3 | × Note 3 | × Note 3 | 0 | 1 | UART4 transmission Note 5 | INTP1/ P50 | INTP2/ P51/RxD4 | TxD4 |

**Notes 1.** Serial channel enable register 2 (SE2) is a read-only status register which is set using serial channel start register 2 (SS2) and serial channel stop register 2 (ST2).

**2.** When channel 1 of unit 2 is set to UART4 reception, this pin becomes an RxD4 function pin (refer to **Table 14-18**). In this case, operation stop mode or UART4 transmission must be selected for channel 0 of unit 2.

**3.** This pin can be set as a port function pin.

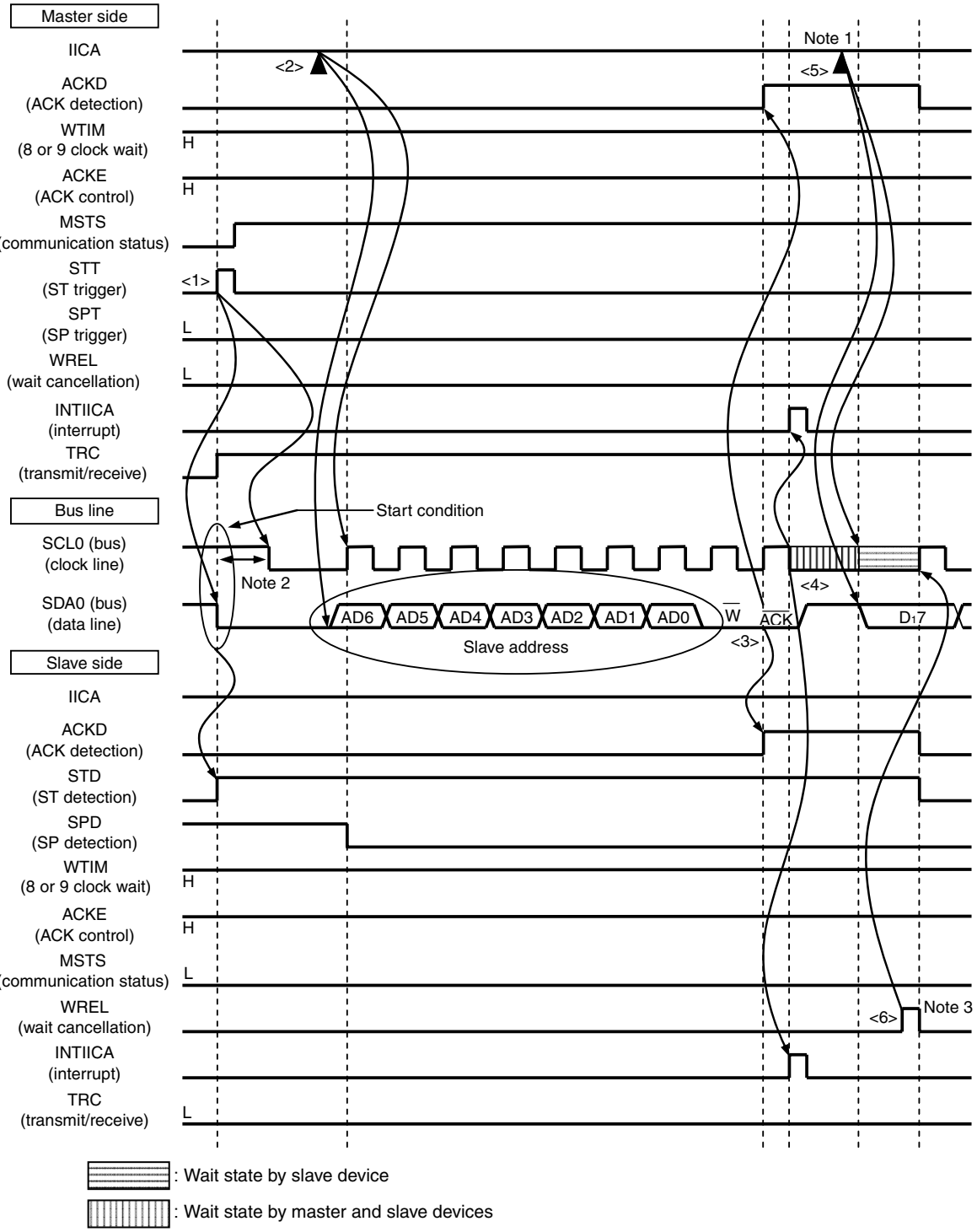
**4.** This is 0 or 1, depending on the communication operation. For details, refer to **14.3 (12) Serial output register m (SOm)**.

**5.** When using UART4 transmission and reception in a pair, set channel 1 of unit 2 to UART4 reception (refer to **Table 14-18**).

**Remark** X: Don't care

**Figure 15-32. Example of Master to Slave Communication (9-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (1/4)**

**(1) Start condition ~ address ~ data**




<R> **Notes 1.** Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a master device.

**2.** Make sure that the time between the fall of the SDA0 pin signal and the fall of the SCL0 pin signal is at least 4.0 μs when specifying standard mode and at least 0.6 μs when specifying fast mode.

<R> **3.** For releasing wait state during reception of a slave device, write “FFH” to IICA or set the WREL bit.

# CHAPTER 17 DMA CONTROLLER

The 78K0R/Kx3-L has an internal DMA (Direct Memory Access) controller.

Data can be automatically transferred between the peripheral hardware supporting DMA, SFRs, and internal RAM without via CPU.

As a result, the normal internal operation of the CPU and data transfer can be executed in parallel with transfer between the SFR and internal RAM, and therefore, a large capacity of data can be processed. In addition, real-time control using communication, timer, and A/D can also be realized.

## 17.1 Functions of DMA Controller

- Number of DMA channels: 2
- Transfer unit: 8 or 16 bits
- Maximum transfer unit: 1024 times
- Transfer type: 2-cycle transfer (One transfer is processed in 2 clocks and the CPU stops during that processing.)
- Transfer mode: Single-transfer mode
- Transfer request: Selectable from the following peripheral hardware interrupts
  - A/D converter
  - Serial interface (CSI00, CSI01, CSI10, UART0, UART1, UART3[Note], or IIC10)
  - Timer (channel 0, 1, 4, or 5)
- Transfer target: Between SFR and internal RAM

**Note** 78K0R/KF3-L, 78K0R/KG3-L only.

Here are examples of functions using DMA.

- Successive transfer of serial interface
- Batch transfer of analog data
- Capturing A/D conversion result at fixed interval
- Capturing port value at fixed interval

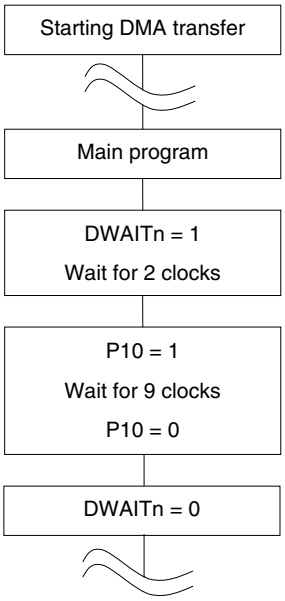
### 17.5.4 Holding DMA transfer pending by DWAITn bit

When DMA transfer is started, transfer is performed while an instruction is executed. At this time, the operation of the CPU is stopped and delayed for the duration of 2 clocks. If this poses a problem to the operation of the set system, a DMA transfer can be held pending by setting the DWAITn bit to 1. The DMA transfer for a transfer trigger that occurred while DMA transfer was held pending is executed after the pending status is canceled. However, because only one transfer trigger can be held pending for each channel, even if multiple transfer triggers occur for one channel during the pending status, only one DMA transfer is executed after the pending status is canceled.

To output a pulse with a width of 10 clocks of the operating frequency from the P10 pin, for example, the clock width increases to 12 if a DMA transfer is started midway. In this case, the DMA transfer can be held pending by setting the DWAITn bit to 1.

After setting the DWAITn bit to 1, it takes two clocks until a DMA transfer is held pending.

**Figure 17-10. Example of Setting for Holding DMA Transfer Pending by DWAITn Bit**




**Caution When DMA transfer is held pending while using both DMA channels, be sure to held the DMA transfer pending for both channels (by setting DWAIT0 and DWAIT1 to 1). If the DMA transfer of one channel is executed while that of the other channel is held pending, DMA transfer might not be held pending for the latter channel.**

**Remarks 1.** n: DMA channel number (n = 0, 1)

**2.** 1 clock: $1/f_{CLK}$ ($f_{CLK}$: CPU clock)

**Cautions 6. It can be selected by the option byte whether the internal low-speed oscillator continues oscillating or stops in the HALT or STOP mode. For details, see CHAPTER 25 OPTION BYTE.**

**7. The STOP instruction cannot be executed when the CPU operates on the 20 MHz internal high-speed oscillation clock. Be sure to execute the STOP instruction after shifting to internal high-speed oscillation clock operation.**

### 20.1.2 Registers controlling standby function

The standby function is controlled by the following two registers.

- Oscillation stabilization time counter status register (OSTC)
- Oscillation stabilization time select register (OSTS)

**Remark** For the registers that start, stop, or select the clock, see **CHAPTER 7 CLOCK GENERATOR**.

**Table 21-2. Hardware Statuses After Reset Acknowledgment (1/4)**

| Hardware | | After Reset Acknowledgment[Note 1] |
|---|---|---|
| Program counter (PC) | | The contents of the reset vector table (0000H, 0001H) are set. |
| Stack pointer (SP) | | Undefined |
| Program status word (PSW) | | 06H |
| RAM | Data memory | Undefined[Note 2] |
| | General-purpose registers | Undefined[Note 2] |
| Processor mode control register (PMC) | | 00H |
| Port registers (P0 to P9, P11 to P15) (output latches) | | 00H |
| Port mode registers | PM0 to PM9, PM11 to PM15[Note 3] | FFH |
| Port input mode registers 0, 1, 3, 7, 8, 14 (PIM0, PIM1, PIM3, PIM7, PIM8, PIM14) | | 00H |
| Port output mode registers 0, 1, 3, 7, 14 (POM0, POM1, POM3, POM7, POM14) | | 00H |
| Pull-up resistor option registers (PU0, PU1, PU3 to PU9, PU11 to PU14) | | 00H |
| Clock operation mode control register (CMC) | | 00H |
| Clock operation status control register (CSC) | | C0H |
| System clock control register (CKC) | | 09H |
| 20 MHz internal high-speed oscillation control register (DSCCTL) | | 00H |
| Oscillation stabilization time counter status register (OSTC) | | 00H |
| Oscillation stabilization time select register (OSTS) | | 07H |
| Noise filter enable registers 0, 1, 2 (NFEN0, NFEN1, NFEN2) | | 00H |
| Peripheral enable registers 0, 1, 2 (PER0, PER1, PER2) | | 00H |
| Operation speed mode control register (OSMC) | | 00H |
| Timer array unit | Timer data registers 00 to 07, 10 to 13 (TDR00 to TDR07, TDR10 to TDR13) | 0000H |
| | Timer mode registers 00 to 07, 10 to 13 (TMR00 to TMR07, TMR10 to TMR13) | 0000H |
| | Timer status registers 00 to 07, 10 to 13 (TSR00 to TSR07, TSR10 to TSR13) | 0000H |
| | Timer input select registers 0, 1 (TIS0, TIS1) | 00H |
| | Timer counter registers 00 to 07, 10 to 13 (TCR00 to TCR07, TCR10 to TCR13) | FFFFH |
| | Timer channel enable status registers 0, 1 (TE0, TE1) | 0000H |
| | Timer channel start registers 0, 1 (TS0, TS1) | 0000H |
| | Timer channel stop registers 0, 1 (TT0, TT1) | 0000H |
| | Timer clock select registers 0, 1 (TPS0, TPS1) | 0000H |
| | Timer output registers 0, 1 (TO0, TO1) | 0000H |
| | Timer output enable registers 0 , 1(TOE0, TOE1) | 0000H |
| | Timer output level registers 0, 1 (TOL0, TOL1) | 0000H |
| | Timer output mode registers 0, 1 (TOM0, TOM1) | 0000H |

**Notes 1.** During reset signal generation or oscillation stabilization time wait, only the PC contents among the hardware statuses become undefined. All other hardware statuses remain unchanged after reset.

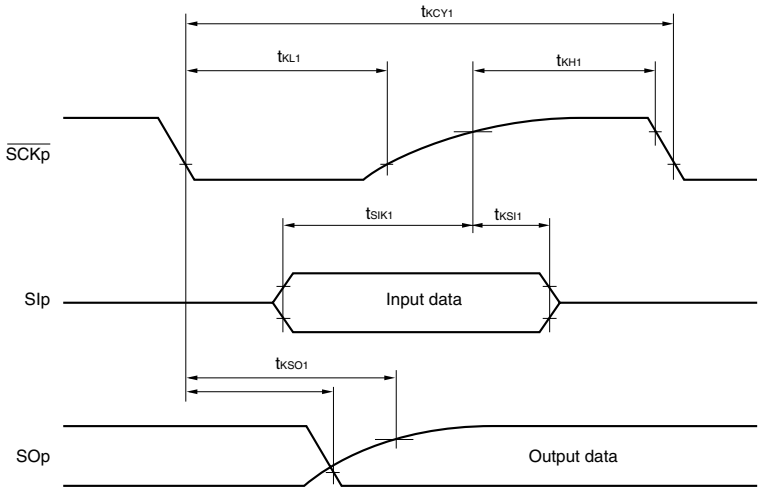
**2.** When a reset is executed in the standby mode, the pre-reset status is held even after reset.

**3.** In the 78K0R/KC3-L, 78K0R/KD3-L, and 78K0R/KE3-L, the reset value of the PM14 register is FEH. In the 78K0R/KF3-L and 78K0R/KG3-L, the reset value of the PM13 register is FEH.

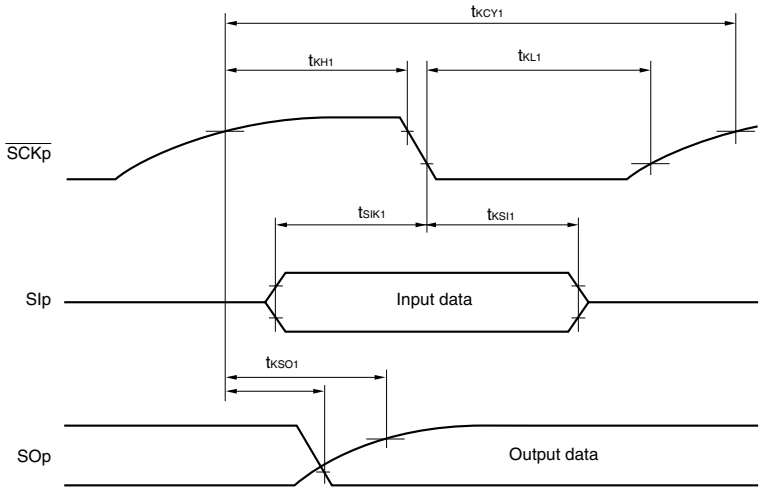
**Remark** The special function register (SFR) mounted depend on the product. See **4.2.4 Special function registers (SFRs)** and **4.2.5 Extended special function registers (2nd SFRs: 2nd Special Function Registers)**.

**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

**CSI mode serial transfer timing: master mode (communication at different potential)**
**(When DAP0n = 0 and CKP0n = 0, or DAP0n = 1 and CKP0n = 1)**




**CSI mode serial transfer timing: master mode (communication at different potential)**
**(When DAP0n = 0 and CKP0n = 1, or DAP0n = 1 and CKP0n = 0)**

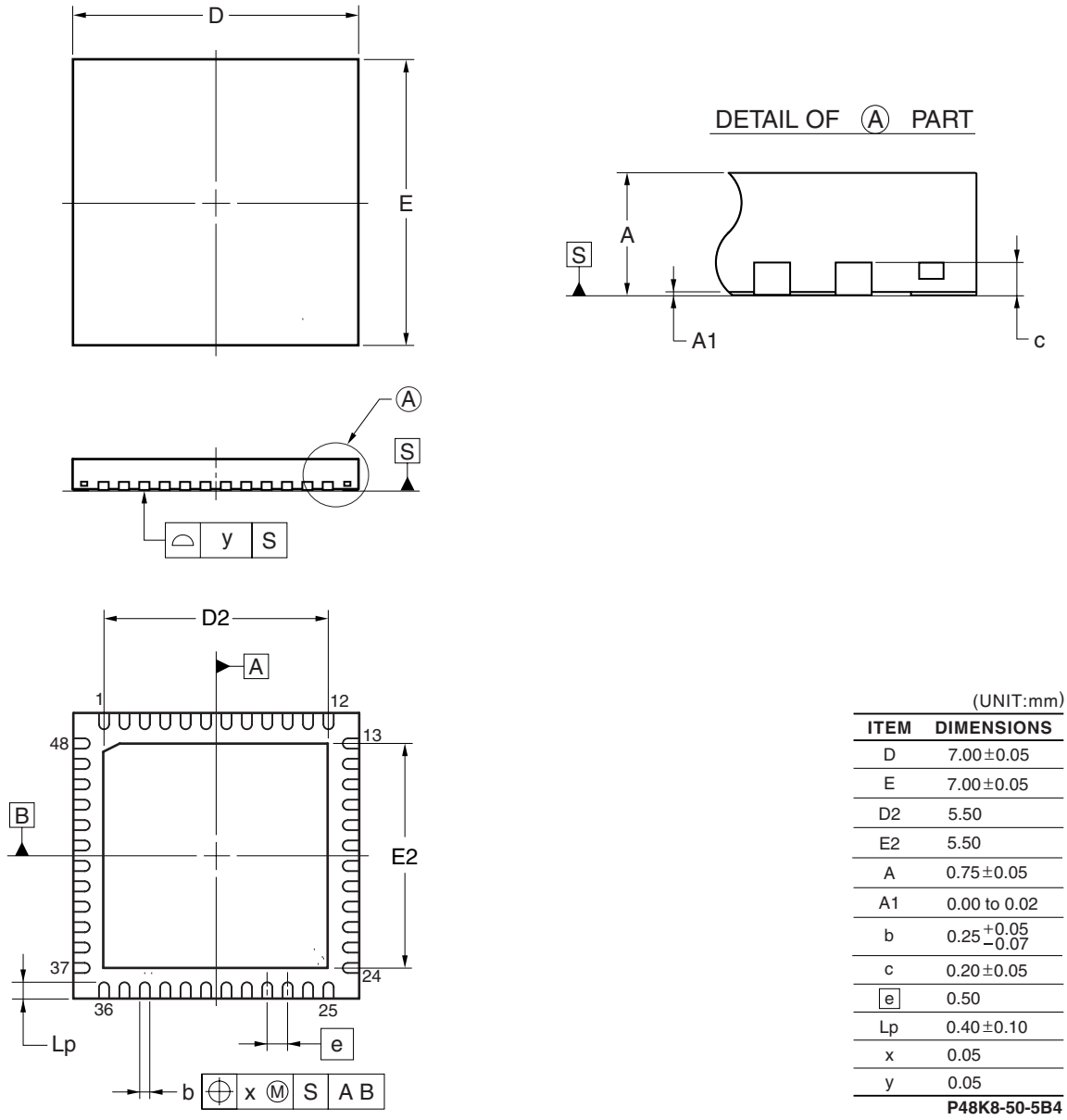



**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark** p: CSI number (p = 00, 01, 10), n: Channel number (n = 0 to 2), g: PIM and POM number (g = 3, 7)

μPD78F1001K8-5B4-AX, 78F1002K8-5B4-AX, 78F1003K8-5B4-AX (Under development)

## 48-PIN PLASTIC WQFN(7x7)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.05 |
| E | 7.00±0.05 |
| D2 | 5.50 |
| E2 | 5.50 |
| A | 0.75±0.05 |
| A1 | 0.00 to 0.02 |
| b | $0.25^{+0.05}_{-0.07}$ |
| c | 0.20±0.05 |
| e | 0.50 |
| Lp | 0.40±0.10 |
| x | 0.05 |
| y | 0.05 |

P48K8-50-5B4