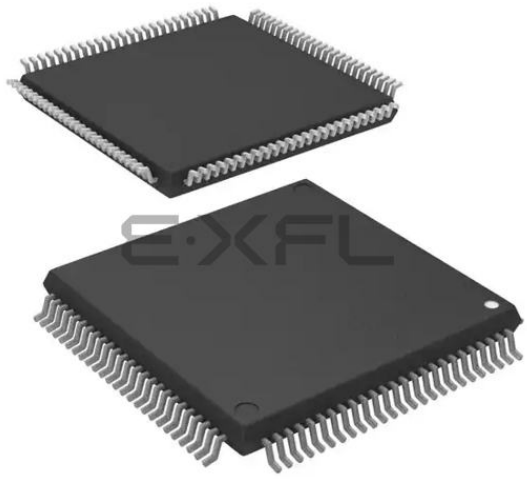
Renesas Electronics America Inc - UPD78F1013GC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1013gc-ueu-ax

14.9.2 78K0R/KF3-L, 78K0R/KG3-L 747

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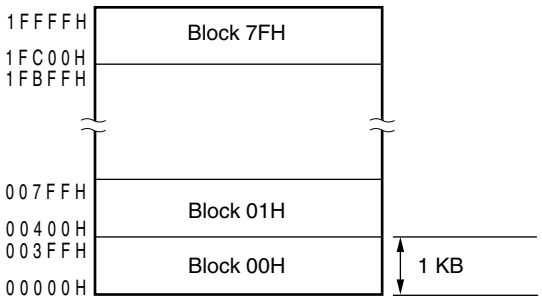
(2/2)

Item		78K0R/KF3-L					78K0R/KG3-L			
		μPD78F1010	μPD78F1011	μPD78F1012	μPD78F1027	μPD78F1028	μPD78F1013	μPD78F1014	μPD78F1029 Note 1	μPD78F1030 Note 1
Clock output/buzzer output		2								
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (peripheral hardware clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)								
10-bit resolution A/D converter (AV_{REF} = 1.8 to 5.5 V)		12 channels					16 channels			
Comparators		–								
Programmable gain amplifiers		–								
Serial interface		• CSI: 2 channels/UART: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • UART supporting LIN-bus: 1 channel • CSI: 2 channels/UART: 1 channel (μPD78F1027, 78F1028, 78F1029, 78F1030)								
	I^2C bus	1 channel								
Multiplier/divider		• 16 bits × 16 bits = 32 bits (multiplication) • 32 bits ÷ 32 bits = 32 bits (division)								
DMA controller		2 channels								
Vectored interrupt sources	Internal	33			35		33			35
	External	13								
Key interrupt		8 channels (KR0 to KR7)								
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by a reset processing check error								
Power-on-clear circuit		• Power-on-reset: 1.61 ±0.09 V • Power-down-reset: 1.59 ±0.09 V								
Low-voltage detector		1.91 V to 4.22 V (16 stages)								
On-chip debug function		Provided								
Power supply voltage		V_{DD} = 1.8 to 5.5 V								
Operating ambient temperature		T_A = −40 to +85 °C								

Notes 1. The μPD78F1029 and μPD78F1030 don't have the FBGA package.

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Remark The flash memory is divided into blocks (one block = 1 KB). For the address values and block numbers, see **Table 4-1 Correspondence Between Address Values and Block Numbers in Flash Memory**.



(μPD78F1012, 78F1014)

4.1.1 Internal program memory space

The internal program memory space stores the program and table data.

The 78K0R/Kx3-L products incorporate internal ROM (flash memory), as shown below.

Table 4-2. Internal ROM Capacity

Part Number	Internal ROM	
	Structure	Capacity
μPD78F1000	Flash memory	16384 × 8 bits (00000H to 03FFFH)
μPD78F1001, 78F1004, 78F1007		32768 × 8 bits (00000H to 07FFFH)
μPD78F1002, 78F1005, 78F1008		49152 × 8 bits (00000H to 0BFFFH)
μPD78F1003, 78F1006, 78F1009, 78F1010		65536 × 8 bits (00000H to 0FFFFH)
μPD78F1011, 78F1013		98304 × 8 bits (00000H to 17FFFH)
μPD78F1012, 78F1014		131072 × 8 bits (00000H to 1FFFFH)
μPD78F1027, 78F1029		196608 × 8 bits (00000H to 2FFFFH)
μPD78F1028, 78F1030		262144 × 8 bits (00000H to 3FFFFH)

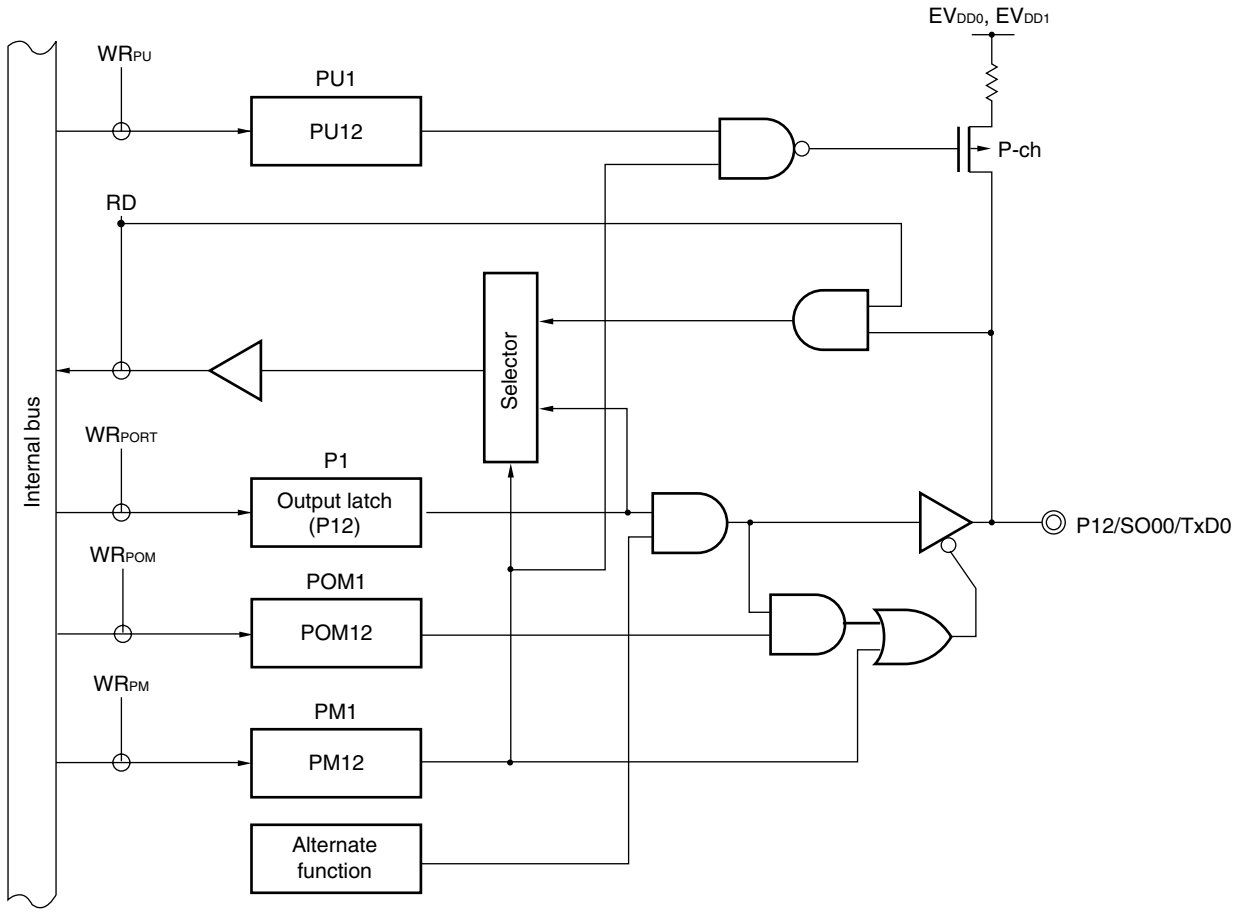
The internal program memory space is divided into the following areas.

(1) Vector table area

The 128-byte area 00000H to 0007FH is reserved as a vector table area. The program start addresses for branch upon reset or generation of each interrupt request are stored in the vector table area. Furthermore, the interrupt jump address is a 64 K address of 00000H to 0FFFFH, because the vector code is assumed to be 2 bytes.

Of the 16-bit address, the lower 8 bits are stored at even addresses and the higher 8 bits are stored at odd addresses.

Figure 6-8. Block Diagram of P12



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
POM1: Port output mode register 1
RD: Read signal
WR××: Write signal

Figure 7-7. Format of Oscillation Stabilization Time Counter Status Register (OSTC)

Address: FFFA2H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
OSTC	MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18

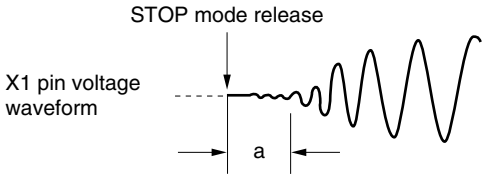
MOST 8	MOST 9	MOST 10	MOST 11	MOST 13	MOST 15	MOST 17	MOST 18	Oscillation stabilization time status		
									fx = 10 MHz	fx = 20 MHz
0	0	0	0	0	0	0	0	2^8/fx max.	25.6 μs max.	12.8 μs max.
1	0	0	0	0	0	0	0	2^8/fx min.	25.6 μs min.	12.8 μs min.
1	1	0	0	0	0	0	0	2^9/fx min.	51.2 μs min.	25.6 μs min.
1	1	1	0	0	0	0	0	2^{10}/fx min.	102.4 μs min.	51.2 μs min.
1	1	1	1	0	0	0	0	2^{11}/fx min.	204.8 μs min.	102.4 μs min.
1	1	1	1	1	0	0	0	2^{13}/fx min.	819.2 μs min.	409.6 μs min.
1	1	1	1	1	1	0	0	2^{15}/fx min.	3.27 ms min.	1.64 ms min.
1	1	1	1	1	1	1	0	2^{17}/fx min.	13.11 ms min.	6.55 ms min.
1	1	1	1	1	1	1	1	2^{18}/fx min.	26.21 ms min.	13.11 ms min.

Cautions 1. After the above time has elapsed, the bits are set to 1 in order from the MOST8 bit and remain 1.

2. The oscillation stabilization time counter counts up to the oscillation stabilization time set by the oscillation stabilization time select register (OSTS).
In the following cases, set the oscillation stabilization time of the OSTS register to the value greater than the count value which is to be checked by the OSTC register after the oscillation starts.

- **If the X1 clock starts oscillation while the internal high-speed oscillation clock or subsystem clock is being used as the CPU clock.**
- **If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock with the X1 clock oscillating.**
(Note, therefore, that only the status up to the oscillation stabilization time set by the OSTS register is set to the OSTC register after the STOP mode is released.)

3. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts ("a" below).



Remark fx: X1 clock oscillation frequency

(9) Timer output enable register m (TOEm)

The TOEm register is used to enable or disable timer output of each channel.

Channel n for which timer output has been enabled becomes unable to rewrite the value of the TOmn bit of timer output register m (TOm) described later by software, and the value reflecting the setting of the timer output function through the count operation is output from the timer output pin (TOmn).

The TOEm register can be set by a 16-bit memory manipulation instruction.

The lower 8 bits of the TOEm register can be set with a 1-bit or 8-bit memory manipulation instruction with TOEmL.

Reset signal generation clears this register to 0000H.

Figure 8-22. Format of Timer Output Enable register m (TOEm)

Address: F01BAH, F01BBH After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE0	0	0	0	0	0	0	0	0	TOE07	TOE06	TOE05	TOE04	TOE03	TOE02	TOE01	TOE00

Address: F01E2H, F01E3H After reset: 0000H R/W

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOE1	0	0	0	0	0	0	0	0	0	0	0	0	TOE13	TOE12	TOE11	TOE10

TOEmn	Timer output enable/disable of channel n
0	The TOmn operation stopped by count operation (timer channel output bit). Writing to the TOmn bit is enabled. The TOmn pin functions as data output, and it outputs the level set to the TOmn bit. The output level of the TOmn pin can be manipulated by software.
1	The TOmn operation enabled by count operation (timer channel output bit). Writing to the TOmn bit is disabled (writing is ignored). The TOmn pin functions as timer output, and the TOEmn bit is set or reset depending on the timer operation. The TOmn pin outputs the square-wave or PWM depending on the timer operation.

Caution Be sure to clear bits 15 to 8 of the TOE0 register and bits 15 to 4 of the TOE1 register to "0".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Figure 8-28. Format of Noise Filter Enable Registers 1, 2 (NFEN1, NFEN2) (78K0R/KF3-L, 78K0R/KG3-L) (1/2)

Address: F0061H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN1	TNFEN07	TNFEN06	TNFEN05	TNFEN04	TNFEN03	TNFEN02	TNFEN01	TNFEN00

Address: F0062H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
NFEN2	0	0	0	0	TNFEN13	TNFEN12	TNFEN11	TNFEN10

TNFEN07	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: SI41[Note 1]/TI07/TO07/P54 pin or RxD3/P14 pin[Note 2] 78K0R/KG3-L: TI07/TO07/P145 pin or RxD3/P14 pin[Note 2]
0	Noise filter OFF
1	Noise filter ON

TNFEN06	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: TI06/TO06/P06 pin 78K0R/KG3-L: TI06/TO06/P131 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN05	Enable/disable using noise filter of the following pin input signal 78K0R/KF3-L: TI05/TO05/P05 pin 78K0R/KG3-L: TI05/TO05/P146 pin
0	Noise filter OFF
1	Noise filter ON

TNFEN04	Enable/disable using noise filter of TI04/TO04/P42 pin input signal
0	Noise filter OFF
1	Noise filter ON

TNFEN03	Enable/disable using noise filter of TI03/TO03/INTP4/P31 pin input signal
0	Noise filter OFF
1	Noise filter ON

Notes 1. SI41 pin is only mounted in the μPD78F1027 and 78F1028.

2. The applicable pin can be switched by setting the ISC1 bit of the ISC register.

ISC1 = 0: Whether or not to use the noise filter of the TI07 pin can be selected.

ISC1 = 1: Whether or not to use the noise filter of the RxD3 pin can be selected.

(2) Scan mode

The four analog input channels of scans 0 to 3, which are specified by the analog input channel specification register (ADS), while the ADMD bit of the A/D converter mode register (ADM) is 1, are A/D converted successively. A/D conversion is performed in sequence, starting from the analog input channel specified by scan 0.

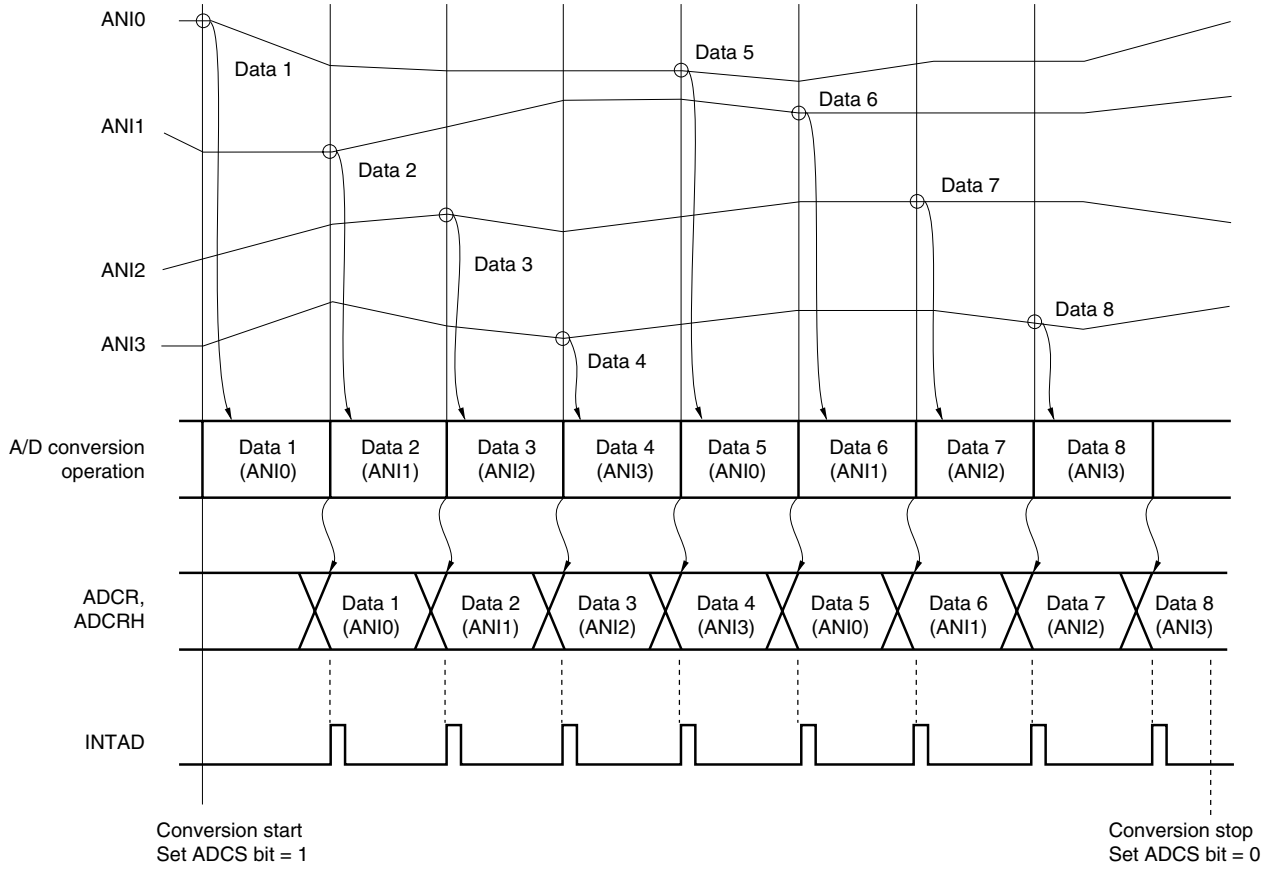
When A/D conversion of one analog input is complete, the conversion result is stored in the A/D conversion result register (ADCR) and the A/D conversion end interrupt request signal (INTAD) is generated.

The A/D conversion results of all the analog input channels are stored in the ADCR register. It is therefore recommended to save the contents of the ADCR register to RAM, once A/D conversion of one analog input channel has been completed.

After A/D conversion has been completed, A/D conversion is repeated successively, unless the ADCS bit is set to 0.

If anything is written to the ADM or ADS register during conversion, A/D conversion is aborted. In this case, A/D conversion is started again from the analog input channel of scan 0.

Figure 13-15. Example of Scan Mode Operation Timing



(10) Serial channel enable status register m (SEm)

The SEm register indicates whether data transmission/reception operation of each channel is enabled or stopped.

When 1 is written a bit of serial channel start register m (SSm), the corresponding bit of this register is set to 1.

When 1 is written a bit of serial channel stop register m (STm), the corresponding bit is cleared to 0.

Channel n that is enabled to operate cannot rewrite by software the value of the CKOmn bit (serial clock output of channel n) of serial output register m (SOm) to be described below, and a value reflected by a communication operation is output from the serial clock pin.

Channel n that stops operation can set the value of the CKOmn bit of the SOm register by software and output its value from the serial clock pin. In this way, any waveform, such as that of a start condition/stop condition, can be created by software.

The SEm register can be read by a 16-bit memory manipulation instruction.

The lower 8 bits of the SEm register can be set with an 1-bit or 8-bit memory manipulation instruction with SEmL.

Reset signal generation clears the SEm register to 0000H.

Figure 14-14. Format of Serial Channel Enable Status Register m (SEm)

Address: F0120H, F0121H (SE0), F0160H, F0161H (SE1), F0210H, F0211H (SE2) After reset: 0000H R

Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEm	0	0	0	0	0	0	0	0	0	0	0	0	SEm 3 Note	SEm 2 Note	SEm 1	SEm 0

SEm n	Indication of operation enable/stop status of channel n
0	Operation stops
1	Operation is enabled.

Note Those bits are invalid while operating serial allay unit 2.

Remark m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 03

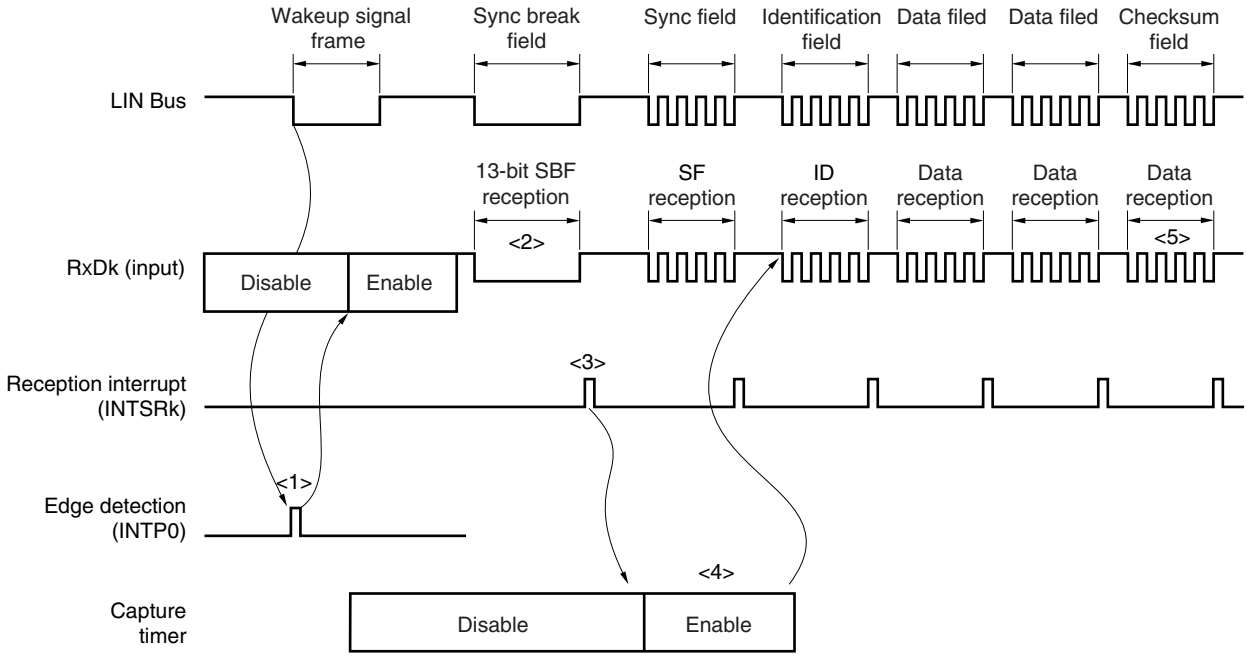
78K0R/KF3-L□μ PD78F1010, 78F1011, 78F1012□: mn = 00 to 03, 10 to 13

78K0R/KF3-L□μ PD78F1027, 78F1028□: mn = 00 to 03, 10 to 13, 20, 21

78K0R/KG3-L□μ PD78F1013, 78F1014□: mn = 00 to 03, 10 to 13

78K0R/KG3-L□μ PD78F1029, 78F1030□: mn = 00 to 03, 10 to 13, 20, 21

Figure 14-94. Reception Operation of LIN



Here is the flow of signal processing.

<1> The wakeup signal is detected by detecting an interrupt edge (INTP0) on a pin. When the wakeup signal is detected, enable reception of UARTk (RXEmn = 1) and wait for SBF reception.

<2> When the start bit of SBF is detected, reception is started and serial data is sequentially stored in the RXDk register (= bits 7 to 0 of serial data register mn (SDRmn)) at the set baud rate. When the stop bit is detected, the reception end interrupt request (INTSRk) is generated. When data of low levels of 11 bits or more is detected as SBF, it is judged that SBF reception has been correctly completed. If data of low levels of less than 11 bits is detected as SBF, it is judged that an SBF reception error has occurred, and the system returns to the SBF reception wait status.

<3> When SBF reception has been correctly completed, start channel 7 of the timer array unit 0 and measure the bit interval (pulse width) of the sync field (see **8.7.5 Operation as input signal high-/low-level width measurement**).

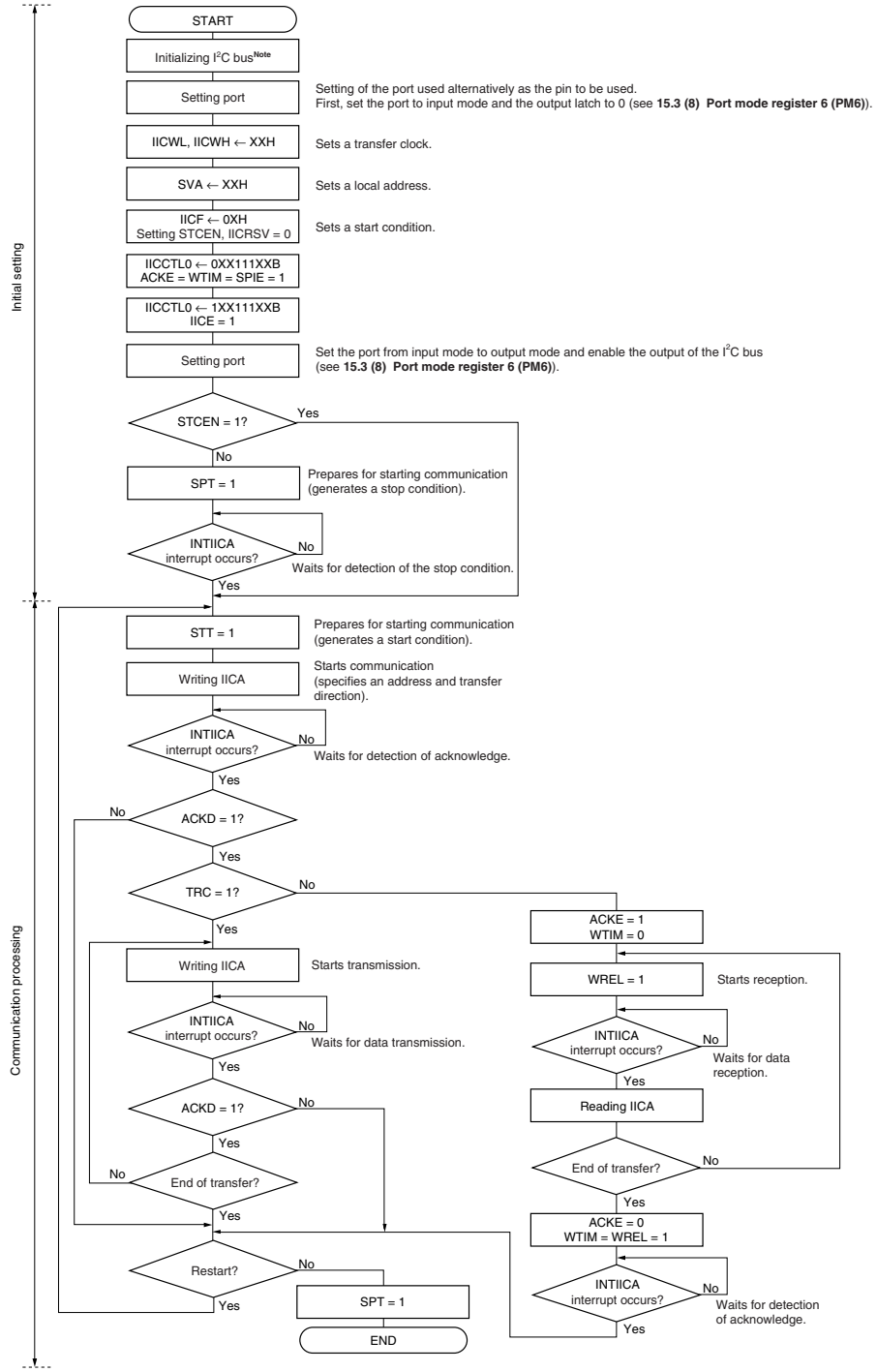
<4> Calculate a baud rate error from the bit interval of sync field (SF). Stop UARTk once and adjust (re-set) the baud rate.

<5> The checksum field should be distinguished by software. In addition, processing to initialize UARTk after the checksum field is received and to wait for reception of SBF should also be performed by software.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 1, 3),
k: Number of UART used for LIN communication (k = 0, 3)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 01, k = 0
78K0R/KF3-L, 78K0R/KG3-L: mn = 13, k = 3

(1) Master operation in single-master system

Figure 15-28. Master Operation in Single-Master System



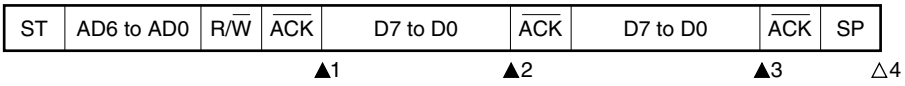
Note Release (SCL0 and SDA0 pins = high level) the I^2C bus in conformance with the specifications of the product that is communicating. If EEPROM is outputting a low level to the SDA0 pin, for example, set the SCL0 pin in the output port mode, and output a clock pulse from the output port until the SDA0 pin is constantly at high level.

Remark Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

(2) Slave device operation (slave address data reception)

(a) Start ~ Address ~ Data ~ Data ~ Stop

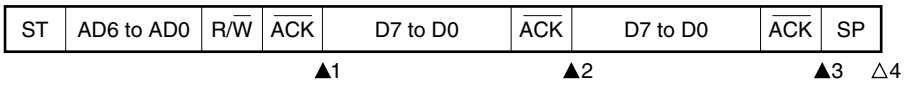
(i) When WTIM = 0



▲1: IICS = 0001×110B
▲2: IICS = 0001×000B
▲3: IICS = 0001×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1



▲1: IICS = 0001×110B
▲2: IICS = 0001×100B
▲3: IICS = 0001××00B
△4: IICS = 00000001B

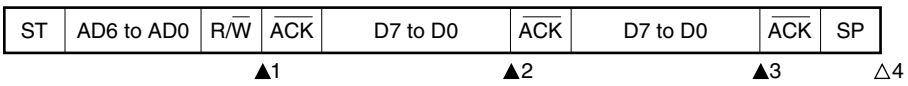
Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(3) Slave device operation (when receiving extension code)

The device is always participating in communication when it receives an extension code.

(a) Start ~ Code ~ Data ~ Data ~ Stop

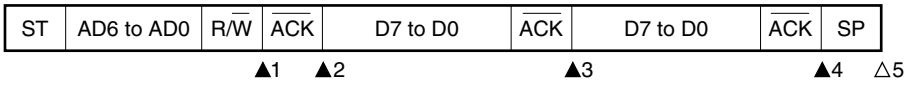
(i) When WTIM = 0



▲1: IICS = 0010×010B
▲2: IICS = 0010×000B
▲3: IICS = 0010×000B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

(ii) When WTIM = 1



▲1: IICS = 0010×010B
▲2: IICS = 0010×110B
▲3: IICS = 0010×100B
▲4: IICS = 0010××00B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

17.5.5 Forced termination by software

After the DSTn bit is set to 0 by software, it takes up to 2 clocks until a DMA transfer is actually stopped and the DSTn bit is set to 0. To forcibly terminate a DMA transfer by software without waiting for occurrence of the interrupt (INTDMAn) of DMAn, therefore, perform either of the following processes.

<When using one DMA channel>

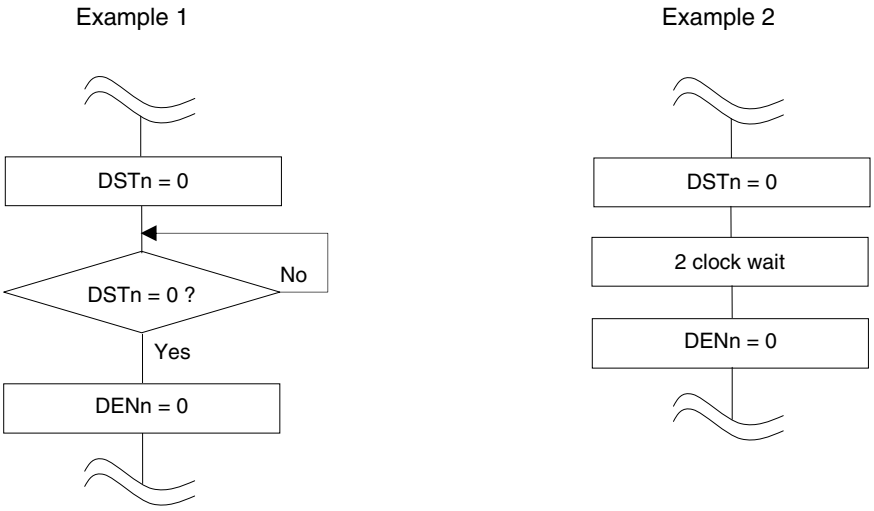
- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software, confirm by polling that the DSTn bit has actually been cleared to 0, and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction).

- Set the DSTn bit to 0 (use DRCn = 80H to write with an 8-bit manipulation instruction) by software and then set the DENn bit to 0 (use DRCn = 00H to write with an 8-bit manipulation instruction) two or more clocks after.

<When using both DMA channels>

- To forcibly terminate DMA transfer by software when using both DMA channels (by setting DSTn to 0), clear the DSTn bit to 0 after the DMA transfer is held pending by setting the DWAIT0 and DWAIT1 bits of both channels to 1. Next, clear the DWAIT0 and DWAIT1 bits of both channels to 0 to cancel the pending status, and then clear the DENn bit to 0.

Figure 17-11. Forced Termination of DMA Transfer (1/2)



Remarks 1. n: DMA channel number (n = 0, 1)

2. 1 clock: $1/f_{CLK}$ (f_{CLK}: CPU clock)

(4) External interrupt rising edge enable registers (EGP0, EGP1), external interrupt falling edge enable registers (EGN0, EGN1)

These registers specify the valid edge for INTP0 to INTP11.

The EGP0, EGP1, EGN0, and EGN1 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 18-10. Format of External Interrupt Rising Edge Enable Registers (EGP0, EGP1) and External Interrupt Falling Edge Enable Registers (EGN0, EGN1)

Address: FFF38H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP0	EGP7	EGP6	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FFF39H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN0	EGN7	EGN6	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

Address: FFF3AH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP1	0	0	0	0	EGP11	EGP10	EGP9	EGP8

Address: FFF3BH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN1	0	0	0	0	EGN11	EGN10	EGN9	EGN8

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 11)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

Table 18-5 shows the ports corresponding to the EGPn and EGNn bits.

Table 18-5. Ports Corresponding to EGPn and EGNn bits

Detection Enable Bit		Edge Detection Port		Interrupt Request Signal
		78K0R/KF3-L	78K0R/KG3-L	
EGP0	EGN0	P120	P120	INTP0
EGP1	EGN1	P50	P46	INTP1
EGP2	EGN2	P51	P47	INTP2
EGP3	EGN3	P30	P30	INTP3
EGP4	EGN4	P31	P31	INTP4
EGP5	EGN5	P16	P16	INTP5
EGP6	EGN6	P140	P140	INTP6
EGP7	EGN7	P55	P141	INTP7
EGP8	EGN8	P74	P74	INTP8
EGP9	EGN9	P75	P75	INTP9
EGP10	EGN10	P76	P76	INTP10
EGP11	EGN11	P77	P77	INTP11

Caution Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.

Remark n = 0 to 11

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Real-time counter operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz		V_{DD} = 3.0 V		0.2	1.0	μA
				V_{DD} = 2.0 V		0.2	1.0	μA
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 30 kHz				0.31	0.35	μA
A/D converter operating current	I_{ADC} Note 4	During conversion at maximum speed	High speed mode 1	AV_{REF} = V_{DD} = 5.0 V		1.72	3.2	mA
			High speed mode 2	AV_{REF} = V_{DD} = 3.0 V		0.72	1.6	mA
			Normal mode	AV_{REF} = V_{DD} = 5.0 V		0.86	1.9	mA
			Low voltage mode	AV_{REF} = V_{DD} = 3.0 V		0.37	0.8	mA
Programmable gain amplifier operating current	I_{AMP} Note 5					0.56	1.2	mA
Comparator operating current	I_{CMP} Note 6	Per channel when the internal reference voltage is not used		AV_{REF} = V_{DD} = 5.0 V		120	240	μA
				AV_{REF} = V_{DD} = 3.0 V			120	μA
		Per channel when the internal reference voltage is used		AV_{REF} = V_{DD} = 5.0 V		160	300	μA
				AV_{REF} = V_{DD} = 3.0 V			150	μA
LVI operating current	I_{LVI} Note 7					9	18	μA

Notes 1. Current flowing only to the real-time counter (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time counter operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time counter operating current. When the real-time counter operates during f_{CLK} = f_{SUB}/2, the TYP. value of I_{DD2} includes the real-time counter operating current.

2. When internal high-speed oscillation, 20 MHz internal high-speed oscillation, and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the 30 kHz internal oscillator). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB}/2 when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter (AV_{REF} pin). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the programmable gain amplifier (AV_{REF} pin). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1} or I_{DD2} and I_{AMP} when the programmable gain amplifier operates in an operation mode or the HALT mode.

6. Current flowing only to the comparator (AV_{REF} pin). The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1} or I_{DD2} and I_{CMP} when the comparator operates in an operation mode or the HALT mode.

7. Current flowing only to the LVI circuit. The current value of the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVI circuit operates in the Operating, HALT or STOP mode.

Remarks 1. f_{IL}: Internal low-speed oscillation clock frequency

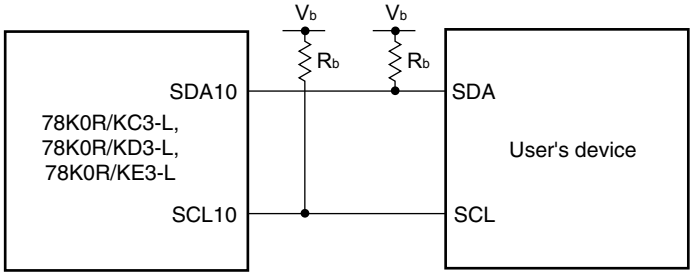
2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

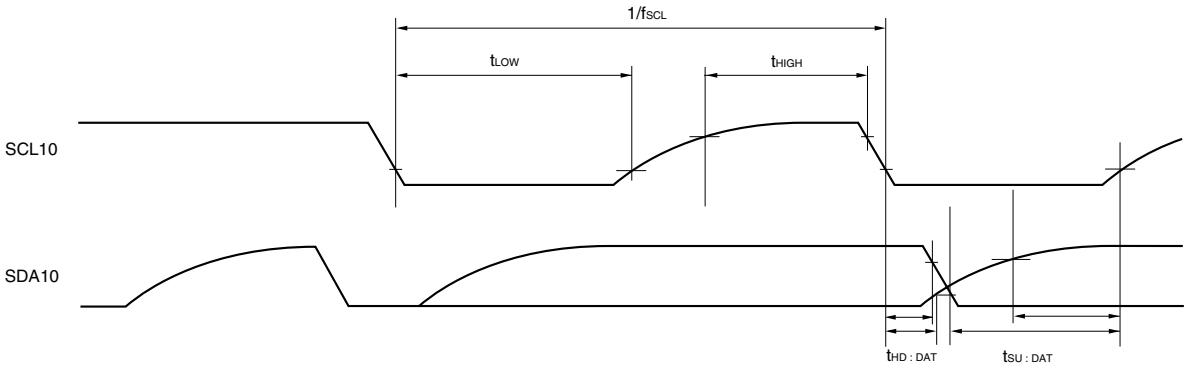
4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

Simplified I²C mode connection diagram (communication at different potential)



Simplified I²C mode serial transfer timing (communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDA10 pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCL10 pin by using port input mode register 3 (PIM3) and port output mode register 3 (POM3).

Remark R_b[Ω]:Communication line (SDA10, SCL10) pull-up resistance, V_b[V]: Communication line voltage

(4/7)

Edition	Description	Chapter
Previous version (U19291E) 3rd edition	Change of **Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Stopped Is Set (Option Byte: LVIOFF = 1))**	CHAPTER 5 CLOCK GENERATOR
	Change of **Figure 5-14. Clock Generator Operation When Power Supply Voltage Is Turned On (When LVI Default Start Function Enabled Is Set (Option Byte: LVIOFF = 0))**	
	Change of **5.6 Controlling Clock**	
	Addition of **Notes 3** and **4** to **5.6.6 CPU clock status transition diagram**	
	Change of **6.1.1 Independent channel operation function**	CHAPTER 6 TIMER ARRAY UNIT
	Change of **6.1.2 Simultaneous channel operation function**	
	Change of **Figure 6-1. Entire Configuration of Timer Array Unit TAUS**	
	Addition of **Figure 6-2. Internal Block Diagram of Channel of Timer Array Unit TAUS**	
	Change of **Figure 6-21. Format of Timer Output Mode Register 0 (TOM0)**	
	Change of **Figure 6-22. Format of Input Switch Control Register (ISC)**	
	Change of description of operation start in **Figure 6-39. Operation Procedure of Interval Timer/Square Wave Output Function**	
	Change of description in **6.7.2 Operation as external event counter**	
	Addition of **Caution** to **6.7.5 Operation as input signal high-/low-level width measurement**	
	Change of description in **6.8.2 Operation as PWM function**	
	Change of **Note** in **Figure 7-2. Format of Peripheral Enable Register 0 (PER0)**	CHAPTER 7 REAL-TIME COUNTER
	Addition of **Note** to **Figure 7-18. Procedure for Starting Operation of Real-Time Counter**	
	Change of **10.4.3 Setting window open period of watchdog timer** (deletion of window open period 25% setting)	CHAPTER 10 WATCHDOG TIMER
	Change of **Figure 11-5. A/D Converter Sampling and A/D Conversion Timing**	CHAPTER 11 A/D CONVERTER
	Change of description in **11.6 (9) Conversion results just after A/D conversion start**	
	Change of **Table 11-4. Resistance and Capacitance Values of Equivalent Circuit (Reference Values)**	
	Change of **Note 2** in **Figure 12-4. Format of Serial Clock Select Register 0 (SPS0)**	CHAPTER 12 SERIAL ARRAY UNIT
	Change of description of the MD0n0 bit in **Figure 12-5. Format of Serial Mode Register 0n (SMR0n) (2/2)**	
	Addition of **Note** to **Figure 12-6. Format of Serial Communication Operation Setting Register 0n (SCR0n) (2/3)**	
	Change of description in **12.3 (5) Higher 7 bits of the serial data register 0n (SDR0n)**	
	Change of **Figure 12-8. Format of Serial Flag Clear Trigger Register 0n (SIR0n)**	
	Change of **Figure 12-9. Format of Serial Status Register 0n (SSR0n)**	
	Change of **Figure 12-25. Procedure for Stopping Master Transmission**	
	Change of **Figure 12-27. Timing Chart of Master Transmission (in Single-Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	
	Change of **Figure 12-29. Timing Chart of Master Transmission (in Continuous Transmission Mode) (Type 1: DAP0n = 0, CKP0n = 0)**	