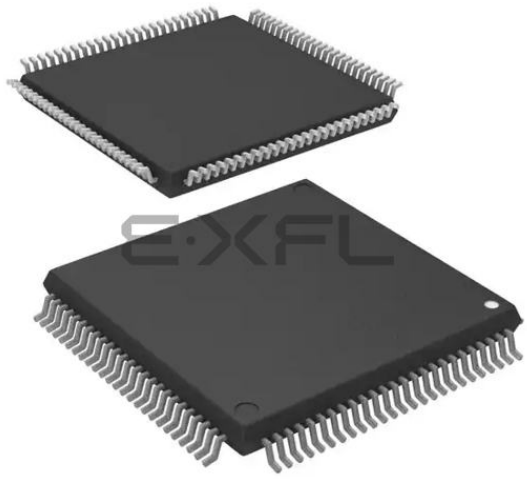
Renesas Electronics America Inc - UPD78F1013GF-GAS-AX Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1013gf-gas-ax

(1) Port functions (2/2): 78K0R/KD3-L

Function Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7. 8-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$
P76				KR6
P77				KR7
P80	I/O	Port 8. 4-bit I/O port. Inputs/output can be specified in 1-bit units. Inputs of P80 to P83 can be set as comparator inputs or programmable gain amplifier inputs.	Analog input	CMP0P/INTP3/ PGAI
P81				CMP0M
P82				CMP1P/INTP7
P83				CMP1M
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. For only P120, input/output can be specified in 1-bit units. For only P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1
P122				X2/EXCLK
P123				XT1
P124				XT2
P140	Output	Port 14. 1-bit output port.	Output port	PCLBUZ0
P150 to P152	I/O	Port 15. 3-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI8 to ANI10

2.2 Description of Pin Functions

Remark The pins mounted depend on the product. See **1.4 Pin Configuration (Top View)** and **2.1 Pin Function List**.

2.2.1 P00, P01 (port 0)

P00 and P01 function as an I/O port. These pins also function as timer I/O.

	78K0R/KC3-L (μPD78F100y: y = 0 to 3)		78K0R/KC3-L (48-pin) (μPD78F100y: y = 1 to 3)	78K0R/KD3-L (μPD78F100y: y = 4 to 6)	78K0R/KE3-L (μPD78F100y: y = 7 to 9)
	40-pin	44-pin			
P00/ TI00	–		–	√	√
P11/TO00	–		–	√	√

Remark √: Mounted

The following operation modes can be specified in 1-bit units.

(1) Port mode

P00 and P01 function as an I/O port. P00 and P01 can be set to input or output port in 1-bit units using port mode register 0 (PM0). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 0 (PU0).

(2) Control mode

P00 and P01 function as timer I/O.

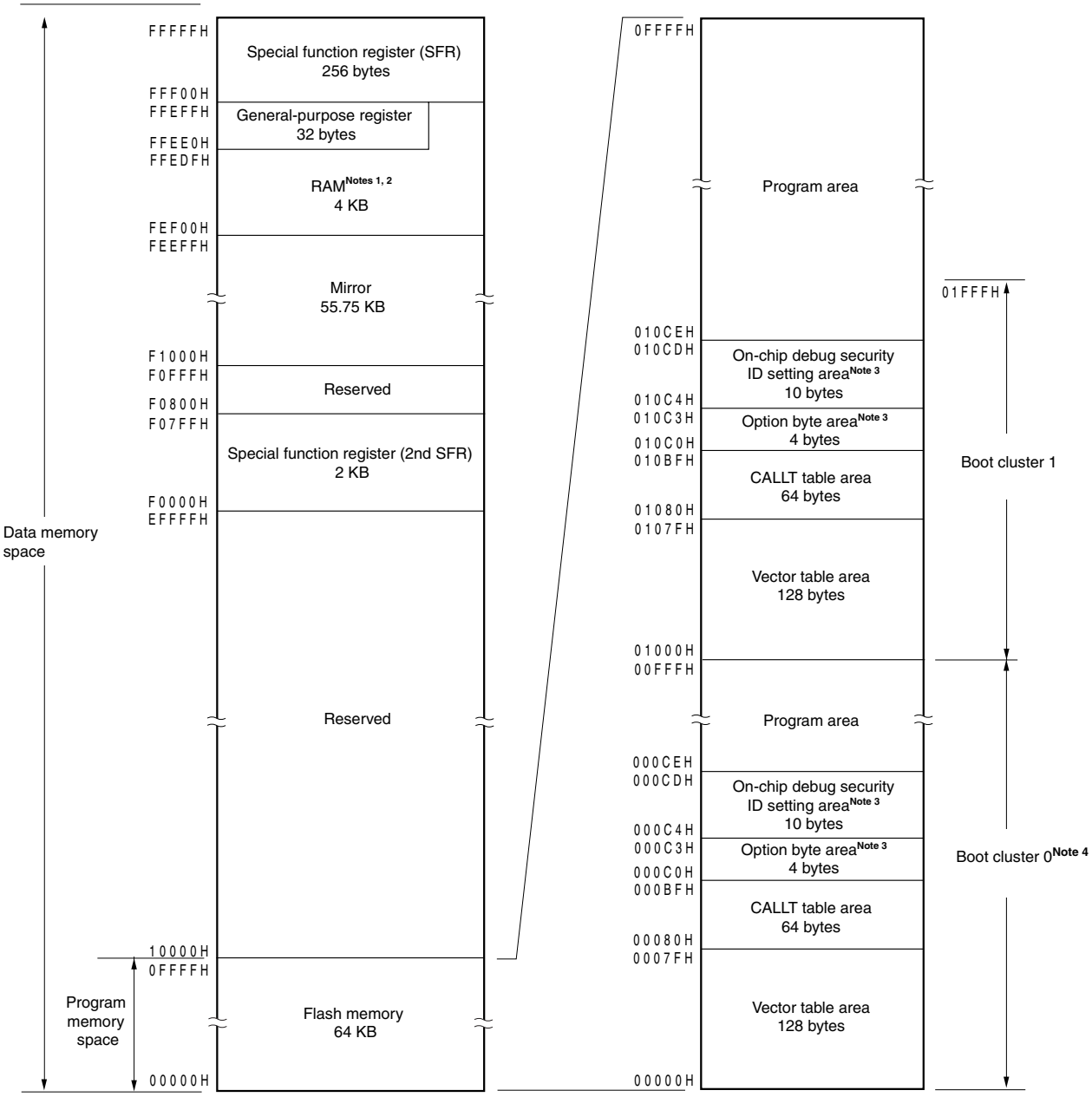
(a) TI00

This is the pin for inputting an external count clock/capture trigger to 16-bit timer 00.

(b) TO00

This is the timer output pin of 16-bit timer 00.

Figure 4-5. Memory Map (μPD78F1010)



Notes 1. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

2. Instructions can be executed from the RAM area excluding the general-purpose register area.

3. When boot swap is not used: Set the option bytes to 000C0H to 000C3H, and the on-chip debug security IDs to 000C4H to 000CDH.

When boot swap is used: Set the option bytes to 000C0H to 000C3H and 010C0H to 010C3H, and the on-chip debug security IDs to 000C4H to 000CDH and 010C4H to 010CDH.

4. Writing boot cluster 0 can be prohibited depending on the setting of security (see **26.7 Security Setting**).

Figure 4-43. Example of ES:[HL + byte], ES:[DE + byte]

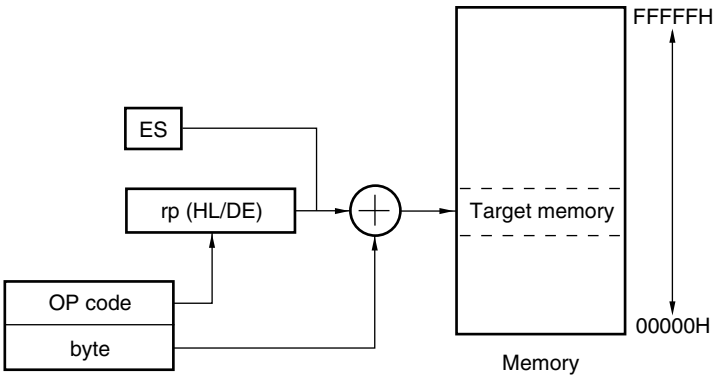


Figure 4-44. Example of ES:word[B], ES:word[C]

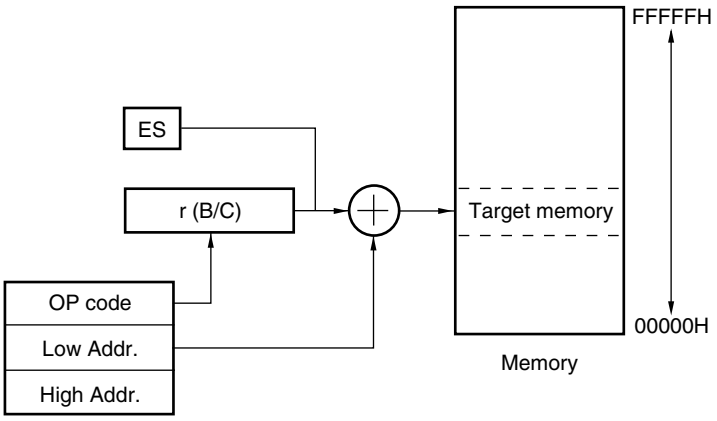


Figure 4-45. Example of ES:word[BC]

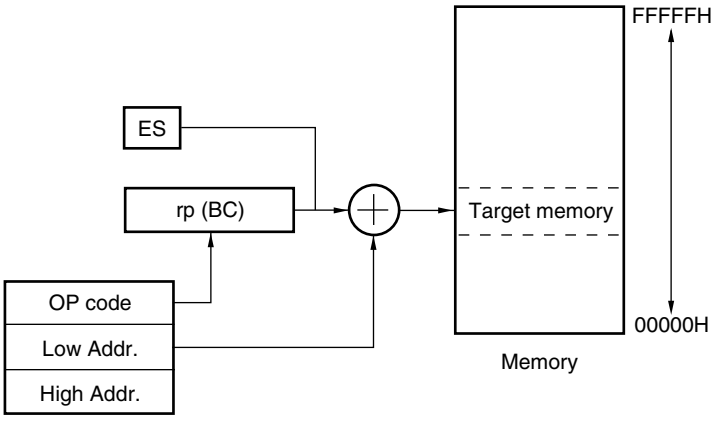
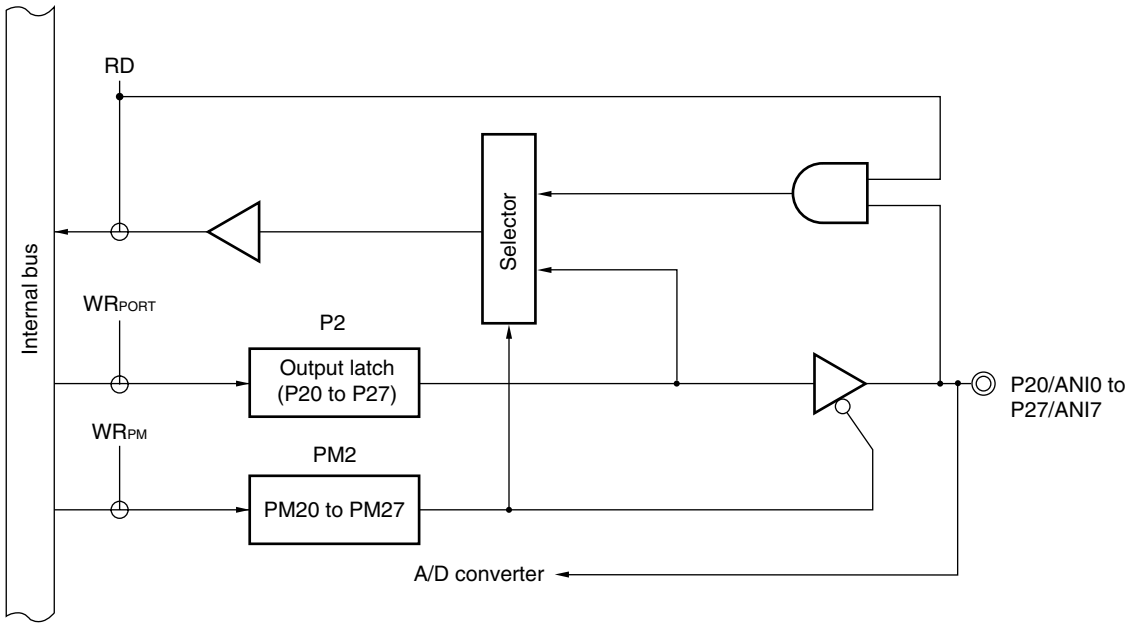
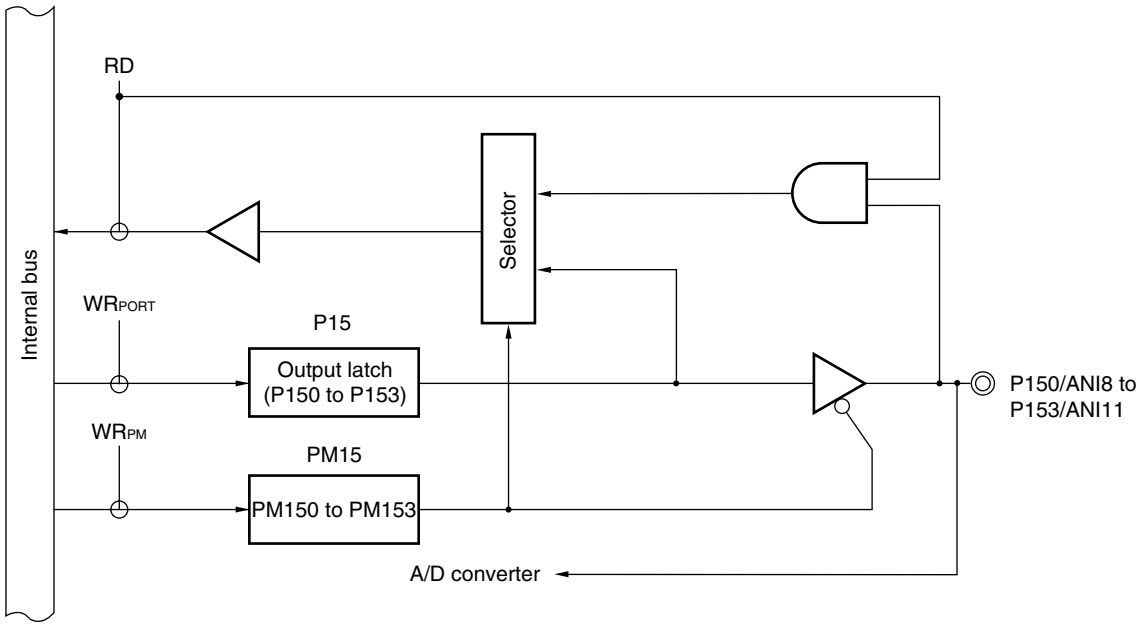


Figure 5-5. Block Diagram of P20 to P27



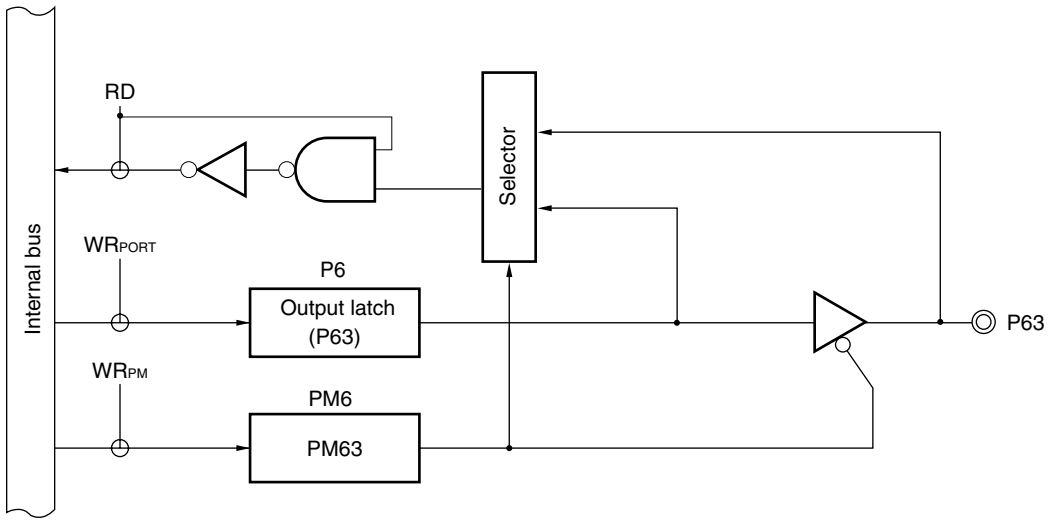
P2: Port register 2
PM2: Port mode register 2
RD: Read signal
WR××: Write signal

Figure 5-27. Block Diagram of P150 to P153



P15: Port register 15
PM15: Port mode register 15
RD: Read signal
WR××: Write signal

Figure 6-35. Block Diagram of P63



P6: Port register 6
PM6: Port mode register 6
RD: Read signal
WR××: Write signal

6.3 Registers Controlling Port Function

Port functions are controlled by the following six types of registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIM0, PIM1, PIM14)
- Port output mode registers (POM0, POM1, POM14)
- A/D port configuration register (ADPC)

(1) Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (FEH for PM13).

When port pins are used as alternate-function pins, set the port mode register by referencing **6.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function**.

Figure 6-52. Format of Port Mode Register (78K0R/KF3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM0	1	PM06	PM05	PM04	PM03	PM02	1	1	FFF20H	FFH	R/W
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	FFF21H	FFH	R/W
PM2	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	FFF22H	FFH	R/W
PM3	1	1	1	1	1	1	PM31	PM30	FFF23H	FFH	R/W
PM4	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	FFF24H	FFH	R/W
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50	FFF25H	FFH	R/W
PM6	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	FFF26H	FFH	R/W
PM7	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	FFF27H	FFH	R/W
PM9	1	1	1	1	1	1	PM91	PM90	FFF29H	FFH	R/W
PM11	1	1	1	1	1	1	PM111	PM110	FFF2BH	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FFF2CH	FFH	R/W
PM14	1	1	1	PM144	PM143	PM142	1	PM140	FFF2EH	FFH	R/W
PM15	1	1	1	1	PM153	PM152	PM151	PM150	FFF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 0 to 7, 9, 11, 12, 14, 15; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 0, 1 and 7 of the PM0 register, bits 2 to 7 of the PM3 register, bits 6 and 7 of the PM5 register, bits 2 to 7 of the PM9 register, bits 2 to 7 of the PM11 register, bits 1 to 7 of the PM12 register, bits 1 and 5 to 7 of the PM14 register, and bits 4 to 7 of the PM15 register to "1".

Figure 6-57. Format of Pull-up Resistor Option Register (78K0R/KG3-L)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00	F0030H	00H	R/W
PU1	PU17	PU16	PU15	PU14	PU13	PU12	PU11	PU10	F0031H	00H	R/W
PU3	0	0	0	0	0	0	PU31	PU30	F0033H	00H	R/W
PU4	PU47	PU46	PU45	PU44	PU43	PU42	PU41	PU40	F0034H	00H	R/W
PU5	PU57	PU56	PU55	PU54	PU53	PU52	PU51	PU50	F0035H	00H	R/W
PU6	PU67	PU66	PU65	PU64	0	0	0	0	F0036H	00H	R/W
PU7	PU77	PU76	PU75	PU74	PU73	PU72	PU71	PU70	F0037H	00H	R/W
PU8	PU87	PU86	PU85	PU84	PU83	PU82	PU81	PU80	F0038H	00H	R/W
PU9	0	0	0	0	0	0	PU91	0	F0039H	00H	R/W
PU11	0	0	0	0	0	0	PU111	PU110	F003BH	00H	R/W
PU12	0	0	0	0	0	0	0	PU120	F003CH	00H	R/W
PU13	0	0	0	0	0	0	PU131	0	F003DH	00H	R/W
PU14	0	0	PU145	PU144	PU143	PU142	PU141	PU140	F003EH	00H	R/W

PUmn	Pmn pin on-chip pull-up resistor selection (m = 0, 1, 3 to 9, 11 to 14; n = 0 to 7)
0	On-chip pull-up resistor not connected
1	On-chip pull-up resistor connected

Caution While timer output is enabled (TOEmn = 1), even if the output by timer interrupt of each timer (INTTMmn) contends with writing to the TOmn bit, output is normally done to the TOmn pin.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

8.5.5 Timer Interrupt and TOmn Pin Output at Operation Start

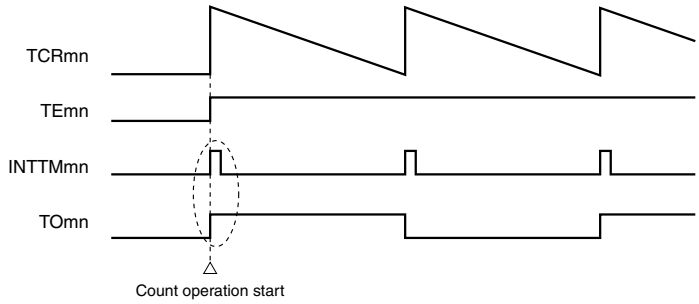
In the interval timer mode or capture mode, the MDmn0 bit in timer mode register mn (TMRmn) sets whether or not to generate a timer interrupt at count start.

When MDmn0 is set to 1, the count operation start timing can be known by the timer interrupt (INTTMmn) generation.

In the other modes, neither timer interrupt at count operation start nor TOmn output is controlled.

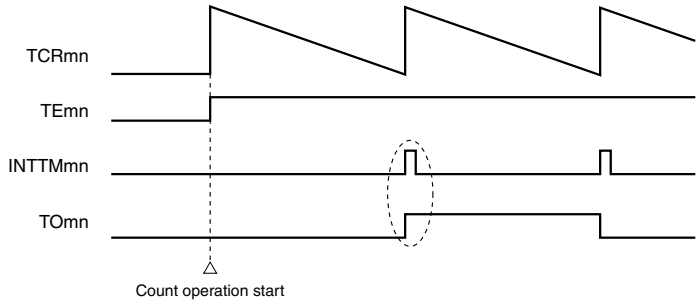
Figures 8-37 and 8-38 show operation examples when the interval timer mode (TOEmn = 1, TOMmn = 0) is set.

Figure 8-38. When MDmn0 is set to 1



When MDmn0 is set to 1, a timer interrupt (INTTMmn) is output at count operation start, and TOmn performs a toggle operation.

Figure 8-39. When MDmn0 is set to 0



When MDmn0 is set to 0, a timer interrupt (INTTMmn) is not output at count operation start, and TOmn does not change either. After counting one cycle, INTTMmn is output and TOmn performs a toggle operation.

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer output pin (TOmn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

13.6 Cautions for A/D Converter

(1) Operating current in STOP mode

Shift to STOP mode after stopping the A/D converter (by setting bit 7 (ADCS) of the A/D converter mode register (ADM) to 0). The operating current can be reduced by setting bit 0 (ADCE) of the ADM register to 0 at the same time. To restart from the standby status, clear bit 0 (ADIF) of interrupt request flag register 1L (IF1L) to 0 and start operation.

(2) Input range of ANI0 to ANI15 pins

Observe the rated range of the ANI0 to ANI15 pins input voltage. If a voltage of AV_{REF} or higher and AV_{SS} or lower (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

(3) Conflicting operations

<1> Conflict between the A/D conversion result register (ADCR, ADCRH) write and the ADCR or ADCRH register read by instruction upon the end of conversion

The ADCR or ADCRH register read has priority. After the read operation, the new conversion result is written to the ADCR or ADCRH registers.

<2> Conflict between the ADCR or ADCRH register write and the A/D converter mode register (ADM) write, the analog input channel specification register (ADS), or A/D port configuration register (ADPC) write upon the end of conversion

The ADM, ADS, or ADPC registers write has priority. The ADCR or ADCRH register write is not performed, nor is the conversion end interrupt signal (INTAD) generated.

(4) Noise countermeasures

To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REF} pin and ANI0 to ANI15 pins.

<1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

<2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external C as shown in Figure 13-22 is recommended.

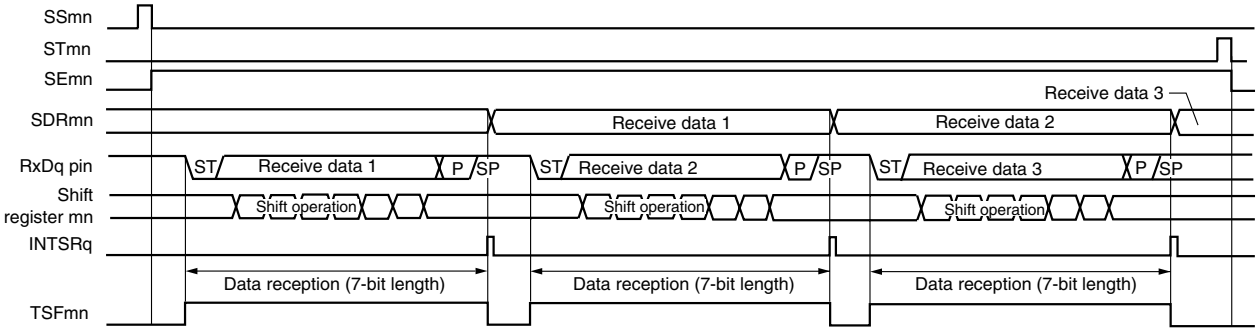
<3> Do not switch these pins with other pins during conversion.

<4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

Remark ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

(3) Processing flow

Figure 14-87. Timing Chart of UART Reception



Remark m: Unit number (m = 0 to 2), n: Channel number (n = 1, 3),
r: Channel number (r = n – 1), q: UART number (q = 0 to 4)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L:	mn = 01, 03, q = 0, 1
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012):	mn = 01, 03, 11, 13, q = 0 to 3
78K0R/KF3-L (μPD78F1027, 78F1028):	mn = 01, 03, 11, 13, 21, q = 0 to 4
78K0R/KG3-L (μPD78F1013, 78F1014):	mn = 01, 03, 11, 13, q = 0 to 3
78K0R/KG3-L (μPD78F1029, 78F1030):	mn = 01, 03, 11, 13, 21, q = 0 to 4

15.5.7 Canceling wait

The I^2C usually cancels a wait state by the following processing.

- Writing data to the IICA shift register (IICA)
- Setting bit 5 (WREL) of IICA control register 0 (IICCTL0) (canceling wait)
- Setting bit 1 (STT) of the IICCTL0 register (generating start condition)[Note]
- Setting bit 0 (SPT) of the IICCTL0 register (generating stop condition)[Note]

Note Master only

When the above wait canceling processing is executed, the I^2C cancels the wait state and communication is resumed.

To cancel a wait state and transmit data (including addresses), write the data to the IICA register.

To receive data after canceling a wait state, or to complete data transmission, set bit 5 (WREL) of the IICCTL0 register to 1.

To generate a restart condition after canceling a wait state, set bit 1 (STT) of the IICCTL0 register to 1.

To generate a stop condition after canceling a wait state, set bit 0 (SPT) of the IICCTL0 register to 1.

Execute the canceling processing only once for one wait state.

If, for example, data is written to the IICA register after canceling a wait state by setting the WREL bit to 1, an incorrect value may be output to SDA0 line because the timing for changing the SDA0 line conflicts with the timing for writing the IICA register.

In addition to the above, communication is stopped if the IICE bit is cleared to 0 when communication has been aborted, so that the wait state can be canceled.

If the I^2C bus has deadlocked due to noise, processing is saved from communication by setting bit 6 (LREL) of the IICCTL0 register, so that the wait state can be canceled.

Caution If a processing to cancel a wait state is executed when WUP = 1, the wait state will not be canceled.

CHAPTER 26 FLASH MEMORY

The 78K0R/Kx3-L incorporates the flash memory to which a program can be written, erased, and overwritten while mounted on the board.

26.1 Writing with Flash Memory Programmer

The following dedicated flash memory programmer can be used to write data to the internal flash memory of the 78K0R/Kx3-L.

- PG-FP5, FL-PR5
- QB-MINI2

Data can be written to the flash memory on-board or off-board, by using a dedicated flash memory programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the 78K0R/Kx3-L has been mounted on the target system. The connectors that connect the dedicated flash memory programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the 78K0R/Kx3-L is mounted on the target system.

Remark FL-PR5 and FA series are products of Naito Densei Machida Mfg. Co., Ltd.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, 1.8 V ≤ AV_{REF} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = – 3.0 mA	V_{DD} – 0.7			V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = –1.0 mA	V_{DD} – 0.5			V
	V_{OH2}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}, I_{OH2} = –0.1 mA	AV_{REF} – 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P130, P131, P140 to P145	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.0 mA			0.5	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = 0.5 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P157	AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 15.0 mA			2.0	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 5.0 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.4	V
			1.8 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 2.0 mA			0.4	V

Caution The maximum value of V_{IH} of pins P02 to P04, P10, P12, and P142 to P144 is V_{DD}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.

(5) Communication at different potential (2.5 V, 3 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} = EV_{DD0} = EV_{DD1} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V				f_{MCK}/6	bps
				f_{CLK} = 20 MHz, f_{MCK} = f_{CLK}			3.3	Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2, 4), g: PIM and POM number (g = 0, 1, 14)

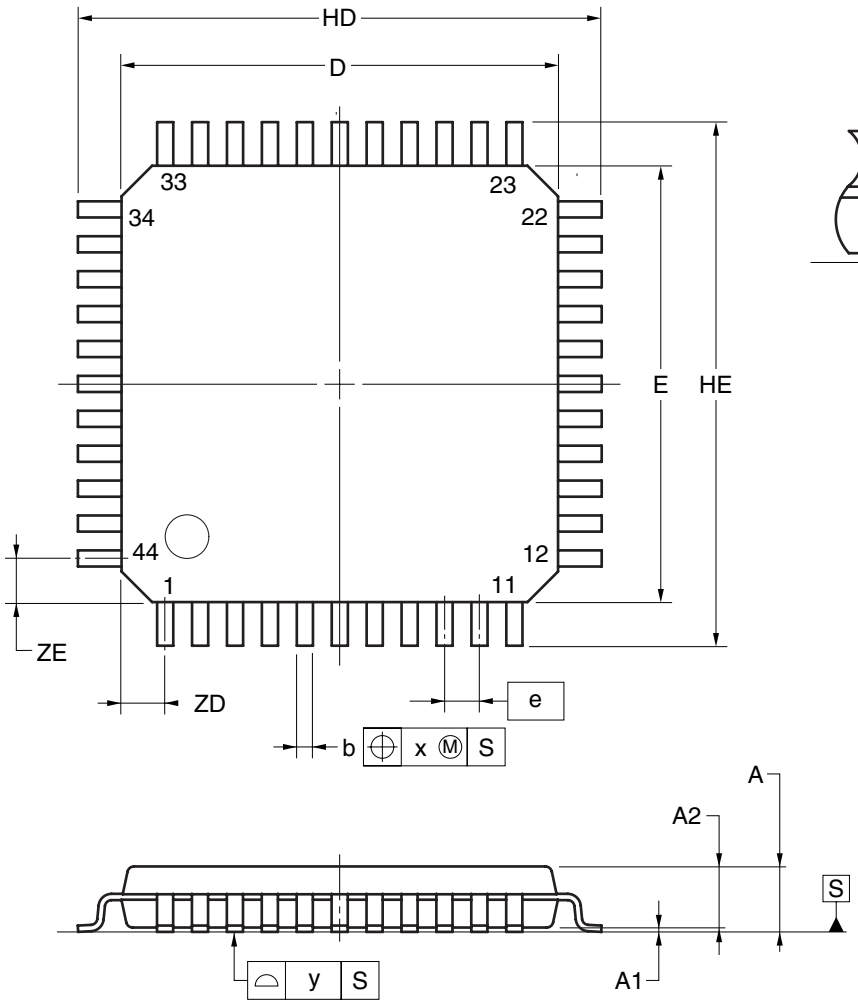
3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 3))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

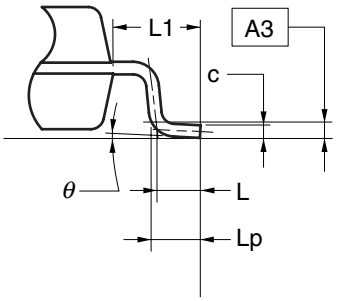
32.2 78K0R/KC3-L (44-pin products)

μPD78F1000GB-GAF-AX, 78F1001GB-GAF-AX, 78F1002GB-GAF-AX, 78F1003GB-GAF-AX

44-PIN PLASTIC LQFP (10x10)



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.35^{+0.08}_{-0.04}$
c	$0.125^{+0.075}_{-0.025}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.80
x	0.20
y	0.10
ZD	1.00
ZE	1.00

P44GB-80-GAF

NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

(2/6)

Edition	Description	Chapter
Current Version (U20024E) 1st edition	Change of **Figure 13-5. A/D Converter Sampling and A/D Conversion Timing**	CHAPTER 13 A/D CONVERTER
	Change of **Figure 13-12. Basic Operation of A/D Converter**	
	Change of **Figure 13-14. Example of Select Mode Operation Timing**	
	Change of **Figure 13-15. Example of Scan Mode Operation Timing**	
	Addition of **13.6 (12) Starting the A/D converter**	
	Addition of **Caution** to **14.3 (5) Higher 7 bits of the serial data register mn (SDRmn)**	CHAPTER 14 SERIAL ARRAY UNIT
	Change of **14.5.2 Master reception**	
	Change of **Figure 14-35. Example of Contents of Registers for Master Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20) (1/2)**	
	Addition of **14.5.2 (4) Processing flow (in continuous reception mode)**	
	Addition of **Caution** to **Figure 14-65. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20) (1/2)**	
	Addition of **Caution** to **Figure 14-66. Initial Setting Procedure for Slave Transmission/Reception**	
	Addition of **Caution** to **Figure 14-68. Procedure for Resuming Slave Transmission/Reception**	
	Addition of **Caution** to **Figure 14-70. Flowchart of Slave Transmission/Reception (in Single- Transmission/Reception Mode)**	
	Addition of **Caution** to **Figure 14-72. Flowchart of Slave Transmission/Reception (in Continuous Transmission/Reception Mode)**	
	Change of **14.8 Operation of Simplified I2C (IIC10, IIC20) Communication**	
	Change of **14.8.1 Address field transmission**	
	Change of **14.8.2 Data transmission**	
	Change of **14.8.3 Data reception**	
	Addition of **Caution**, and Change of **Remark** of **14.8.5 Calculating transfer rate**	
	Addition of **Figure 14-109. Processing Procedure in Case of Overrun Error**	
	Change of **15.6 Timing Charts**	CHAPTER 15 SERIAL INTERFACE IICA
	Addition of **Note** to **Figure 17-4. Format of DMA Mode Control Register n (DMCn) (1/2)**	CHAPTER 17 DMA CONTROLLER
	Change of description in **Figure 17-7. Example of Setting for CSI Consecutive Transmission**	
	Addition of description to **17.5.4 Holding DMA transfer pending by DWAITn bit**	
	Change of **Caution** in **17-11. Forced Termination of DMA Transfer (2/2)**	
	Change of **Caution 2** in **17.6 (2) DMA response time**	
	Change of **17.6 (4) DMA pending instruction**	
	Change of **18.5.4 Interrupt request hold**	CHAPTER 18 INTERRUPT FUNCTIONS
	Change of **Figure 20-4. HALT Mode Release by Reset**	CHAPTER 20 STANDBY FUNCTION
	Change of **Figure 20-5. STOP Mode Release by Interrupt Request Generation**	
	Change of **Figure 20-6. STOP Mode Release by Reset**	