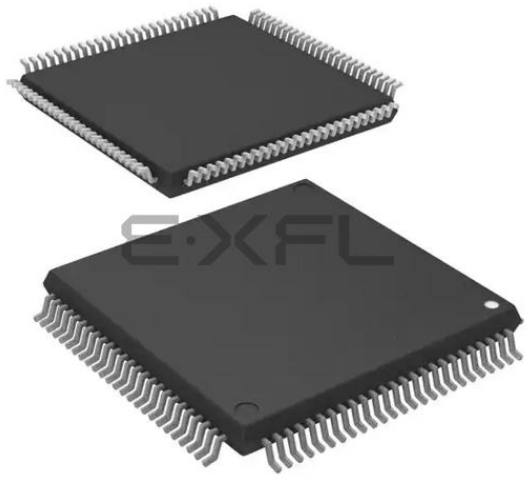
Renesas Electronics America Inc - UPD78F1014GC-UEU-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0R
Core Size	16-Bit
Speed	20MHz
Connectivity	3-Wire SIO, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1014gc-ueu-ax

2.1.1 78K0R/KC3-L (40-pin products)

(1) Port functions (1/2): 78K0R/KC3-L (40-pin)

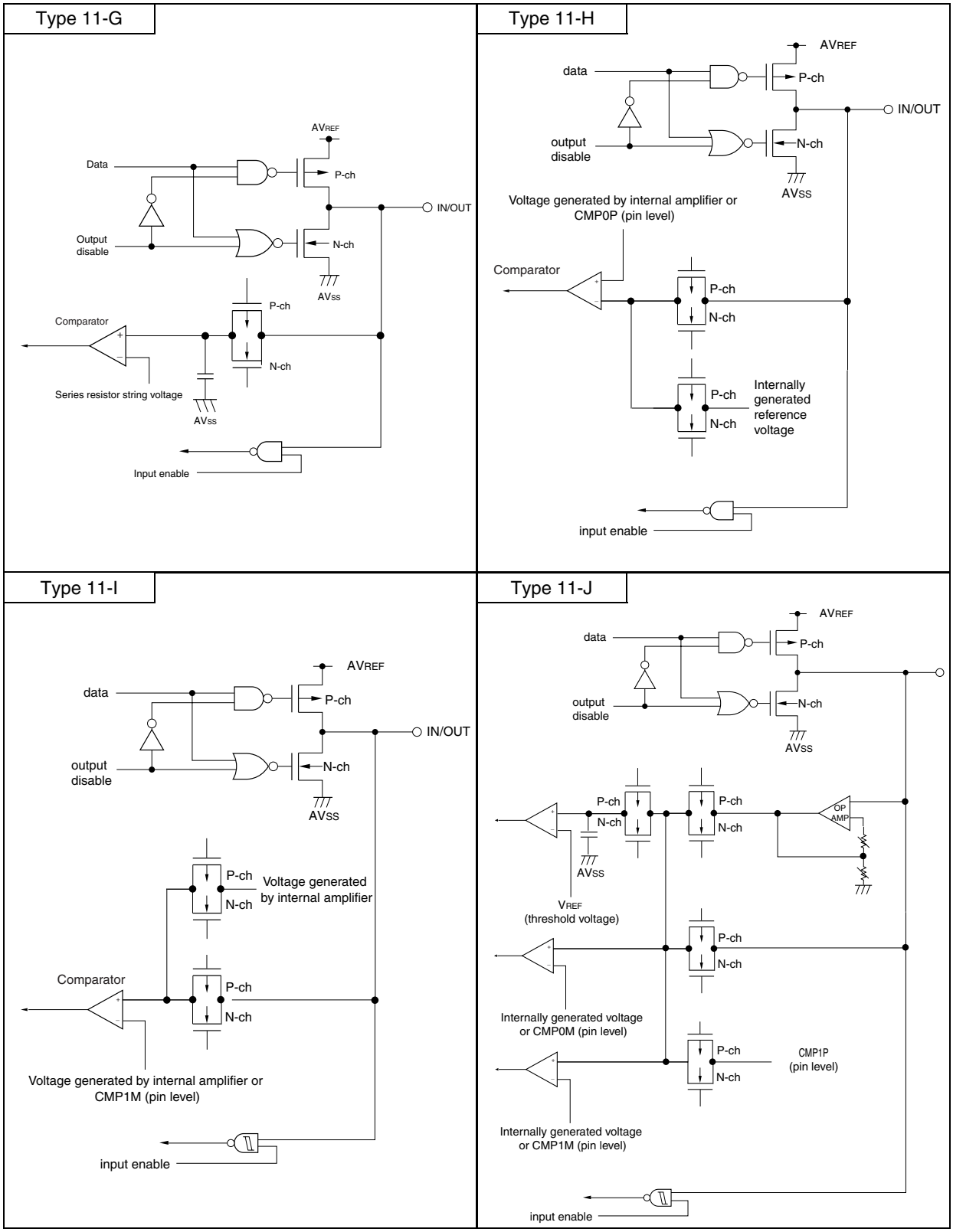
Function Name	I/O	Function	After Reset	Alternate Function
P10	I/O	Port 1. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI02/TO02
P11				TI03/TO03
P12				TI04/TO04
P13				TI05/TO05
P20 to P27	I/O	Port 2. 8-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	ANI0 to ANI7
P30	I/O	Port 3. 3-bit I/O port. Input of P31 and P32 can be set to TTL buffer. Output of P30 to P32 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SO10/TxD1
P31				SI10/RxD1/SDA10/INTP1
P32				$\overline{\text{SCK10}}$/SCL10/INTP2
P40[Note]	I/O	Port 4. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOOL0
P41				TOOL1
P50	I/O	Port 5. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TI06/TO06
P51				TI07/TO07
P70	I/O	Port 7. 6-bit I/O port. Input of P71, P72, P74, and P75 can be set to TTL buffer. Output of P70, P72, P73, and P75 can be set to N-ch open-drain output (V_{DD} tolerance). Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	KR0/SO01/INTP4
P71				KR1/SI01/INTP5
P72				KR2/$\overline{\text{SCK01}}$/INTP6
P73				KR3/SO00/TxD0
P74				KR4/SI00/RxD0
P75				KR5/$\overline{\text{SCK00}}$

Note If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

(2) Non-port functions (2/3): 78K0R/KE3-L

Function Name	I/O	Function	After Reset	Alternate Function
RxD0	Input	Serial data input to UART0	Input port	P74/KR4/SI00
RxD1		Serial data input to UART1		P31/SI10/SDA10/INTP1
$\overline{SCK00}$	I/O	Clock input/output for CSI00	Input port	P75/KR5
$\overline{SCK01}$		Clock input/output for CSI01		P72/KR2/INTP6
$\overline{SCK10}$		Clock input/output for CSI10		P32/SCL10/INTP2
SCL0	I/O	Clock input/output for I^2C	Input port	P60
SCL10	I/O	Clock input/output for simplified I^2C	Input port	P32/$\overline{SCK10}$/INTP2
SDA0	I/O	Serial data I/O for I^2C	Input port	P61
SDA10	I/O	Serial data I/O for simplified I^2C	Input port	P31/SI10/RxD1/INTP1
SI00	Input	Serial data input to CSI00	Input port	P74/KR4/RxD0
SI01		Serial data input to CSI01		P71/KR1/INTP5
SI10		Serial data input to CSI10		P31/RxD1/SDA10/INTP1
SLTI	Input	16-bit timer 00, 01 input	Input port	P52/RTC1HZ/SLTO
SLTO	Output	16-bit timer 00, 01 output	Input port	P52/RTC1HZ/SLTI
SO00	Output	Serial data output from CSI00	Input port	P73/KR3/TxD0
SO01		Serial data output from CSI01		P70/KR0/INTP4
SO10		Serial data output from CSI10		P30/TxD1
TI00	Input	External count clock input to 16-bit timer 00	Input port	P00
TI02		External count clock input to 16-bit timer 02		P10/TO02
TI03		External count clock input to 16-bit timer 03		P11/TO03
TI04		External count clock input to 16-bit timer 04		P12/TO04/RTCDIV/RTCCL
TI05		External count clock input to 16-bit timer 05		P13/TO05
TI06		External count clock input to 16-bit timer 06		P14/TO06
TI07		External count clock input to 16-bit timer 07		P15/TO07
TO00	Output	16-bit timer 00 output	Input port	P01
TO02		16-bit timer 02 output		P10/TI02
TO03		16-bit timer 03 output		P11/TI03
TO04		16-bit timer 04 output		P12/TI04/RTCDIV/RTCCL
TO05		16-bit timer 05 output		P13/TI05
TO06		16-bit timer 06 output		P14/TI06
TO07		16-bit timer 07 output		P15/TI07
TxD0	Output	Serial data output from UART0	Input port	P73/KR3/SO00
TxD1		Serial data output from UART1		P30/SO10
X1	–	Resonator connection for main system clock	Input port	P121
X2	–		Input port	P122/EXCLK
XT1	–	Resonator connection for subsystem clock	Input port	P123
XT2	–		Input port	P124
EXCLK	Input	External clock input for main system clock	Input port	P122/X2

Figure 2-1. Pin I/O Circuit List (2/3)



3.2.10 P90, P91 (port 9)

P90 and P91 function as an I/O port.

P90 and P91 can be set to input or output port in 1-bit units using port mode register 9 (PM9). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 9 (PU9).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P90	√	–
P91	√	√

3.2.11 P110, P111 (port 11)

P110 and P111 function as an I/O port.

P110 and P111 can be set to input or output port in 1-bit units using port mode register 11 (PM11). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 11 (PU11).

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P110	√	√
P111	√	√

3.2.12 P120 to P124 (port 12)

P120 function as a 1-bit I/O port. P121 to P124 functions as a 4-bit input port. These pins also function as external interrupt request input, potential input for external low-voltage detection, connecting resonator for main system clock, connecting resonator for subsystem clock, and external clock input for main system clock.

	78K0R/KF3-L (μPD78F10xx: xx = 10, 11, 12, 27, 28)	78K0R/KG3-L (μPD78F10xx: xx = 13, 14, 29, 30)
P120/INTP0/EXLVI	√	√
P121/X1	√	√
P122/X2/EXCLK	√	√
P123/XT1	√	√
P124/XT2	√	√

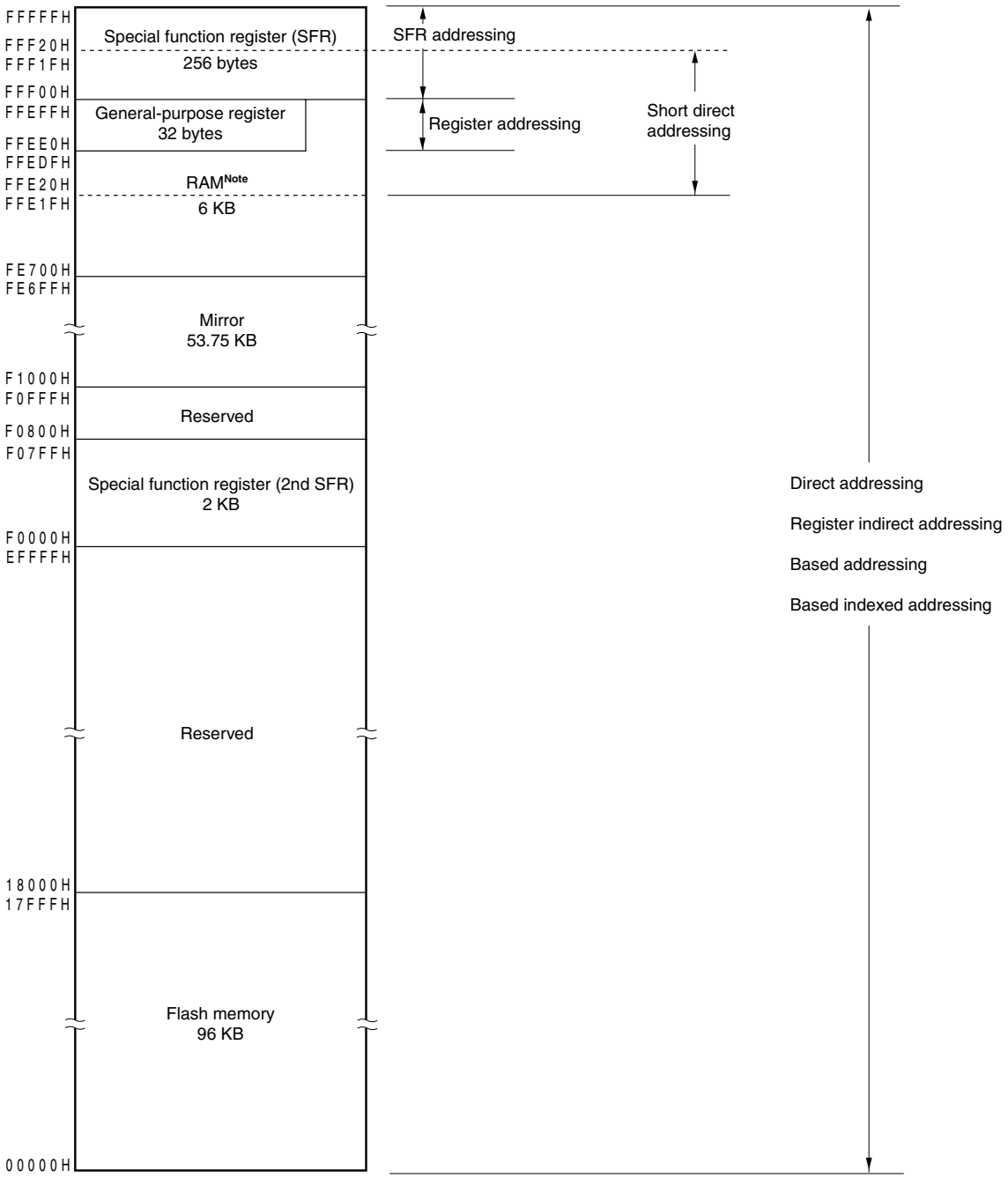
The following operation modes can be specified in 1-bit units.

(1) Port mode

P120 functions as a 1-bit I/O port. P120 can be set to input or output port using port mode register 12 (PM12). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 12 (PU12).

P121 to P124 functions as a 4-bit input port.

Figure 4-16. Correspondence Between Data Memory and Addressing (μPD78F1011, 78F1013)



Note While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory.

(d) Auxiliary carry flag (AC)

If the operation result has a carry from bit 3 or a borrow at bit 3, this flag is set (1). It is reset (0) in all other cases.

(e) In-service priority flags (ISP1, ISP0)

This flag manages the priority of acknowledgeable maskable vectored interrupts. Vectored interrupt requests specified lower than the value of ISP0 and ISP1 flags by the priority specification flag registers (PRn0L, PRn0H, PRn1L, PRn1H, PRn2L, PRn2H) (see **18.3 (3)**) can not be acknowledged. Actual request acknowledgment is controlled by the interrupt enable flag (IE).

Remark n = 0, 1

(f) Carry flag (CY)

This flag stores overflow and underflow upon add/subtract instruction execution. It stores the shift-out value upon rotate instruction execution and functions as a bit accumulator during bit operation instruction execution.

(3) Stack pointer (SP)

This is a 16-bit register to hold the start address of the memory stack area. Only the internal RAM area can be set as the stack area.

Figure 4-22. Format of Stack Pointer

	15															0
SP	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0

The SP is decremented ahead of write (save) to the stack memory and is incremented after read (restored) from the stack memory.

Each stack operation saves data as shown in Figure 4-19.

Caution 1. Since reset signal generation makes the SP contents undefined, be sure to initialize the SP before using the stack.

2. It is prohibited to use the general-purpose register (FFEE0H to FFEFFH) space as a stack area.

3. While using the self-programming function, the area FFE20H to FFEFFH cannot be used as stack memory. Furthermore, the areas of FF300H to FF6FFH and FDF00H to FE2FFH also cannot be used with the μPD78F1003, 78F1006 and 78F1009, and μPD78F1012 and 78F1014, 78F1027, 78F1028, 78F1029, and 78F1030, respectively.

Table 4-6. Extended SFR (2nd SFR) List (6/8)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset	KC3-L (40-pin)	KC3-L (44-pin)	KC3-L (48-pin)	KD3-L	KE3-L	KF3-L	KG3-L
					1-bit	8-bit	16-bit								
F01B6H	Timer clock select register 0	TPS0L	TPS0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01B7H		–			–	–			√	√	√	√	√	√	√
F01B8H	Timer output register 0	TO0L	TO0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01B9H		–			–	–			√	√	√	√	√	√	√
F01BAH	Timer output enable register 0	TOE0L	TOE0	R/W	√	√	√	0000H	√	√	√	√	√	√	√
F01BBH		–			–	–			√	√	√	√	√	√	√
F01BCH	Timer output level register 0	TOL0L	TOL0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01BDH		–			–	–			√	√	√	√	√	√	√
F01BEH	Timer output mode register 0	TOM0L	TOM0	R/W	–	√	√	0000H	√	√	√	√	√	√	√
F01BFH		–			–	–			√	√	√	√	√	√	√
F01C0H	Timer counter register 10	TCR10		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C1H															
F01C2H	Timer counter register 11	TCR11		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C3H															
F01C4H	Timer counter register 12	TCR12		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C5H															
F01C6H	Timer counter register 13	TCR13		R	–	–	√	FFFFH	–	–	–	–	–	√	√
F01C7H															
F01C8H	Timer mode register 10	TMR10		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01C9H															
F01CAH	Timer mode register 11	TMR11		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01CBH															
F01CCH	Timer mode register 12	TMR12		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01CDH															
F01CEH	Timer mode register 13	TMR13		R/W	–	–	√	0000H	–	–	–	–	–	√	√
F01CFH															
F01D0H	Timer status register 10	TSR10L	TSR10	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D1H		–			–	–			–	–	–	–	–	√	√
F01D2H	Timer status register 11	TSR11L	TSR11	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D3H		–			–	–			–	–	–	–	–	√	√
F01D4H	Timer status register 12	TSR12L	TSR12	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D5H		–			–	–			–	–	–	–	–	√	√
F01D6H	Timer status register 13	TSR13L	TSR13	R	–	√	√	0000H	–	–	–	–	–	√	√
F01D7H		–			–	–			–	–	–	–	–	√	√
F01D8H	Timer channel enable status register 1	TE1L	TE1	R	√	√	√	0000H	–	–	–	–	–	√	√
F01D9H		–			–	–			–	–	–	–	–	√	√
F01DAH	Timer channel start register 1	TS1L	TS1	R/W	√	√	√	0000H	–	–	–	–	–	√	√
F01DBH		–			–	–			–	–	–	–	–	√	√

Figure 4-43. Example of ES:[HL + byte], ES:[DE + byte]

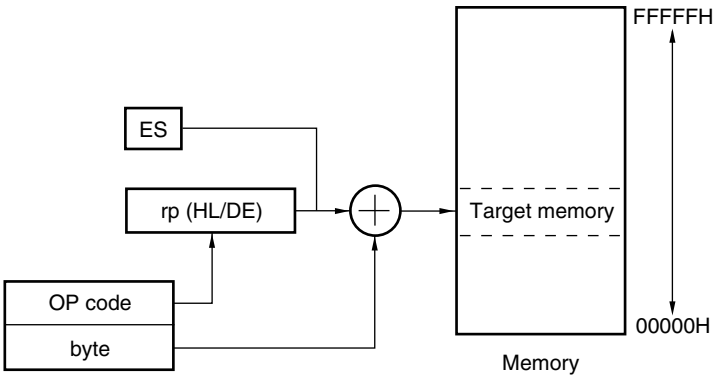


Figure 4-44. Example of ES:word[B], ES:word[C]

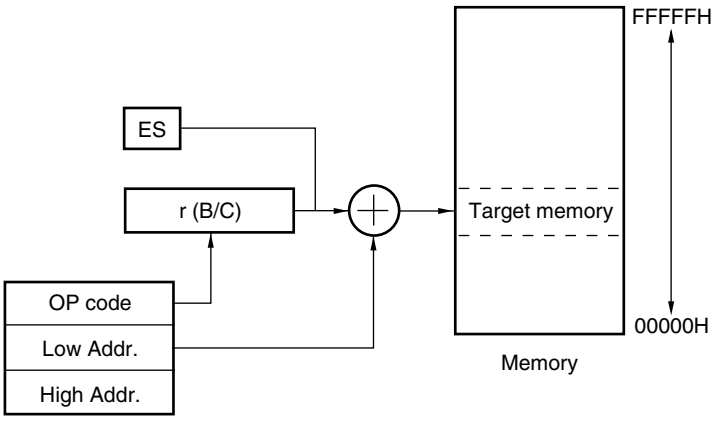
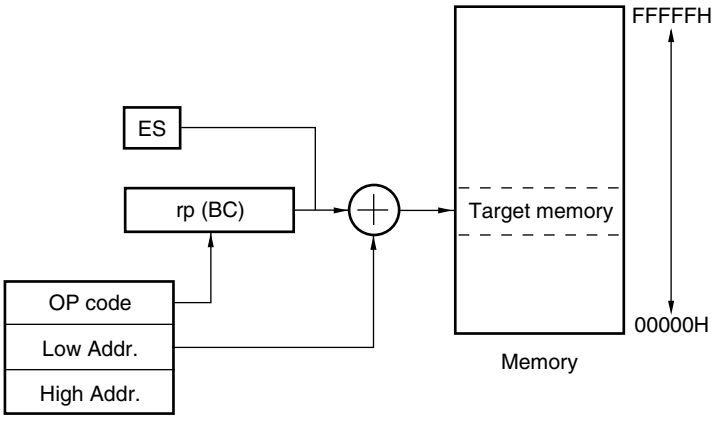


Figure 4-45. Example of ES:word[BC]



6.3 Registers Controlling Port Function

Port functions are controlled by the following six types of registers.

- Port mode registers (PMxx)
- Port registers (Pxx)
- Pull-up resistor option registers (PUxx)
- Port input mode registers (PIM0, PIM1, PIM14)
- Port output mode registers (POM0, POM1, POM14)
- A/D port configuration register (ADPC)

(1) Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH (FEH for PM13).

When port pins are used as alternate-function pins, set the port mode register by referencing **6.5 Settings of Port Mode Register, and Output Latch When Using Alternate Function**.

Figure 8-29. Format of Port Mode Registers 0, 1, 5 (PM0, PM1, PM5) (78K0R/KE3-L)

Address: FFF20H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM0	1	1	1	1	1	1	PM01	PM00

Address: FFF21H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM1	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10

Address: FFF25H After reset: FFH R/W

Symbol	7	6	5	4	3	2	1	0
PM5	1	1	1	1	PM53	PM52	PM51	PM50

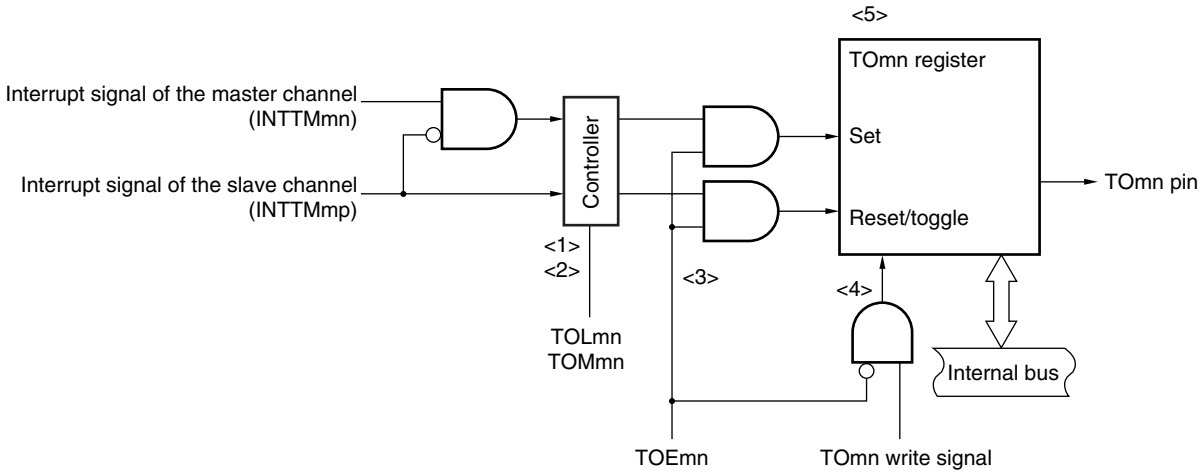
PMmn	Pmn pin I/O mode selection (m = 0, 1, 5; n = 0 to 7)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode registers 0, 1, and 5 of the 78K0R/KE3-L product. See below for the format of the port mode register of other products.
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: 5.3 (1) Port mode registers (PMxx).
78K0R/KF3-L, 78K0R/KG3-L: 6.3 (1) Port mode registers (PMxx).

8.5 Channel Output (TOmn pin) Control

8.5.1 TOmn pin output circuit configuration

Figure 8-30. Output Circuit Configuration



The following describes the TOmn pin output circuit.

<1> When TOMmn = 0 (master channel output mode), the set value of timer output level register m (TOLm) is ignored and only INTTMmp (slave channel timer interrupt) is transmitted to timer output register m (TOm).

<2> When TOMmn = 1 (slave channel output mode), both INTTMmn (master channel timer interrupt) and INTTMmp (slave channel timer interrupt) are transmitted to the TOm register.
At this time, the TOLm register becomes valid and the signals are controlled as follows:

When TOLmn = 0:	Forward operation (INTTMmn → set, INTTMmp → reset)
When TOLmn = 1:	Reverse operation (INTTMmn → reset, INTTMmp → set)

When INTTMmn and INTTMmp are simultaneously generated, (0% output of PWM), INTTMmp (reset signal) takes priority, and INTTMmn (set signal) is masked.

<3> While timer output is enabled (TOEmn = 1), INTTMmn (master channel timer interrupt) and INTTMmp (slave channel timer interrupt) are transmitted to the TOm register. Writing to the TOm register (TOmn write signal) becomes invalid.
When TOEmn = 1, the TOmn pin output never changes with signals other than interrupt signals.
To initialize the TOmn pin output level, it is necessary to set timer operation is stopeed (TOEmn = 0) and to write a value to the TOm register.

<4> While timer output is disabeled (TOEmn = 0), writing to the TOmn bit to the target channel (TOmn write signal) becomes valid. When timer output is disabeled (TOEmn = 0), neither INTTMmn (master channel timer interrupt) nor INTTMmp (slave channel timer interrupt) is transmitted to the TOm register.

<5> The TOm register can always be read, and the TOmn pin output level can be checked.

(**Remark** is listed on the next page.)

11.4 Operations of Clock Output/Buzzer Output Controller

One pin can be used to output a clock or buzzer sound.

The PCLBUZ0 pin outputs a clock/buzzer selected by the clock output select register 0 (CKS0).

The PCLBUZ1 pin outputs a clock/buzzer selected by the clock output select register 1 (CKS1).

11.4.1 Operation as output pin

The PCLBUZn pin is output as the following procedure.

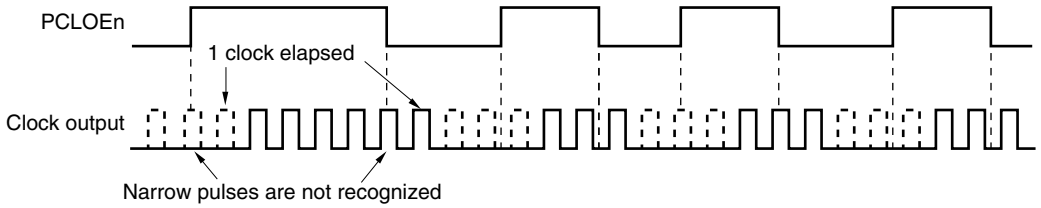
<1> Select the output frequency with bits 0 to 3 (CCSn0 to CCSn2, CSELn) of the clock output select register (CKSn) of the PCLBUZn pin (output in disabled status).

<2> Set bit 7 (PCLOEn) of the CKSn register to 1 to enable clock/buzzer output.

Remarks 1. The controller used for outputting the clock starts or stops outputting the clock one clock after enabling or disabling clock output (PCLOEn bit) is switched. At this time, pulses with a narrow width are not output. Figure 11-4 shows enabling or stopping output using the PCLOEn bit and the timing of outputting the clock.

2. n = 0: 78K0R/KC3-L (48-pin), 78K0R/KD3-L
n = 0, 1: 78K0R/KE3-L, 78K0R/KF3-L, 78K0R/KG3-L

Figure 11-4. Remote Control Output Application Example



14.5.5 Slave reception

Slave reception is that the 78K0R/Kx3-L receives data from another device in the state of a transfer clock being input from another device.

3-Wire Serial I/O	CSI00	CSI01	CSI10	CSI20 Note 1	CSI40 Note 2	CSI41 Note 2
Target channel	Channel 0 of SAU0	Channel 1 of SAU0	Channel 2 of SAU0	Channel 0 of SAU1	Channel 0 of SAU2	Channel 1 of SAU2
Pins used	$\overline{SCK00}$, SI00	$\overline{SCK01}$, SI01	$\overline{SCK10}$, SI10	$\overline{SCK20}$, SI20	$\overline{SCK40}$, SI40	$\overline{SCK41}$, SI41
Interrupt	INTCSI00	INTCSI01	INTCSI10	INTCSI20	INTCSI40	INTCSI41
	Transfer end interrupt only (Setting the buffer empty interrupt is prohibited.)					
Error detection flag	Overrun error detection flag (OVFmn) only					
Transfer data length	7 or 8 bits					
Transfer rate	Max. f_{MCK}/6 [Hz] Notes 3, 4					
Data phase	Selectable by the DAPmn bit of the SCRmn register • DAPmn = 0: Data input starts from the start of the operation of the serial clock. • DAPmn = 1: Data input starts half a clock before the start of the serial clock operation.					
Clock phase	Selectable by the CKPmn bit of the SCRmn register • CKPmn = 0: Forward • CKPmn = 1: Reverse					
Data direction	MSB or LSB first					

Notes 1. 78K0R/KF3-L, 78K0R/KG3-L only.

2. CSI40 and CSI41 are only mounted in the 78K0R/KF3-L (μPD78F1027, 78F1028) and 78K0R/KG3-L (μPD78F1029, 78F1030).

3. Because the external serial clock input to the $\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCK10}$, $\overline{SCK20}$, $\overline{SCK40}$, and $\overline{SCK41}$ pins is sampled internally and used, the fastest transfer rate is the f_{MCK}/6 [Hz] .

4. Use this operation within a range that satisfies the conditions above and the AC characteristics in the electrical specifications (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

Remarks 1. f_{MCK}: Operation clock frequency of target channel

2. m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2)
78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02
78K0R/KF3-L (μPD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10
78K0R/KF3-L (μPD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21
78K0R/KG3-L (μPD78F1013, 78F1014): mn = 00 to 02, 10
78K0R/KG3-L (μPD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21

14.8.5 Calculating transfer rate

The transfer rate for simplified I^2C (IIC10, IIC20) communication can be calculated by the following expressions.

(Transfer rate) = {Operation clock (f_{MCK}) frequency of target channel} ÷ (SDRmn[15:9] + 1) ÷ 2

Caution Setting SDRmn[15:9] = 0000000B is prohibited. Setting SDRmn[15:9] = 0000001B or more.

Remarks 1. The value of SDRmn[15:9] is the value of bits 15 to 9 of the SDRmn register (0000001B to 1111111B) and therefore is 1 to 127.

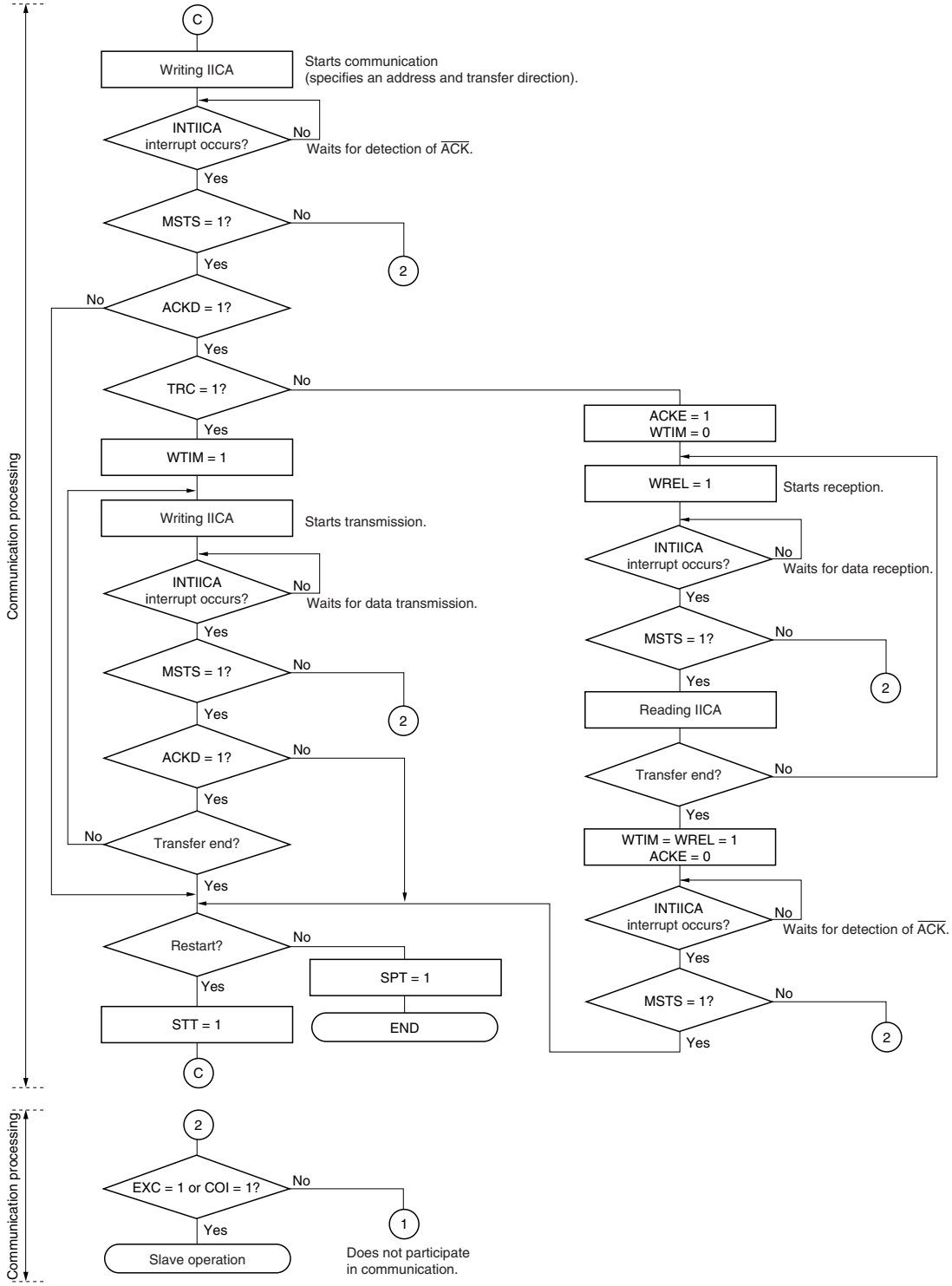
2. m: Unit number (m = 0, 1), n: Channel number (n = 0, 2)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 02

78K0R/KF3-L, 78K0R/KG3-L: mn = 02, 10

The operation clock (f_{MCK}) is determined by serial clock select register m (SPSm) and bit 15 (CKSmn) of serial mode register mn (SMRmn).

Figure 15-29. Master Operation in Multi-Master System (3/3)



Remarks 1. Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

2. To use the device as a master in a multi-master system, read the MSTS bit each time interrupt INTIICA has occurred to check the arbitration result.

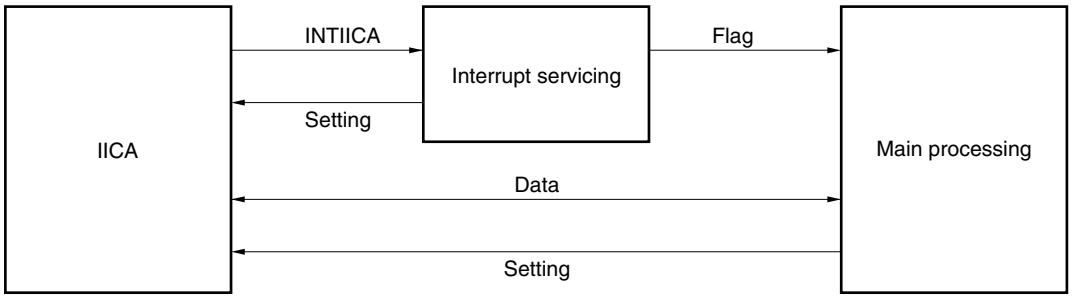
3. To use the device as a slave in a multi-master system, check the status by using the IICA status register (IICS) and IICA flag register (IICF) each time interrupt INTIICA has occurred, and determine the processing to be performed next.

(3) Slave operation

The processing procedure of the slave operation is as follows.

Basically, the slave operation is event-driven. Therefore, processing by the INTIICA interrupt (processing that must substantially change the operation status such as detection of a stop condition during communication) is necessary.

In the following explanation, it is assumed that the extension code is not supported for data communication. It is also assumed that the INTIICA interrupt servicing only performs status transition processing, and that actual data communication is performed by the main processing.



Therefore, data communication processing is performed by preparing the following three flags and passing them to the main processing instead of INTIICA.

<1> Communication mode flag

This flag indicates the following two communication statuses.

- Clear mode: Status in which data communication is not performed
- Communication mode: Status in which data communication is performed (from valid address detection to stop condition detection, no detection of $\overline{\text{ACK}}$ from master, address mismatch)

<2> Ready flag

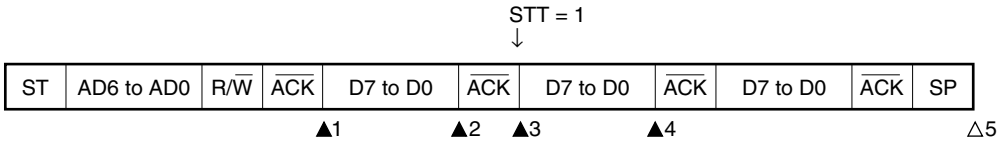
This flag indicates that data communication is enabled. Its function is the same as the INTIICA interrupt for ordinary data communication. This flag is set by interrupt servicing and cleared by the main processing. Clear this flag by interrupt servicing when communication is started. However, the ready flag is not set by interrupt servicing when the first data is transmitted. Therefore, the first data is transmitted without the flag being cleared (an address match is interpreted as a request for the next data).

<3> Communication direction flag

This flag indicates the direction of communication. Its value is the same as the TRC bit.

(f) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

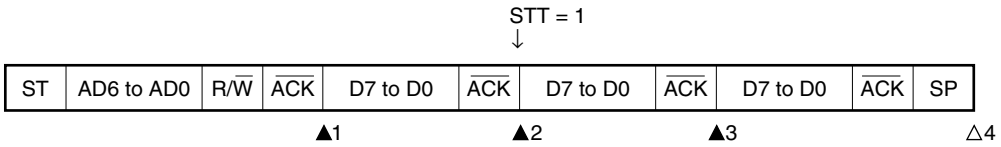
(i) When WTIM = 0



▲1: IICS = 1000×110B
▲2: IICS = 1000×000B (Sets the WTIM bit to 1)
▲3: IICS = 1000×100B (Clears the WTIM bit to 0)
▲4: IICS = 01000000B
△5: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

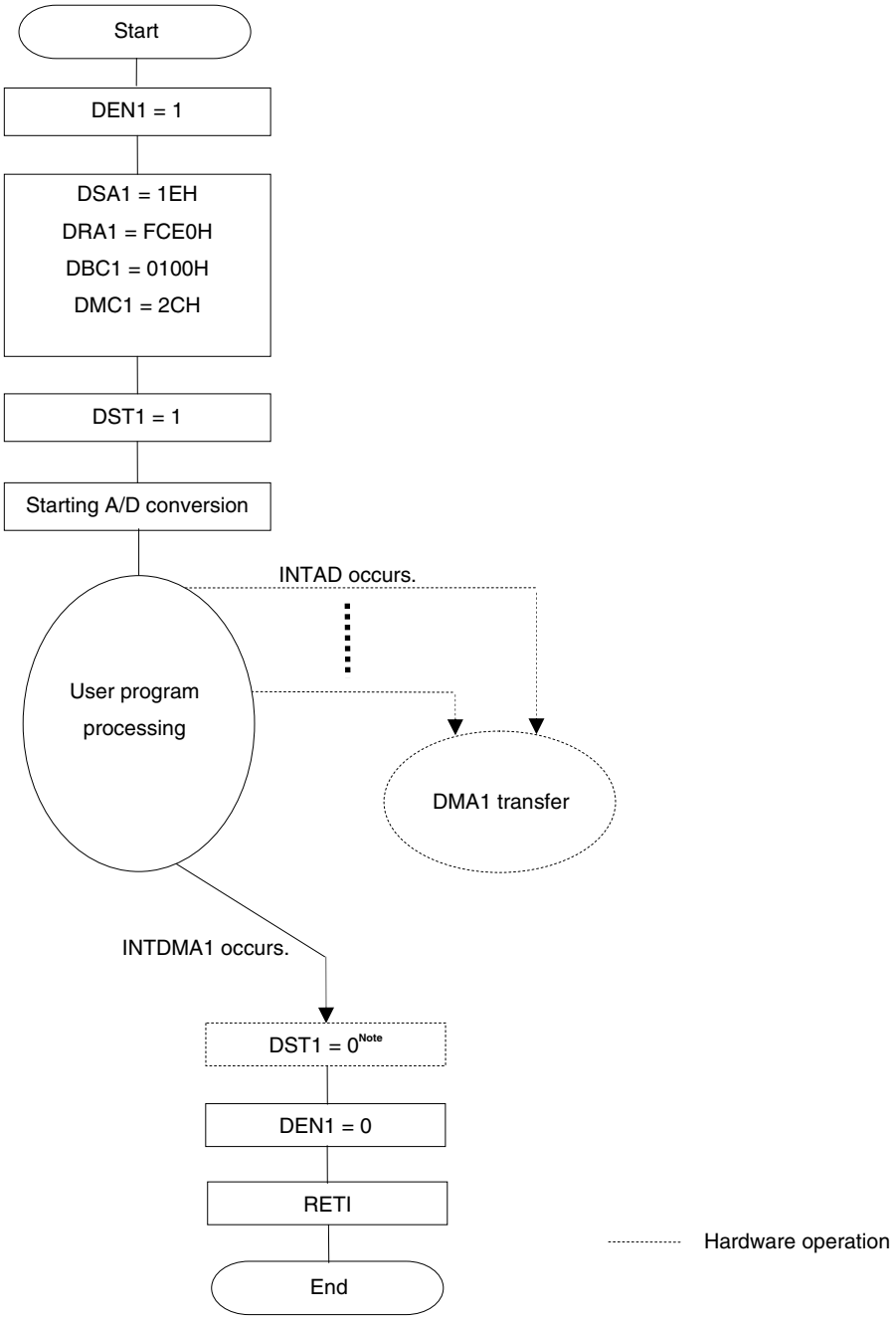
(ii) When WTIM = 1



▲1: IICS = 1000×110B
▲2: IICS = 1000×100B (Sets the STT bit to 1)
▲3: IICS = 01000100B
△4: IICS = 00000001B

Remark ▲: Always generated
△: Generated only when SPIE = 1
×: Don't care

Figure 17-8. Example of Setting of Consecutively Capturing A/D Conversion Results



Note The DST1 flag is automatically cleared to 0 when a DMA transfer is completed.
Writing the DEN1 flag is enabled only when DST1 = 0. To terminate a DMA transfer without waiting for occurrence of the interrupt of DMA1 (INTDMA1), set the DST1 bit to 0 and then the DEN1 bit to 0 (for details, refer to **17.5.5 Forced termination by software**).

Table 29-5. Operation List (14/17)

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag		
				Note 1	Note 2		Z	AC	CY
Bit manipulate	XOR1	CY, saddr.bit	3	1	–	CY ← CY ⊻ (saddr).bit			×
		CY, sfr.bit	3	1	–	CY ← CY ⊻ sfr.bit			×
		CY, A.bit	2	1	–	CY ← CY ⊻ A.bit			×
		CY, PSW.bit	3	1	–	CY ← CY ⊻ PSW.bit			×
		CY, [HL].bit	2	1	4	CY ← CY ⊻ (HL).bit			×
		CY, ES:[HL].bit	3	2	5	CY ← CY ⊻ (ES, HL).bit			×
	SET1	saddr.bit	3	2	–	(saddr).bit ← 1			
		sfr.bit	3	2	–	sfr.bit ← 1			
		A.bit	2	1	–	A.bit ← 1			
		!addr16.bit	4	2	–	(addr16).bit ← 1			
		PSW.bit	3	4	–	PSW.bit ← 1	×	×	×
		[HL].bit	2	2	–	(HL).bit ← 1			
		ES:!addr16.bit	5	3	–	(ES, addr16).bit ← 1			
		ES:[HL].bit	3	3	–	(ES, HL).bit ← 1			
	CLR1	saddr.bit	3	2	–	(saddr.bit) ← 0			
		sfr.bit	3	2	–	sfr.bit ← 0			
		A.bit	2	1	–	A.bit ← 0			
		!addr16.bit	4	2	–	(addr16).bit ← 0			
		PSW.bit	3	4	–	PSW.bit ← 0	×	×	×
		[HL].bit	2	2	–	(HL).bit ← 0			
		ES:!addr16.bit	5	3	–	(ES, addr16).bit ← 0			
		ES:[HL].bit	3	3	–	(ES, HL).bit ← 0			
	SET1	CY	2	1	–	CY ← 1			1
	CLR1	CY	2	1	–	CY ← 0			0
	NOT1	CY	2	1	–	CY ← $\overline{CY}$			×

Notes 1. When the internal RAM area, SFR area, or extended SFR area is accessed, or for an instruction with no data access.

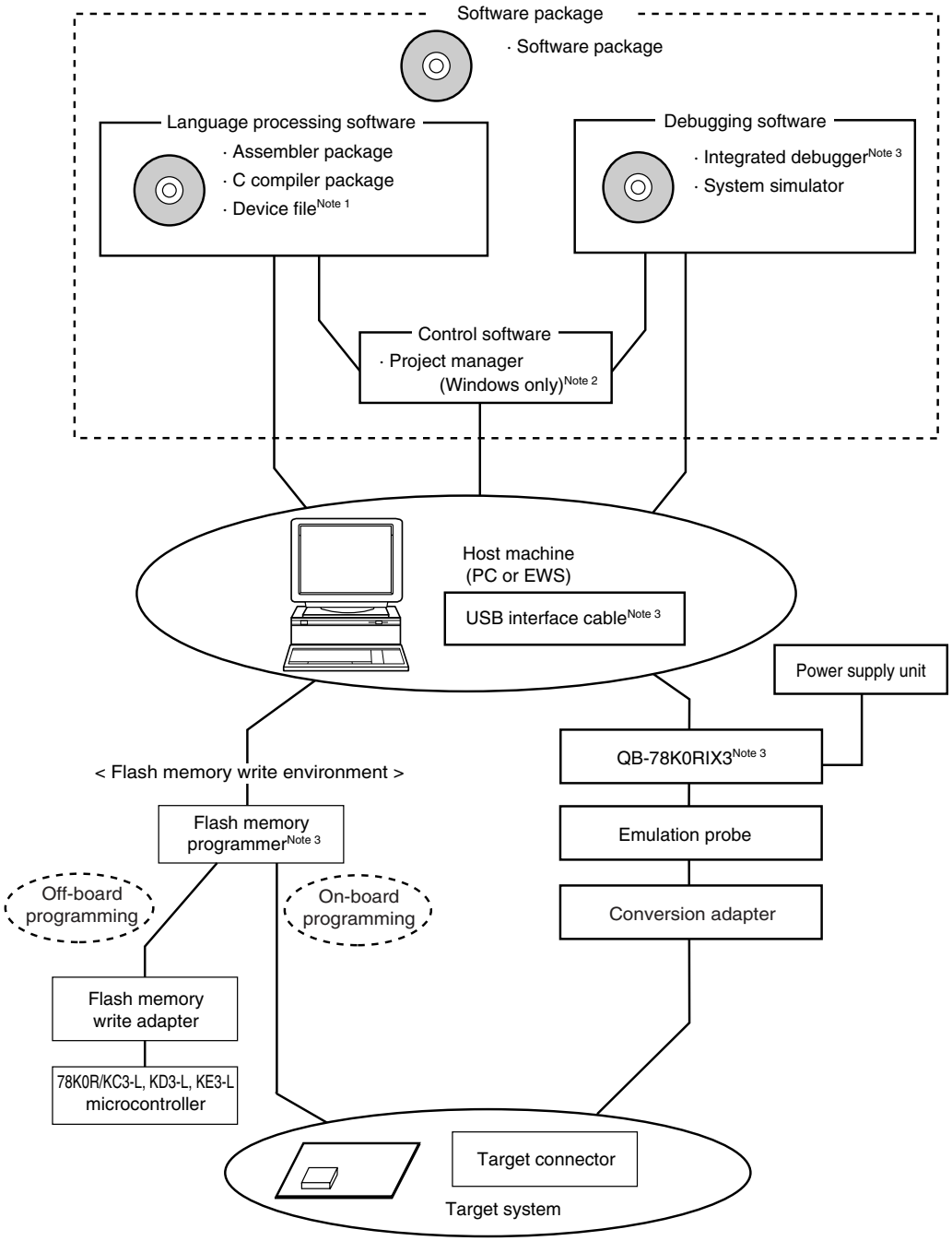
2. When the program memory area is accessed.

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (f_{CPU}) selected by the system clock control register (CKC).

2. This number of clocks is for when the program is in the internal ROM (flash memory) area. When fetching an instruction from the internal RAM area, the number of clocks is twice the number of clocks plus 3, maximum.

Figure A-1. Development Tool Configuration (1/3)

(1) When using the in-circuit emulator QB-78K0RIX3 (compatible with 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L)



Notes 1. Download the device file for the 78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L (DF781014) from the download site for development tools (http://www2.renesas.com/micro/en/ods/).

2. The project manager PM+ is included in the assembler package.
The PM+ is only used for Windows.

3. In-circuit emulator QB-78K0RIX3 is supplied with integrated debugger ID78K0R-QB, on-chip debug emulator with programming function QB-MINI2 and USB interface cable. Any other products are sold separately.