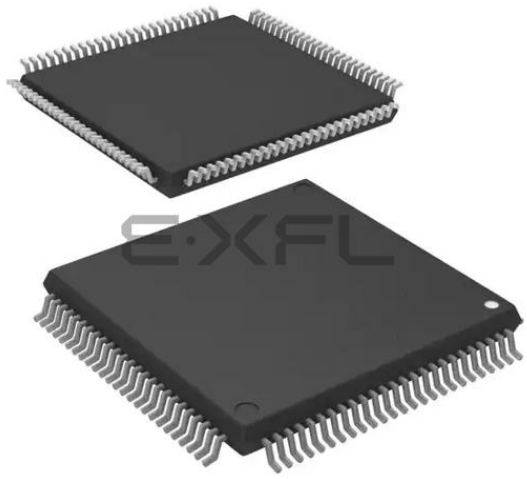
# Renesas Electronics America Inc - UPD78F1014GF-GAS-AX Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 78K/0R |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | 3-Wire SIO, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 84 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 16x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f1014gf-gas-ax |

### 2.1.1 78K0R/KC3-L (40-pin products)

#### (1) Port functions (1/2): 78K0R/KC3-L (40-pin)

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| P10 | I/O | Port 1.<br>4-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | TI02/TO02 |
| P11 | | | | TI03/TO03 |
| P12 | | | | TI04/TO04 |
| P13 | | | | TI05/TO05 |
| P20 to P27 | I/O | Port 2.<br>8-bit I/O port.<br>Input/output can be specified in 1-bit units. | Digital input port | ANI0 to ANI7 |
| P30 | I/O | Port 3.<br>3-bit I/O port.<br>Input of P31 and P32 can be set to TTL buffer.<br>Output of P30 to P32 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | SO10/TxD1 |
| P31 | | | | SI10/RxD1/SDA10/INTP1 |
| P32 | | | | $\overline{\text{SCK10}}$/SCL10/INTP2 |
| P40[Note] | I/O | Port 4.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | TOOL0 |
| P41 | | | | TOOL1 |
| P50 | I/O | Port 5.<br>2-bit I/O port.<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | TI06/TO06 |
| P51 | | | | TI07/TO07 |
| P70 | I/O | Port 7.<br>6-bit I/O port.<br>Input of P71, P72, P74, and P75 can be set to TTL buffer.<br>Output of P70, P72, P73, and P75 can be set to N-ch open-drain output ($V_{DD}$ tolerance).<br>Input/output can be specified in 1-bit units.<br>Use of an on-chip pull-up resistor can be specified by a software setting. | Input port | KR0/SO01/INTP4 |
| P71 | | | | KR1/SI01/INTP5 |
| P72 | | | | KR2/$\overline{\text{SCK01}}$/INTP6 |
| P73 | | | | KR3/SO00/TxD0 |
| P74 | | | | KR4/SI00/RxD0 |
| P75 | | | | KR5/$\overline{\text{SCK00}}$ |

**Note** If on-chip debugging is enabled by using an option byte, be sure to pull up the P40/TOOL0 pin externally.

### (2) Non-port functions (3/3): 78K0R/KE3-L

| Function Name | I/O | Function | After Reset | Alternate Function |
|---|---|---|---|---|
| $V_{DD}$ | – | Positive power supply (P121 to P124 and other than ports (other than $\overline{\text{RESET}}$ pin and FLMD0 pin)) | – | – |
| $EV_{DD}$ | – | Positive power supply for ports (other than P20 to P27, P150 to P153, P80 to P83, and P121 to P124), and $\overline{\text{RESET}}$ and FLMD0 pin | – | – |
| $AV_{REF}$ | – | • A/D converter and comparator reference voltage input<br>• Positive power supply for P20 to P27, P150 to P153, P80 to P83, A/D converter, programmable gain amplifier, and comparator | – | – |
| $V_{SS}$ | – | Ground potential (P121 to P124 and other than ports (other than $\overline{\text{RESET}}$ pin and FLMD0 pin)) | – | – |
| $EV_{SS}$ | – | Ground potential for ports (other than P20 to P27, P150 to P153, and P121 to P124), and $\overline{\text{RESET}}$ and FLMD0 pin | – | – |
| $AV_{SS}$ | – | Ground potential for A/D converter, programmable gain amplifier, comparator, P20 to P27, P150 to P153 and P80 to P83 | – | – |
| FLMD0 | – | Flash memory programming mode setting | – | – |
| TOOL0 | I/O | Data I/O for flash memory programmer/debugger | Input port | P40 |
| TOOL1 | Output | Clock output for debugger | Input port | P41 |

Correspondence between the address values and block numbers in the flash memory are shown below.

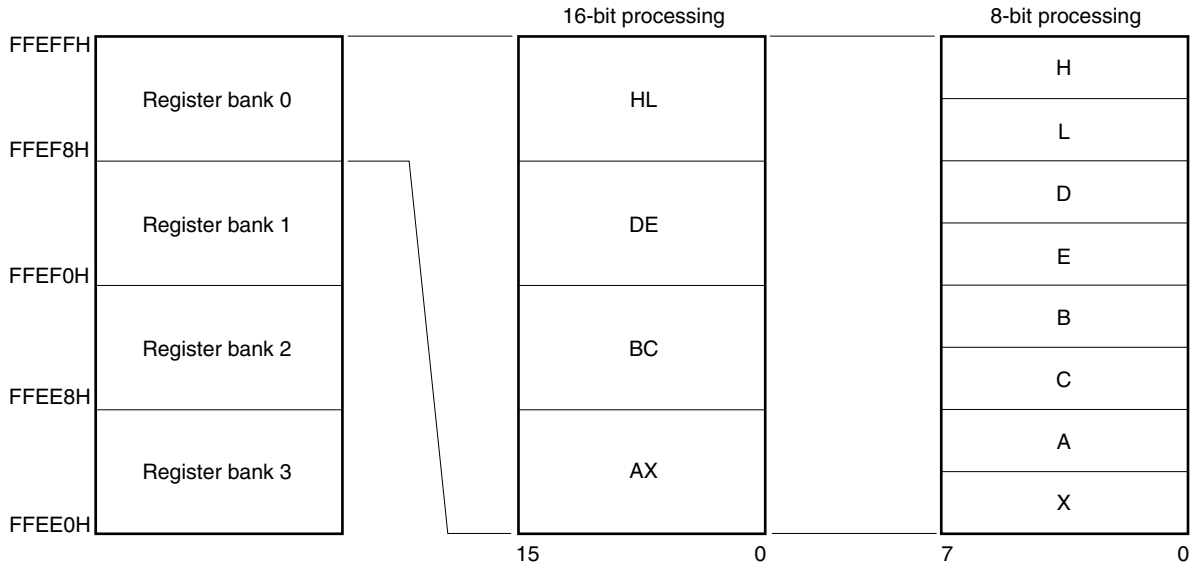
**Table 4-1. Correspondence Between Address Values and Block Numbers in Flash Memory (1/2)**

| Address Value | Block Number | Address Value | Block Number | Address Value | Block Number | Address Value | Block Number |
|---|---|---|---|---|---|---|---|
| 00000H to 003FFH | 00H | 08000H to 083FFH | 20H | 10000H to 103FFH | 40H | 18000H to 183FFH | 60H |
| 00400H to 007FFH | 01H | 08400H to 087FFH | 21H | 10400H to 107FFH | 41H | 18400H to 187FFH | 61H |
| 00800H to 00BFFH | 02H | 08800H to 08BFFH | 22H | 10800H to 10BFFH | 42H | 18800H to 18BFFH | 62H |
| 00C00H to 00FFFH | 03H | 08C00H to 08FFFH | 23H | 10C00H to 10FFFH | 43H | 18C00H to 18FFFH | 63H |
| 01000H to 013FFH | 04H | 09000H to 093FFH | 24H | 11000H to 113FFH | 44H | 19000H to 193FFH | 64H |
| 01400H to 017FFH | 05H | 09400H to 097FFH | 25H | 11400H to 117FFH | 45H | 19400H to 197FFH | 65H |
| 01800H to 01BFFH | 06H | 09800H to 09BFFH | 26H | 11800H to 11BFFH | 46H | 19800H to 19BFFH | 66H |
| 01C00H to 01FFFH | 07H | 09C00H to 09FFFH | 27H | 11C00H to 11FFFH | 47H | 19C00H to 19FFFH | 67H |
| 02000H to 023FFH | 08H | 0A000H to 0A3FFH | 28H | 12000H to 123FFH | 48H | 1A000H to 1A3FFH | 68H |
| 02400H to 027FFH | 09H | 0A400H to 0A7FFH | 29H | 12400H to 127FFH | 49H | 1A400H to 1A7FFH | 69H |
| 02800H to 02BFFH | 0AH | 0A800H to 0ABFFH | 2AH | 12800H to 12BFFH | 4AH | 1A800H to 1ABFFH | 6AH |
| 02C00H to 02FFFH | 0BH | 0AC00H to 0AFFFH | 2BH | 12C00H to 12FFFH | 4BH | 1AC00H to 1AFFFH | 6BH |
| 03000H to 033FFH | 0CH | 0B000H to 0B3FFH | 2CH | 13000H to 133FFH | 4CH | 1B000H to 1B3FFH | 6CH |
| 03400H to 037FFH | 0DH | 0B400H to 0B7FFH | 2DH | 13400H to 137FFH | 4DH | 1B400H to 1B7FFH | 6DH |
| 03800H to 03BFFH | 0EH | 0B800H to 0BBFFH | 2EH | 13800H to 13BFFH | 4EH | 1B800H to 1BBFFH | 6EH |
| 03C00H to 03FFFH | 0FH | 0BC00H to 0BFFFH | 2FH | 13C00H to 13FFFH | 4FH | 1BC00H to 1BFFFH | 6FH |
| 04000H to 043FFH | 10H | 0C000H to 0C3FFH | 30H | 14000H to 143FFH | 50H | 1C000H to 1C3FFH | 70H |
| 04400H to 047FFH | 11H | 0C400H to 0C7FFH | 31H | 14400H to 147FFH | 51H | 1C400H to 1C7FFH | 71H |
| 04800H to 04BFFH | 12H | 0C800H to 0CBFFH | 32H | 14800H to 14BFFH | 52H | 1C800H to 1CBFFH | 72H |
| 04C00H to 04FFFH | 13H | 0CC00H to 0CFFFH | 33H | 14C00H to 14FFFH | 53H | 1CC00H to 1CFFFH | 73H |
| 05000H to 053FFH | 14H | 0D000H to 0D3FFH | 34H | 15000H to 153FFH | 54H | 1D000H to 1D3FFH | 74H |
| 05400H to 057FFH | 15H | 0D400H to 0D7FFH | 35H | 15400H to 157FFH | 55H | 1D400H to 1D7FFH | 75H |
| 05800H to 05BFFH | 16H | 0D800H to 0DBFFH | 36H | 15800H to 15BFFH | 56H | 1D800H to 1DBFFH | 76H |
| 05C00H to 05FFFH | 17H | 0DC00H to 0DFFFH | 37H | 15C00H to 15FFFH | 57H | 1DC00H to 1DFFFH | 77H |
| 06000H to 063FFH | 18H | 0E000H to 0E3FFH | 38H | 16000H to 163FFH | 58H | 1E000H to 1E3FFH | 78H |
| 06400H to 067FFH | 19H | 0E400H to 0E7FFH | 39H | 16400H to 167FFH | 59H | 1E400H to 1E7FFH | 79H |
| 06800H to 06BFFH | 1AH | 0E800H to 0EBFFH | 3AH | 16800H to 16BFFH | 5AH | 1E800H to 1EBFFH | 7AH |
| 06C00H to 06FFFH | 1BH | 0EC00H to 0EFFFH | 3BH | 16C00H to 16FFFH | 5BH | 1EC00H to 1EFFFH | 7BH |
| 07000H to 073FFH | 1CH | 0F000H to 0F3FFH | 3CH | 17000H to 173FFH | 5CH | 1F000H to 1F3FFH | 7CH |
| 07400H to 077FFH | 1DH | 0F400H to 0F7FFH | 3DH | 17400H to 177FFH | 5DH | 1F400H to 1F7FFH | 7DH |
| 07800H to 07BFFH | 1EH | 0F800H to 0FBFFH | 3EH | 17800H to 17BFFH | 5EH | 1F800H to 1FBFFH | 7EH |
| 07C00H to 07FFFH | 1FH | 0FC00H to 0FFFFH | 3FH | 17C00H to 17FFFH | 5FH | 1FC00H to 1FFFFH | 7FH |

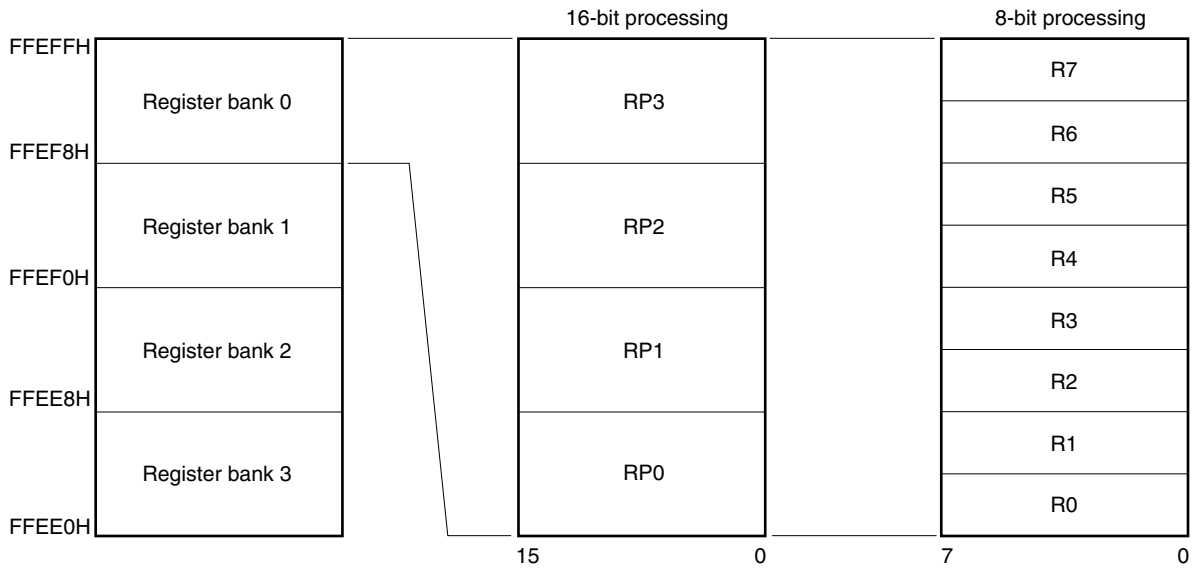
**Remark** μPD78F1000: Block numbers 00H to 0FH
μPD78F1001, 78F1004, 78F1007: Block numbers 00H to 1FH
μPD78F1002, 78F1005, 78F1008: Block numbers 00H to 2FH
μPD78F1003, 78F1006, 78F1009, 78F1010: Block numbers 00H to 3FH
μPD78F1011, 78F1013: Block numbers 00H to 5FH
μPD78F1012, 78F1014: Block numbers 00H to 7FH

**Figure 4-24. Configuration of General-Purpose Registers**

**(a) Function name**




**(b) Absolute name**



### 5.2.4 Port 3

| | 78K0R/KC3-L ($\mu$PD78F100y: y = 0 to 3) | | 78K0R/KC3-L (48-pin) ($\mu$PD78F100y: y = 1 to 3) | 78K0R/KD3-L ($\mu$PD78F100y: y = 4 to 6) | 78K0R/KE3-L ($\mu$PD78F100y: y = 7 to 9) |
|---|---|---|---|---|---|
| | 40-pin | 44-pin | | | |
| P30/SO10/TxD1 | √ | | √ | √ | √ |
| P31/SI10/RxD1/ SDA10/INTP1 | √ | | √ | √ | √ |
| P32/$\overline{\text{SCK10}}$/ SCL10/INTP2 | √ | | √ | √ | √ |
| P33 | – | | – | – | √ |

**Remark** √: Mounted

Port 3 is an I/O port with an output latch. Port 3 can be set to the input mode or output mode in 1-bit units using port mode register 3 (PM3). When the P30 to P33 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 3 (PU3).

Input to the P31 and P32 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units using port input mode register 3 (PIM3).

Output from the P30 to P32 pins can be specified as N-ch open-drain output ($V_{DD}$ tolerance) in 1-bit units using port output mode register 3 (POM3).

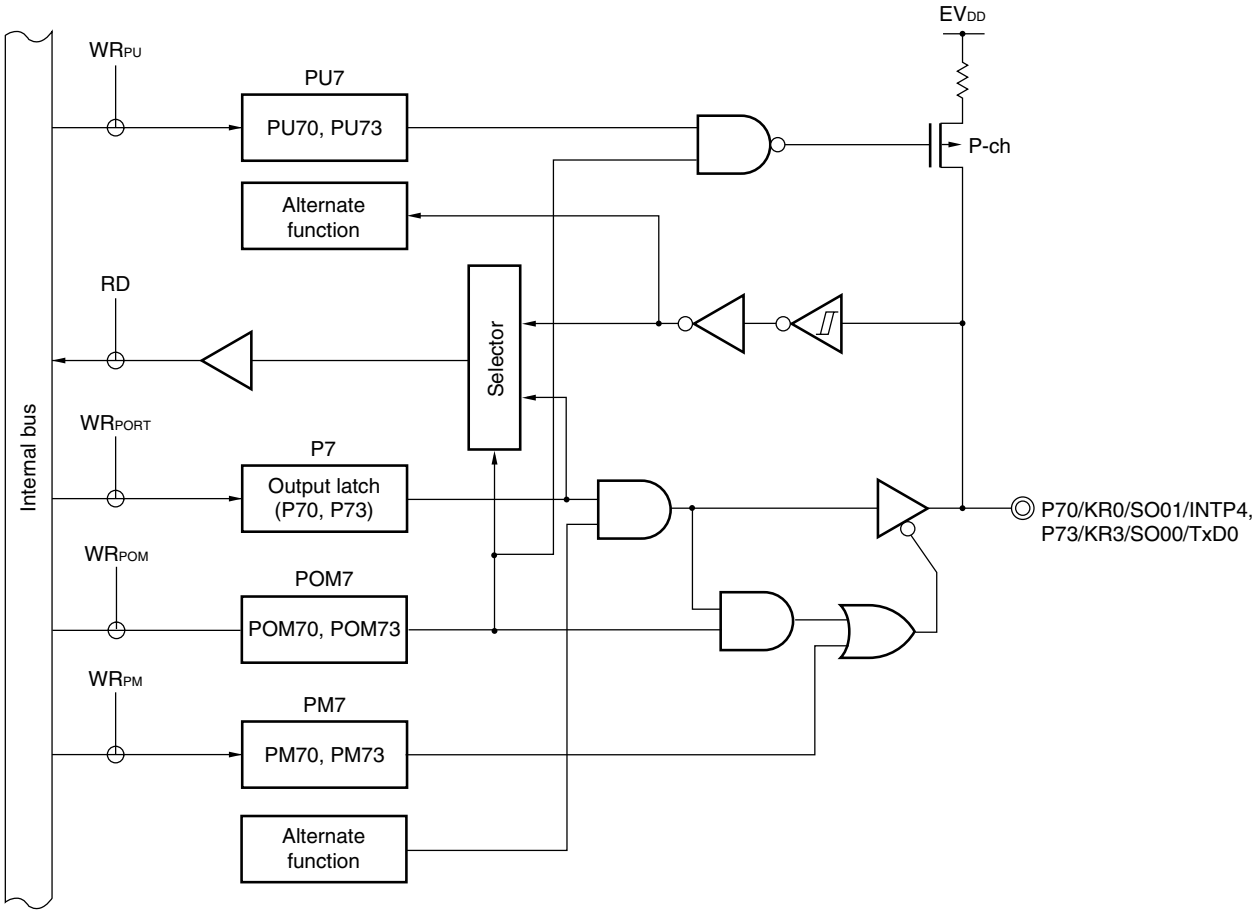
This port can also be used for serial interface data I/O, clock I/O, and external interrupt request input.

Reset signal generation sets port 3 to input mode.

Figures 5-6 to 5-8 show block diagrams of port 3.

**Caution To use P30/SO10/TxD1, P31/SI10/RxD1/SDA10/INTP1, P32/$\overline{\text{SCK10}}$/SCL10/INTP2 as a general-purpose port, note the serial array unit setting. For details, refer to Table 14-7 Relationship Between Register Settings and Pins (Channel 2: CSI10, UART1 Transmission, IIC10) and Table 14-8 Relationship Between Register Settings and Pins (Channel 3: UART1 Reception).**

**Figure 5-15. Block Diagram of P70 and P73**




P7: Port register 7
PU7: Pull-up resistor option register 7
POM7: Port output mode register 7
PM7: Port mode register 7
RD: Read signal
WR××: Write signal

**Remark** With products not provided with an $EV_{DD}$ or $EV_{SS}$ pin, replace $EV_{DD}$ with $V_{DD}$, or replace $EV_{SS}$ with $V_{SS}$.

**Figure 5-30. Format of Port Mode Register (78K0R/KD3-L)**

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Address | After reset | R/W |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PM0 | 1 | 1 | 1 | 1 | 1 | 1 | PM01 | PM00 | FFF20H | FFH | R/W |
| PM1 | 1 | 1 | 1 | 1 | PM13 | PM12 | PM11 | PM10 | FFF21H | FFH | R/W |
| PM2 | PM27 | PM26 | PM25 | PM24 | PM23 | PM22 | PM21 | PM20 | FFF22H | FFH | R/W |
| PM3 | 1 | 1 | 1 | 1 | 1 | PM32 | PM31 | PM30 | FFF23H | FFH | R/W |
| PM4 | 1 | 1 | 1 | 1 | 1 | 1 | PM41 | PM40 | FFF24H | FFH | R/W |
| PM5 | 1 | 1 | 1 | 1 | 1 | PM52 | PM51 | PM50 | FFF25H | FFH | R/W |
| PM6 | 1 | 1 | 1 | 1 | 1 | 1 | PM61 | PM60 | FFF26H | FFH | R/W |
| PM7 | PM77 | PM76 | PM75 | PM74 | PM73 | PM72 | PM71 | PM70 | FFF27H | FFH | R/W |
| PM8 | 1 | 1 | 1 | 1 | PM83 | PM82 | PM81 | PM80 | FFF28H | FFH | R/W |
| PM12 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | PM120 | FFF2CH | FFH | R/W |
| PM15 | 1 | 1 | 1 | 1 | 1 | PM152 | PM151 | PM150 | FFF2FH | FFH | R/W |

| PMmn | Pmn pin I/O mode selection<br>(m = 0 to 8, 12, 15; n = 0 to 7) |
|---|---|
| 0 | Output mode (output buffer on) |
| 1 | Input mode (output buffer off) |

**Caution Be sure to set bits 2 to 7 of the PM0 register, bits 4 to 7 of the PM1 register, bits 3 to 7 of the PM3 register, bits 2 to 7 of the PM4 register, bits 3 to 7 of the PM5 register, bits 2 to 7 of the PM6 register, bits 4 to 7 of the PM8 register, bits 1 to 7 of the PM12 register, and bits 3 to 7 of the PM15 register to 1.**

**(2) Setting procedure when using I/O pins of simplified IIC10 functions**

<1> After reset release, the port mode is the input mode (Hi-Z).

<2> Externally pull up the pin to be used (on-chip pull-up resistor cannot be used).

In case of simplified IIC10: P31, P32

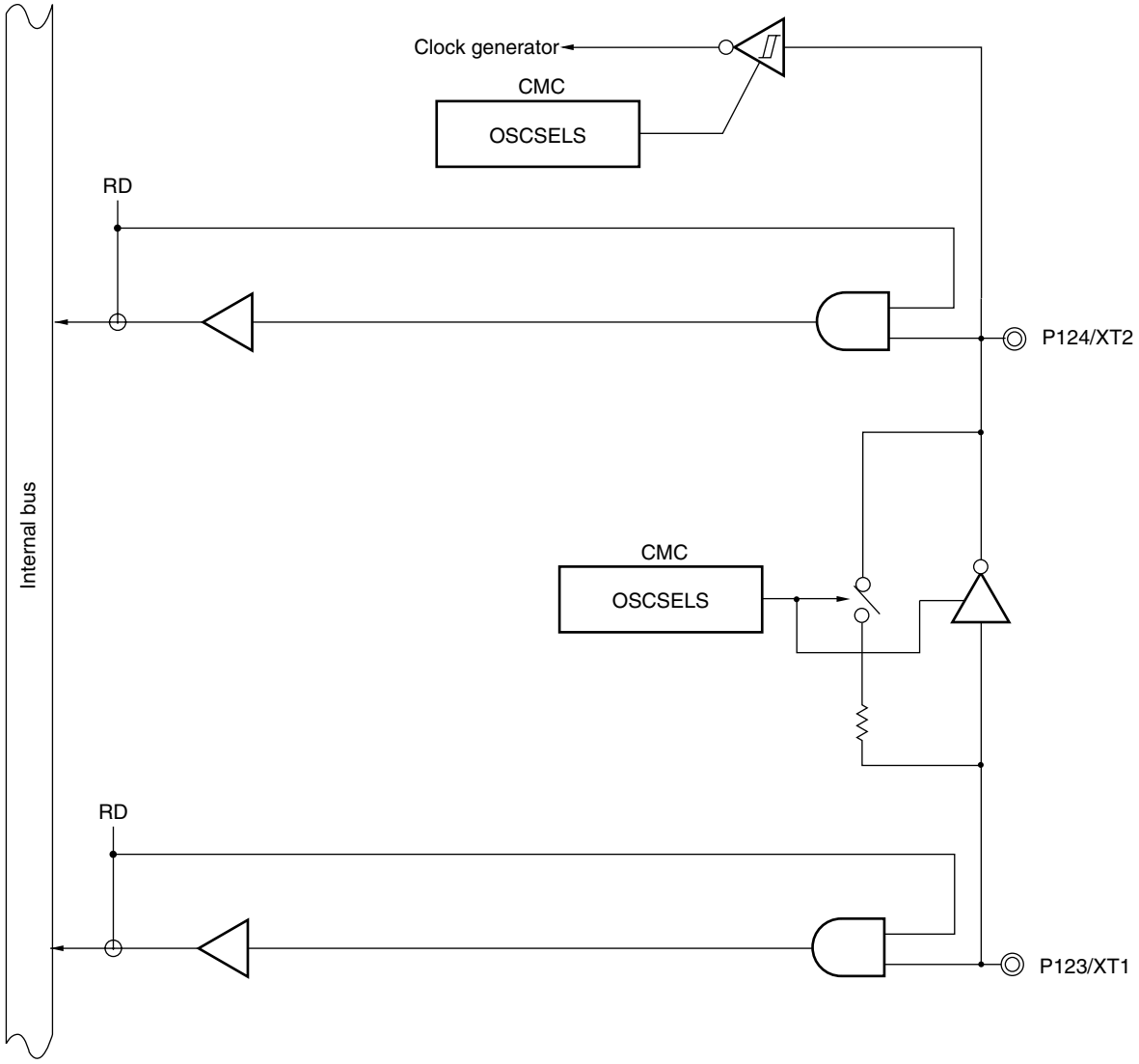
<3> Set the output latch of the corresponding port to 1.

<4> Set the corresponding bit of the POM3 register to 1 to set the N-ch open drain output ($V_{DD}$ withstand voltage) mode.

<5> Set the corresponding bit of the PM3 register to the output mode (data I/O is possible in the output mode). At this time, the output data is high level, so the pin is in the Hi-Z state.

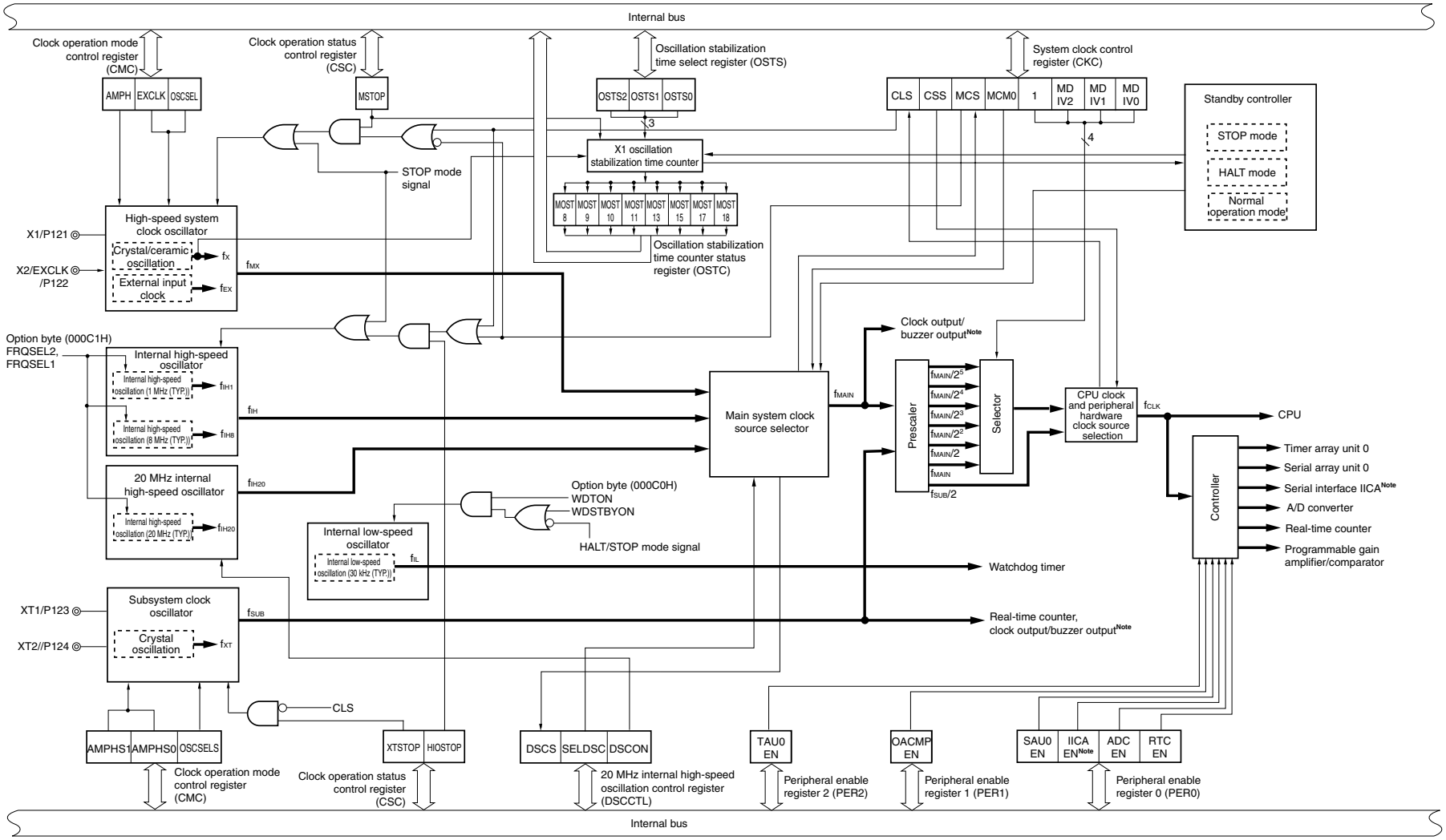
<6> Enable the operation of the serial array unit and set the mode to the simplified $I^2C$ mode.

**Figure 6-44. Block Diagram of P123 and P124**




CMC: Clock operation mode control register
RD: Read signal

**Figure 7-2. Block Diagram of Clock Generator (78K0R/KC3-L (44-pin and 48-pin), 78K0R/KD3-L, 78K0R/KE3-L)**




**Note** This is not mounted onto 44-pin product of the 78K0R/KC3-L.

(**Remark** is listed on the next page after next.)

**(8) Timer input select register m (TISm)**

The TISm register is used to select whether a signal input to the timer input pin (TImn) or the subsystem clock divided by four ($f_{SUB}/4$)[Note] is valid for each channel.

The TISm register can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

**Note** The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

**Figure 8-21. Format of Timer Input Select register m (TISm)**

Address: FFF3EH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TIS0 | TIS07 | TIS06 | TIS05 | TIS04 | TIS03 | TIS02 | TIS01 | TIS00 |

Address: FFF3FH After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| TIS1 | 0 | 0 | 0 | 0 | TIS13 | TIS12 | TIS11 | TIS10 |

| TISmn | Selection of timer input/subsystem clock used with channel n |
|---|---|
| 0 | Input signal of timer input pin (TImn) |
| 1 | Subsystem clock divided by 4 ($f_{SUB}/4$)[Note] |

**Note** The 78K0R/KC3-L (40-pin) doesn't have the subsystem clock.

**Remark** m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)
However, in case of the timer input pin (TImn), mn changes as below.
78K0R/KC3-L (40-pin): mn = 02 to 07
78K0R/KC3-L (44-pin, 48-pin): mn = 00 to 07
78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 07
78K0R/KF3-L, 78K0R/KG3-L: mn = 00 to 07, 10 to 13

Correction example <1>

Example of correcting from 32772.3 Hz to 32768 Hz (32772.3 Hz – 131.2 ppm)

[Measuring the oscillation frequency]

The oscillation frequency[Note] of each product is measured by outputting about 32.768 kHz from the RTCCL pin or outputting about 1 Hz from the RTC1HZ pin when the watch error correction register (SUBCUD) is set to its initial value (00H).

**Note** See **9.4.5 1 Hz output of real-time counter** for the setting procedure of outputting about 1 Hz from the RTC1HZ pin, and **9.4.6 32.768 kHz output of real-time counter** for the setting procedure of outputting about 32 kHz from the RTCCL pin.

[Calculating the correction value]

(When the output frequency from the RTCCL pin is 32772.3 Hz)

If the target frequency is assumed to be 32768 Hz (32772.3 Hz – 131.2 ppm), the correction range for –131.2 ppm is –63.1 ppm or less, so assume DEV to be 0.

The expression for calculating the correction value when DEV is 0 is applied.

Correction value = Number of correction counts in 1 minute ÷ 3
= (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60 ÷ 3
= (32772.3 ÷ 32768 – 1) × 32768 × 60 ÷ 3
= 86

[Calculating the values to be set to (F6 to F0)]

(When the correction value is 86)

If the correction value is 0 or more (when delaying), assume F6 to be 0.

Calculate (F5, F4, F3, F2, F1, F0) from the correction value.

{ (F5, F4, F3, F2, F1, F0) – 1} × 2 = 86
(F5, F4, F3, F2, F1, F0) = 44
(F5, F4, F3, F2, F1, F0) = (1, 0, 1, 1, 0, 0)

Consequently, when correcting from 32772.3 Hz to 32768 Hz (32772.3 Hz – 131.2 ppm), setting the correction register such that DEV is 0 and the correction value is 86 (bits 6 to 0 of SUBCUD register: 0101100) results in 32768 Hz (0 ppm).

Figure 9-26 shows the operation when (DEV, F6, F5, F4, F3, F2, F1, F0) is (0, 0, 1, 0, 1, 1, 0, 0).

## 13.2 Configuration of A/D Converter

The A/D converter includes the following hardware.

**(1) ANI0 to ANI15 pins**

These are the analog input pins of the sixteen channels of the A/D converter. They input analog signals to be converted into digital signals. Pins other than the one selected as the analog input pin can be used as I/O port pins.

**Remark** ANI0 to ANI9: 78K0R/KC3-L (40-pin, 44-pin)
ANI0 to ANI10: 78K0R/KC3-L (48-pin) and 78K0R/KD3-L
ANI0 to ANI11: 78K0R/KE3-L, 78K0R/KF3-L
ANI0 to ANI15: 78K0R/KG3-L

**(2) PGAO (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L only)**

This is the programmable gain amplifier output signal from the PGAI pin. The A/D converter can perform A/D conversion by selecting the output signal of the programmable gain amplifier as the analog input.

**(3) Sample & hold circuit**

The sample & hold circuit samples each of the analog input voltages sequentially sent from the input circuit, and sends them to the A/D voltage comparator. This circuit also holds the sampled analog input voltage during A/D conversion.

**(4) A/D voltage comparator**

This A/D voltage comparator compares the voltage generated from the voltage tap of the array with the analog input voltage. If the analog input voltage is found to be greater than the reference voltage (1/2 $AV_{REF}$) as a result of the comparison, the most significant bit (MSB) of the successive approximation register (SAR) is set. If the analog input voltage is less than the reference voltage (1/2 $AV_{REF}$), the MSB bit of the SAR is reset.
After that, bit 10 of the SAR register is automatically set, and the next comparison is made. The voltage tap of the array is selected by the value of bit 11, to which the result has been already set.

Bit 11 = 0: (1/4 $AV_{REF}$)
Bit 11 = 1: (3/4 $AV_{REF}$)

The voltage tap of the array and the analog input voltage are compared and bit 10 of the SAR register is manipulated according to the result of the comparison.

Analog input voltage ≥ Voltage tap of array: Bit 10 = 1
Analog input voltage ≤ Voltage tap of array: Bit 10 = 0

Comparison is continued like this to bit 0 of the SAR register.

**(5) Array**

The array generates the comparison voltage input from an analog input pin.

## 14.5 Operation of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) Communication

This is a clocked communication function that uses three lines: serial clock ($\overline{SCK}$) and serial data (SI and SO) lines.

[Data transmission/reception]

- Data length of 7 or 8 bits
- Phase control of transmit/receive data
- MSB/LSB first selectable
- Level setting of transmit/receive data

[Clock control]

- Master/slave selection
- Phase control of I/O clock
- Setting of transfer period by prescaler and internal counter of each channel
- Maximum transfer rate

  During master communication: Max. $f_{CLK}/4$, during slave communication: Max. $f_{MCK}/6$ Note

[Interrupt function]

- Transfer end interrupt/buffer empty interrupt

[Error detection flag]

- Overrun error

**Note** Use the clocks within a range satisfying the $\overline{SCK}$ cycle time ($t_{KCY}$) characteristics (see **CHAPTER 30 ELECTRICAL SPECIFICATIONS (78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L), CHAPTER 31 ELECTRICAL SPECIFICATIONS (78K0R/KF3-L, 78K0R/KG3-L)**).

**Figure 14-66. Example of Contents of Registers for Slave Transmission/Reception of 3-Wire Serial I/O (CSI00, CSI01, CSI10, CSI20, CSI40, CSI41) (2/2)**

**(e) Serial output enable register m (SOEm) … Sets only the bits of the target channel to 1.**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOEm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SOEm2<br>0/1<br>Note 2 | SOEm1<br>0/1<br>Note 1 | SOEm0<br>0/1 |

**(f) Serial channel start register m (SSm) … Sets only the bits of the target channel to 1.**

<R>

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SSm | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SSm3<br>× | SSm2<br>0/1<br>Note 2 | SSm1<br>0/1 | SSm0<br>0/1 |

**Notes 1.** Those bits are invalid while operating serial allay unit 1.

**2.** Those bits are invalid while operating serial allay unit 2.

**Remarks 1.** m: Unit number (m = 0 to 2), n: Channel number (n = 0 to 2), p: CSI number (p = 00, 01, 10, 20, 40, 41)

78K0R/KC3-L, 78K0R/KD3-L, 78K0R/KE3-L: mn = 00 to 02, p = 00, 01, 10

78K0R/KF3-L (μ PD78F1010, 78F1011, 78F1012): mn = 00 to 02, 10, p = 00, 01, 10, 20

78K0R/KF3-L (μ PD78F1027, 78F1028): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

78K0R/KG3-L (μ PD78F1013, 78F1014): mn = 00 to 02, 10, p = 00, 01, 10, 20

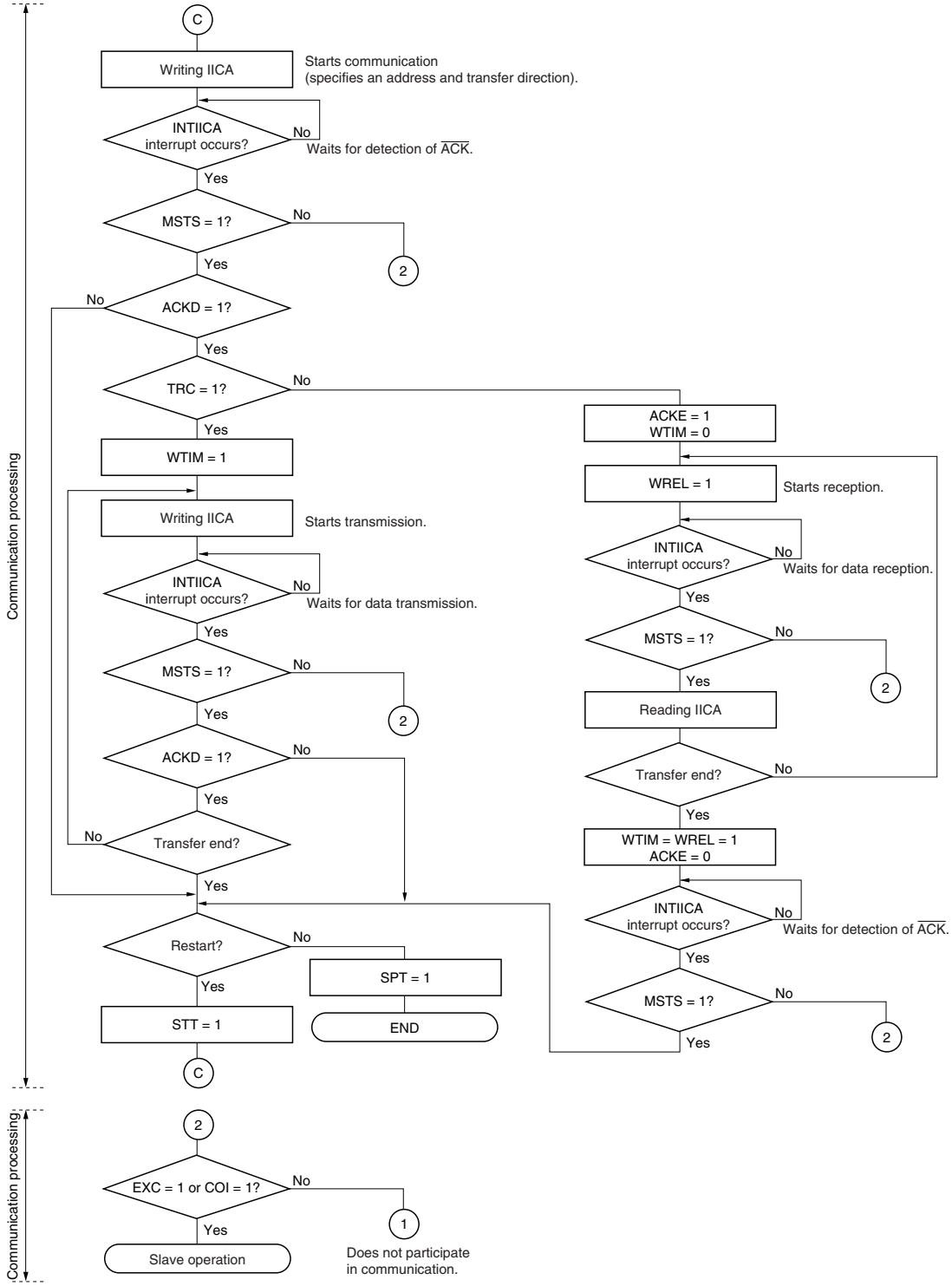
78K0R/KG3-L (μ PD78F1029, 78F1030): mn = 00 to 02, 10, 20, 21, p = 00, 01, 10, 20, 40, 41

**2.** □ : Setting is fixed in the CSI master transmission mode, ■ : Setting disabled (set to the initial value)

×: Bit that cannot be used in this mode (set to the initial value when not used in any mode)

0/1: Set to 0 or 1 depending on the usage of the user

**Figure 15-29. Master Operation in Multi-Master System (3/3)**



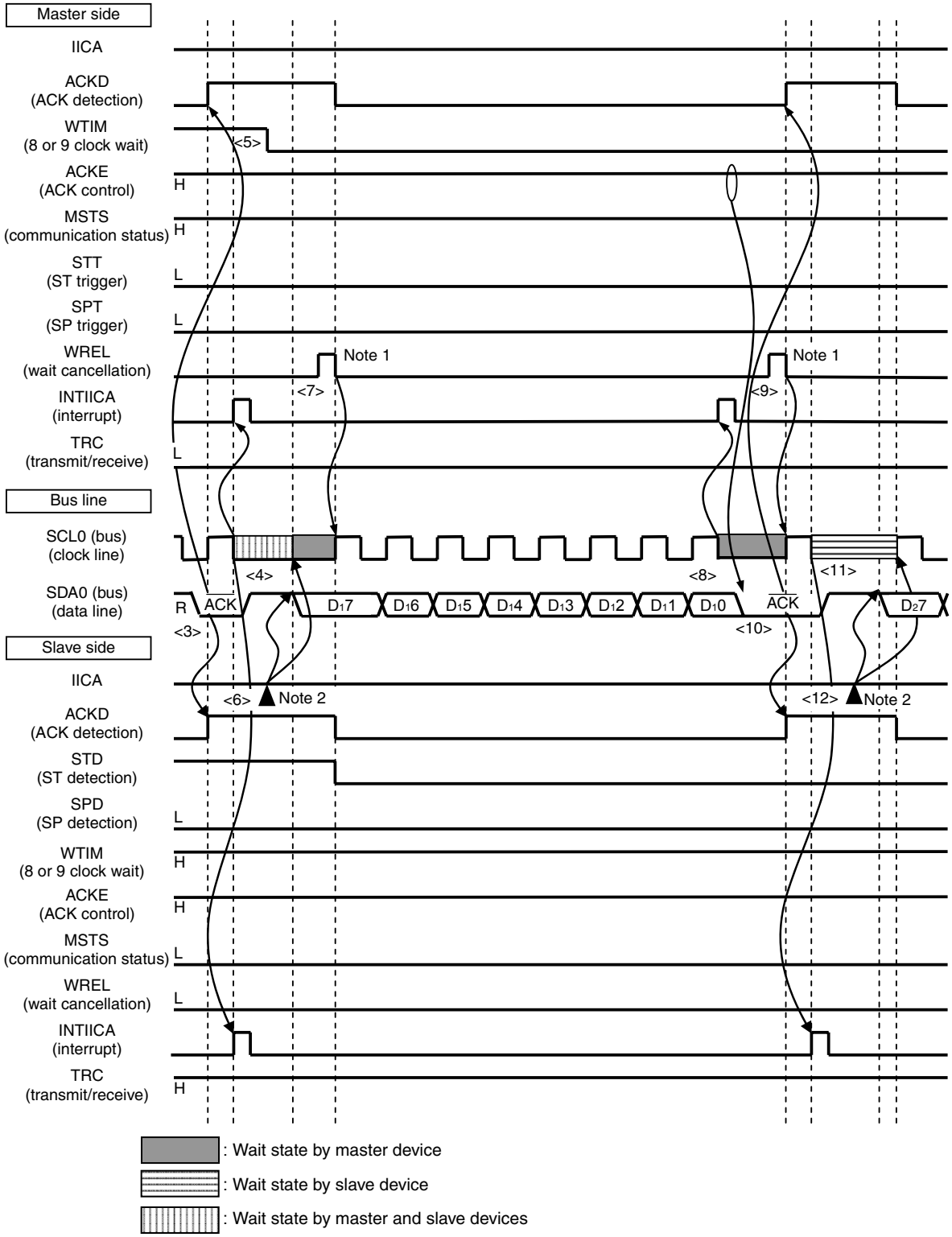

**Remarks 1.** Conform to the specifications of the product that is communicating, with respect to the transmission and reception formats.

**2.** To use the device as a master in a multi-master system, read the MSTS bit each time interrupt INTIICA has occurred to check the arbitration result.

**3.** To use the device as a slave in a multi-master system, check the status by using the IICA status register (IICS) and IICA flag register (IICF) each time interrupt INTIICA has occurred, and determine the processing to be performed next.

**Figure 15-33. Example of Slave to Master Communication (8-Clock Wait Is Selected for Master, 9-Clock Wait Is Selected for Slave) (2/3)**

**(2) Address ~ data ~ data**




<R> **Notes 1.** For releasing wait state during reception of a master device, write “FFH” to IICA or set the WREL bit.

<R> **2.** Write data to IICA, not setting the WREL bit, in order to cancel a wait state during transmission by a slave device.

**(4) External interrupt rising edge enable register 0 (EGP0), external interrupt falling edge enable register 0 (EGN0)**

These registers specify the valid edge for INTP0 to INTP7[Note].

The EGP0 and EGN0 registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

**Figure 18-5. Format of External Interrupt Rising Edge Enable Register 0 (EGP0) and External Interrupt Falling Edge Enable Register 0 (EGN0)**

Address: FFF38H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| EGP0 | EGP7[Note] | EGP6 | EGP5 | EGP4 | EGP3 | EGP2 | EGP1 | EGP0 |

Address: FFF39H After reset: 00H R/W

| Symbol | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| EGN0 | EGN7[Note] | EGN6 | EGN5 | EGN4 | EGN3 | EGN2 | EGN1 | EGN0 |

| EGPn | EGNn | INTPn pin valid edge selection (n = 0 to 7[Note]) |
|---|---|---|
| 0 | 0 | Edge detection disabled |
| 0 | 1 | Falling edge |
| 1 | 0 | Rising edge |
| 1 | 1 | Both rising and falling edges |

Table 18-3 shows the ports corresponding to the EGPn and EGNn bits.

**Table 18-3. Ports Corresponding to EGPn and EGNn Bits**

| Detection Enable Bit | | Edge Detection Port | Interrupt Request Signal |
|---|---|---|---|
| EGP0 | EGN0 | P120 | INTP0 |
| EGP1 | EGN1 | P31 | INTP1 |
| EGP2 | EGN2 | P32 | INTP2 |
| EGP3 | EGN3 | P80 | INTP3 |
| EGP4 | EGN4 | P70 | INTP4 |
| EGP5 | EGN5 | P71 | INTP5 |
| EGP6 | EGN6 | P72 | INTP6 |
| EGP7[Note] | EGN7[Note] | P82[Note] | INTP7[Note] |

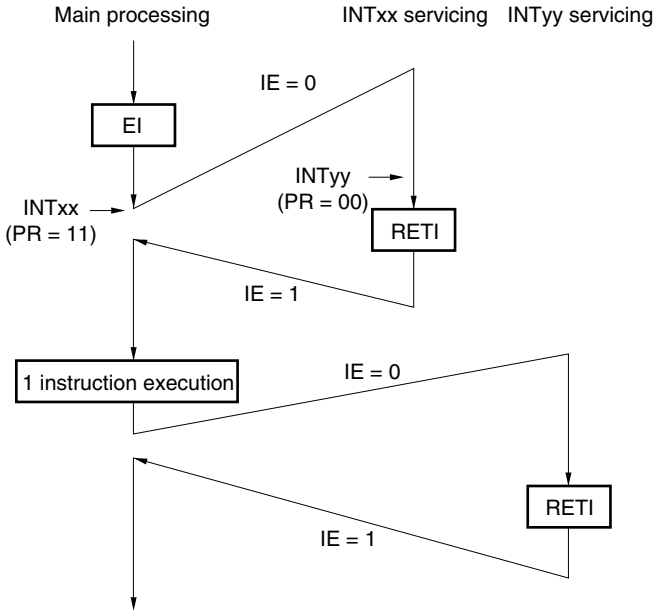
**Note** Those are not provided in the 40-pin product of the 78K0R/KC3-L.

**Caution Select the port mode by clearing the EGPn and EGNn bits to 0 because an edge may be detected when the external interrupt function is switched to the port function.**

**Remark** 78K0R/KC3-L (40-pin): n = 0 to 6
78K0R/KC3-L (44-pin, 48-pin), 78K0R/KD3-L, 78K0R/KE3-L: n = 0 to 7
78K0R/KF3-L, 78K0R/KG3-L: n = 0 to 7

**Figure 18-15. Examples of Multiple Interrupt Servicing (2/2)**

**Example 3. Multiple interrupt servicing does not occur because interrupts are not enabled**




Interrupts are not enabled during servicing of interrupt INTxx (EI instruction is not issued), therefore, interrupt request INTyy is not acknowledged and multiple interrupt servicing does not take place. The INTyy interrupt request is held pending, and is acknowledged following execution of one main processing instruction.

PR = 00: Specify level 0 with ××PR1× = 0, ××PR0× = 0 (higher priority level)
PR = 01: Specify level 1 with ××PR1× = 0, ××PR0× = 1
PR = 10: Specify level 2 with ××PR1× = 1, ××PR0× = 0
PR = 11: Specify level 3 with ××PR1× = 1, ××PR0× = 1 (lower priority level)
IE = 0: Interrupt request acknowledgment is disabled
IE = 1: Interrupt request acknowledgment is enabled.

**Caution The pins mounted depend on the product. Refer to Caution 2 at the beginning of this chapter.**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $V_{DD}$ = $EV_{DD0}$ = $EV_{DD1}$ ≤ 5.5 V, 1.8 V ≤ $AV_{REF}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = $AV_{SS}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P131, P140 to P145, FLMD0, $\overline{\text{RESET}}$ | $V_I = V_{DD}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P150 to P157 | $V_I = AV_{REF}$<br>$AV_{REF} = V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2) | $V_I = V_{DD}$ | In input port | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90, P91, P110, P111, P120, P131, P140 to P145, FLMD0, $\overline{\text{RESET}}$ | $V_I = V_{SS}$ | | | | –1 | μA |
| | $I_{LIL2}$ | P20 to P27, P150 to P157 | $V_I = V_{SS}$<br>$AV_{REF} = V_{DD}$ | | | | –1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2) | $V_I = V_{SS}$ | In input port | | | –1 | μA |
| | | | | In resonator connection | | | –10 | μA |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.