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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410c8u6tr

3.15 Power supply supervisor

3.15.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

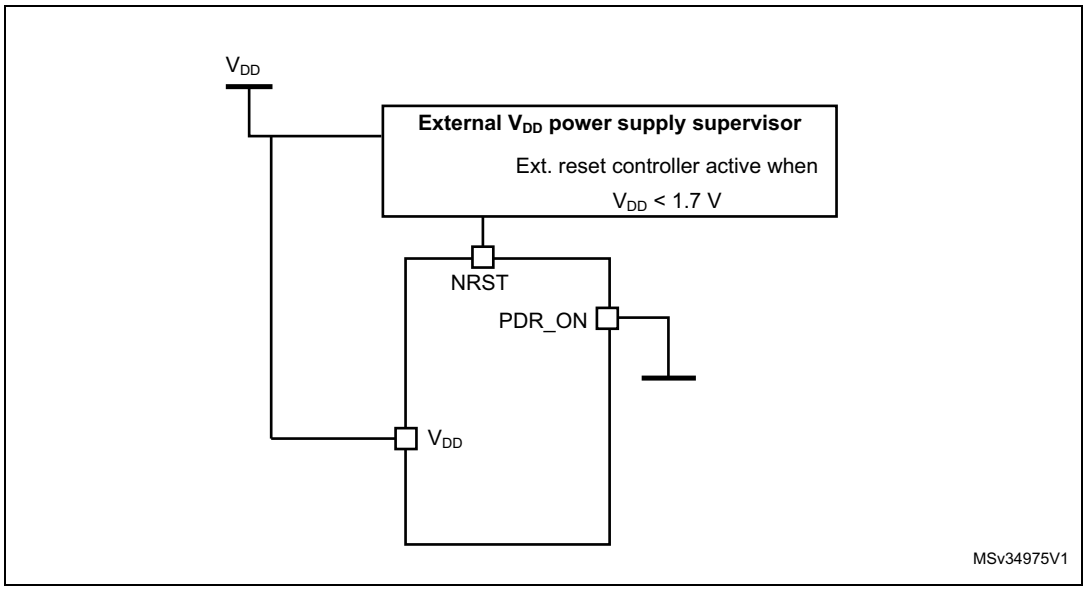
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available on WLCSP36 package only. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 4: Power supply supervisor interconnection with internal reset OFF*.

Figure 4. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available on WLCSP36 package only.

Table 11. STM32F410x8/B register boundary addresses(1)

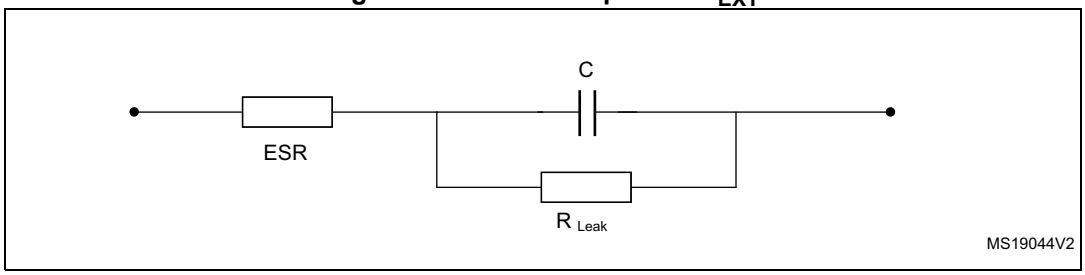
Bus	Boundary address	Peripheral
-	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex®-M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
-	0x5000 0000 - 0xDFFF FFFF	Reserved
AHB1	0x4008 0400 - 0x4FFF FFFF	Reserved
	0x4008 0000 - 0x4008 03FF	RNG
	0x4002 6800 - 0x4007 FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 4FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2800 - 0x4002 2FFF	Reserved
	0x4002 2400 - 0x4002 27FF	LPTIM1
	0x4002 2000 - 0x4002 23FF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 0C00 - 0x4002 1BFF	Reserved
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

6.3.2 VCAP_1 external capacitor

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 pin.

C_{EXT} is specified in *Table 17*.

Figure 15. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 17. VCAP_1 operating conditions

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	4.7 µF
ESR	ESR of external capacitor	< 1 Ω

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 19. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} rise time rate	Power-up	20	∞	
	V_{CAP_1} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(3)(4), External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	8.0	8.2(5)	9.0	9.4(6)	10.2(5)	mA
			84	S2	168	6.5	6.7	7.4	7.7	8.5	
			64	S3	128	4.6	4.7	5.2	5.5	6.3	
			50	S3	100	3.7	3.9	4.3	4.6	5.4	
			25	S3	100	2.2	2.3	2.6	2.9	3.8	
			20	S3	160	2.1	2.2	2.5	2.8	3.6	
		All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	1.1	1.2	1.5	1.9	2.7	
			1	S3	off	0.3	0.4	0.7	1.1	1.9	
		All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON	100	S1	200	8.4	8.7	9.5	9.9	10.7	
			84	S2	168	6.9	7.1	7.7	8.1	8.9	
			64	S3	128	4.9	5.1	5.5	5.9	6.7	
			50	S3	100	4.0	4.2	4.6	4.9	5.7	
			25	S3	100	2.5	2.6	2.9	3.2	4.0	
			20	S3	160	2.4	2.5	2.7	3.1	3.9	
		All peripherals enabled(3), HSI, PLL OFF, Flash memory ON	16	S3	off	1.4	1.4	1.8	2.2	3.0	
			1	S3	off	0.6	0.6	1.0	1.3	2.0	

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD} (continued)	Supply current in **Sleep mode** (continued)	All peripherals disabled, External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	2.2	2.3(5)	2.6	3.0(6)	3.8(5)	mA
			84	S2	168	1.8	1.9	2.2	2.6	3.4	
			64	S3	128	1.4	1.5	1.8	2.1	2.9	
			50	S3	100	1.2	1.3	1.6	1.9	2.7	
			25	S3	100	0.9	1.0	1.3	1.7	2.5	
			20	S3	160	1.0	1.2	1.4	1.7	2.5	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.3	0.4	0.7	1.1	1.9	
			1	S3	off	0.3	0.3	0.7	1.0	1.8	
		All peripherals disabled, External clock, PLL ON, Flash memory ON	100	S1	200	2.6	2.7	3.0	3.4	4.2	
			84	S2	168	2.2	2.3	2.6	3.0	3.8	
			64	S3	128	1.8	1.9	2.1	2.5	3.3	
			50	S3	100	1.5	1.6	1.9	2.2	3.1	
			25	S3	100	1.2	1.4	1.6	2.0	2.8	
			20	S3	160	1.3	1.4	1.7	2.0	2.8	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.6	0.6	1.0	1.3	2.0	
			1	S3	off	0.5	0.6	0.9	1.3	2.0	

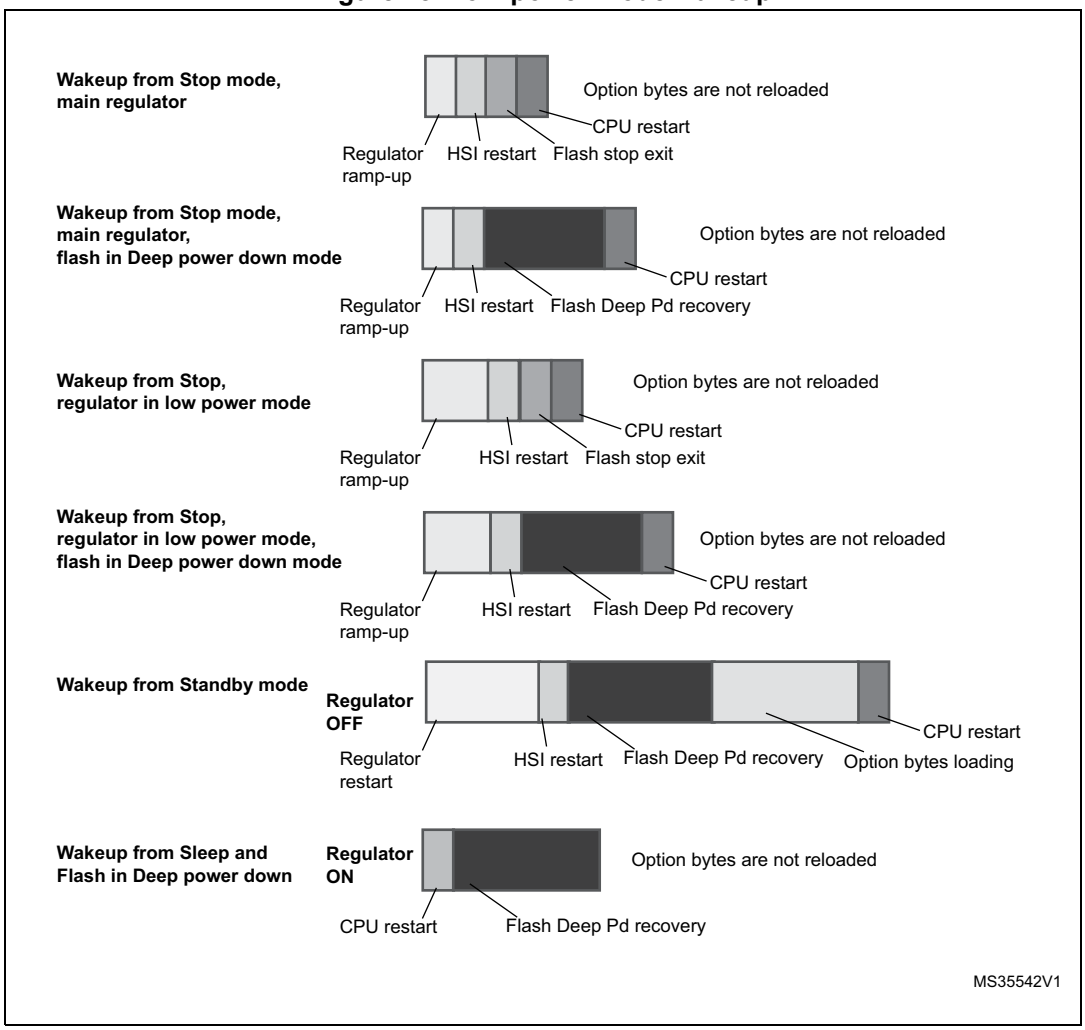
1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production on temperature range 7 salestypes only.

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

Figure 18. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

6.3.9 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

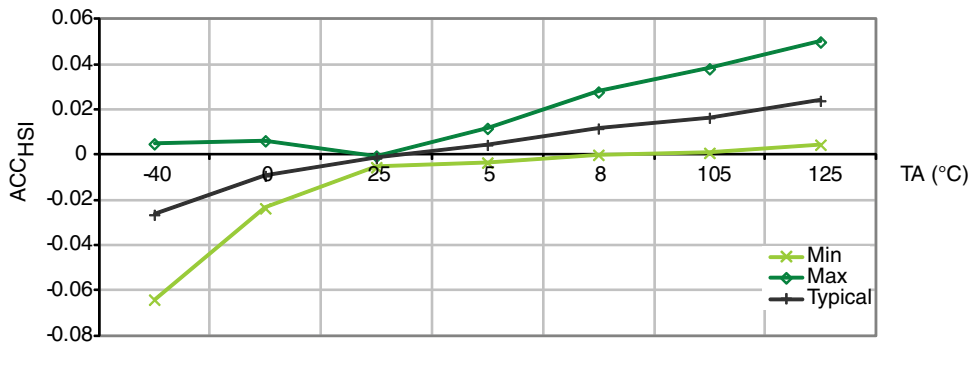
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	16	-	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1	%
		Factory-calibrated	T_A = –40 to 125 °C(3)	–8	-	5.5	%
			T_A = –10 to 85 °C(3)	–4	-	4	%
			T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-		-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-		-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. Factory calibrated non-soldered parts.

Figure 23. ACC_{HSI} versus temperature



1. Guaranteed by characterization.

Figure 25 and *Figure 26* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 25. PLL output clock waveforms in center spread mode

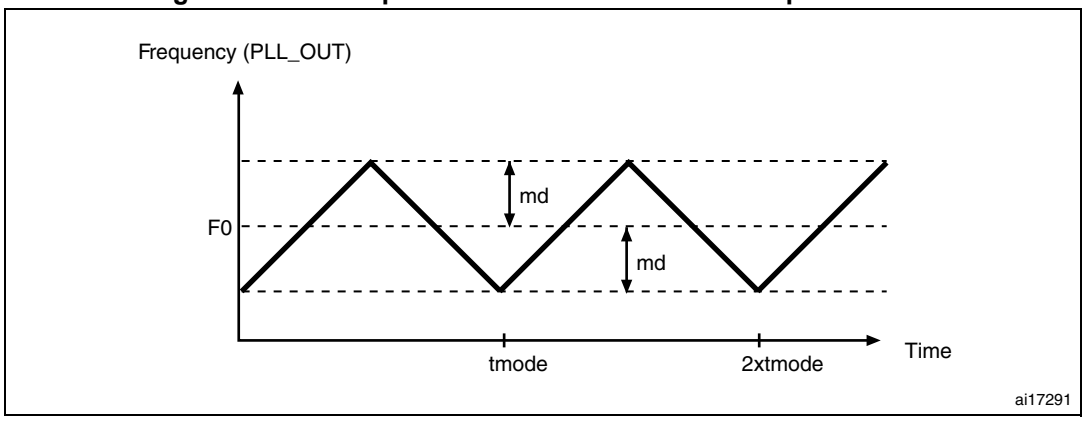
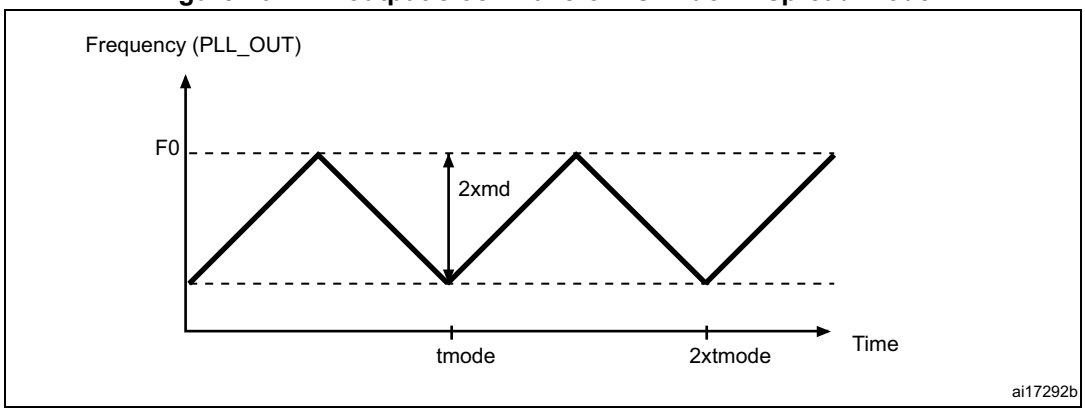


Figure 26. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

In noisy environments, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are PA14 and PA15.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

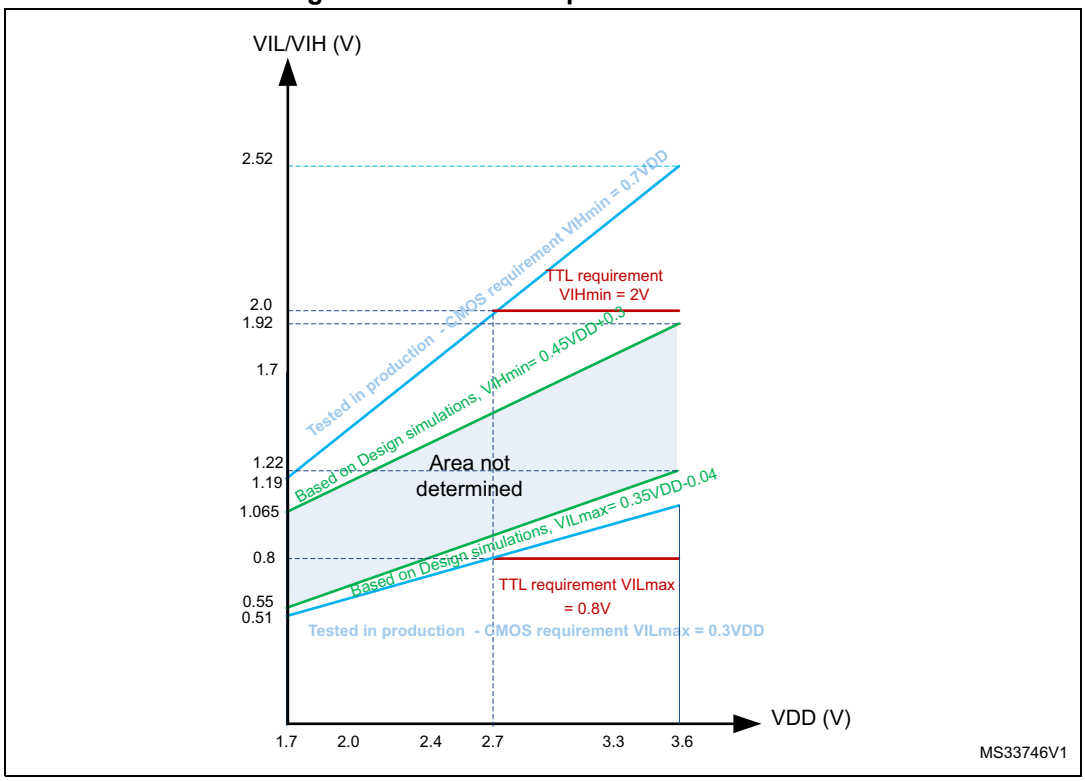
Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 51. EMI characteristics for LQFP64

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				8/100 MHz	
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, conforming to IEC61967-2	0.1 to 30 MHz	10	dBµV
			30 to 130 MHz	11	
			130 MHz to 1 GHz	5	
			SAE EMI Level	2.5	-

Figure 27. FT/TC I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating ΣI_{VDD} (see *Table 13*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see *Table 13*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*. All I/Os are CMOS and TTL compliant.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 60*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.

Table 60. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450(3)	0	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	0	50(5)	0	50(5)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Table 62. SCL frequency (f_{PCLK1}= 42 MHz.,V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 31. FMPI^{2}C timing diagram and measurement circuit

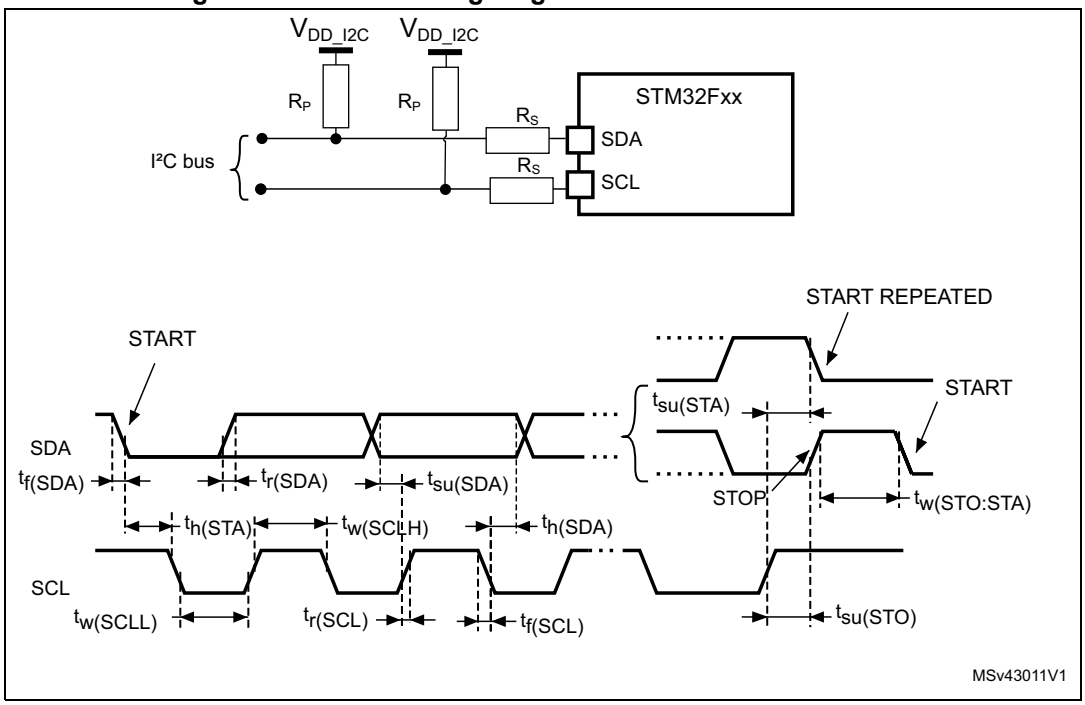
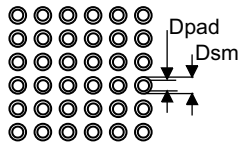


Table 79. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.518	2.553	2.588	0.1012	0.1026	0.1039
E	2.544	2.579	2.614	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-
F	-	0.2765	-	-	0.0119	-
G	-	0.2895	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 42. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



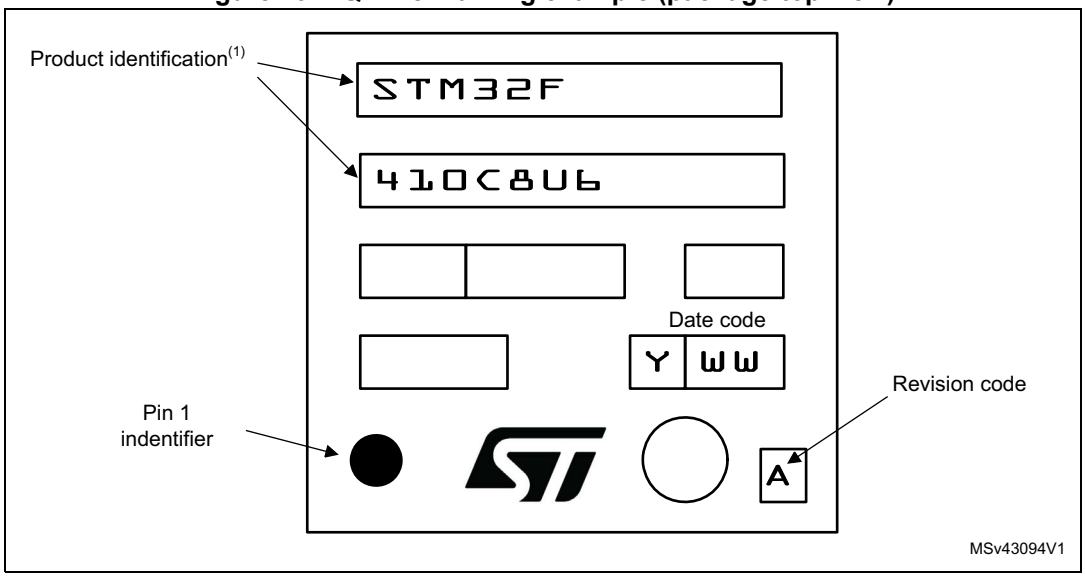
A05F_FP_V1

LQFP48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 49. LQFP48 marking example (package top view)



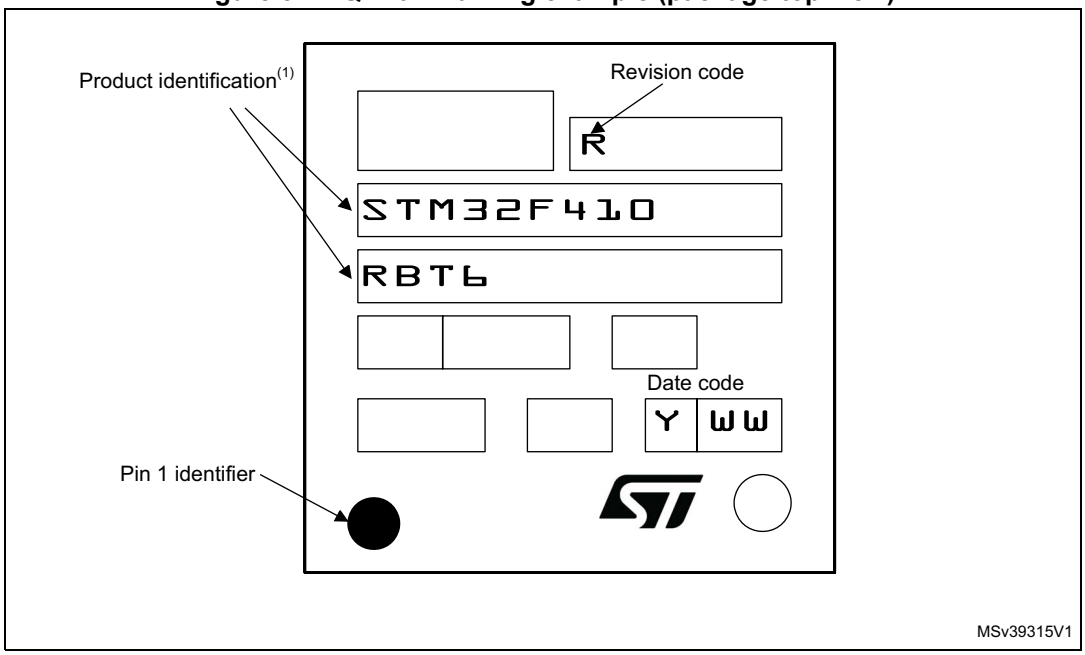
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

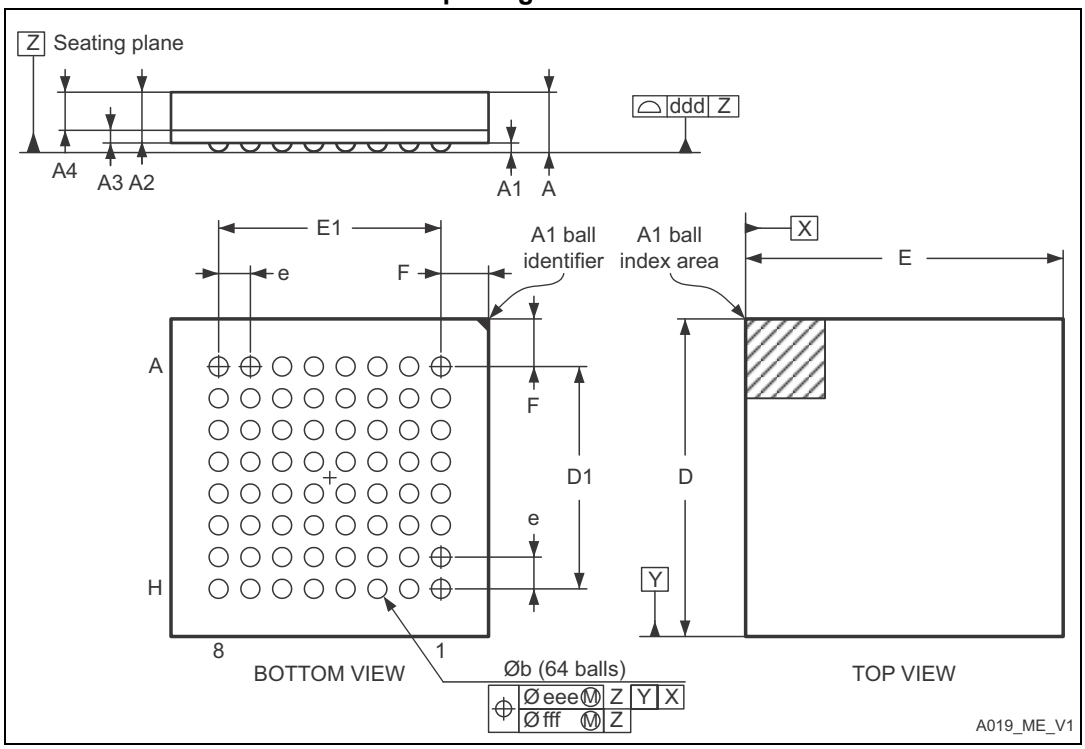
Figure 52. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 UFBGA64 package information

Figure 53. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 84. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

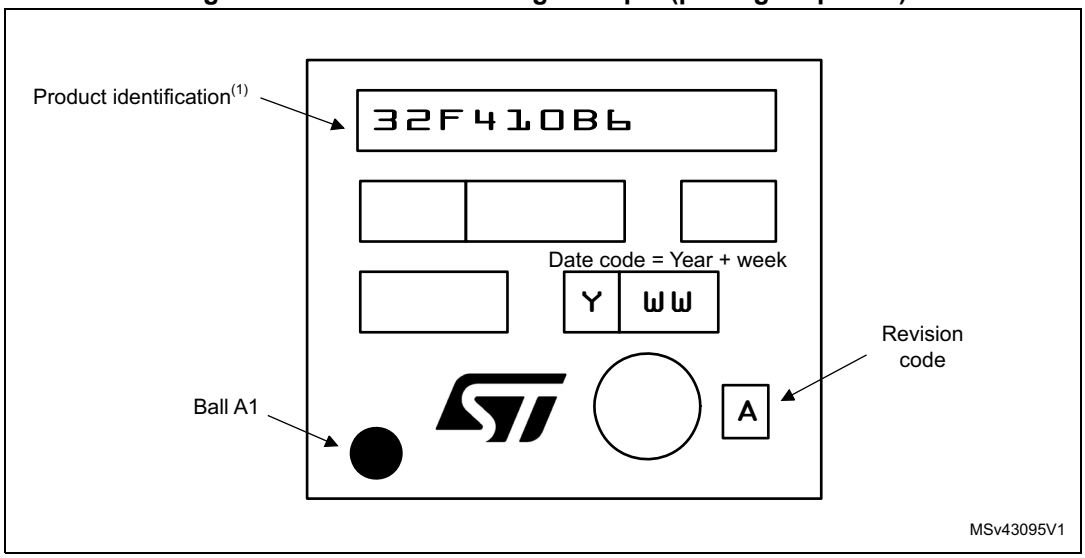
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-

UFBGA64 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 55. UFBGA64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.