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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

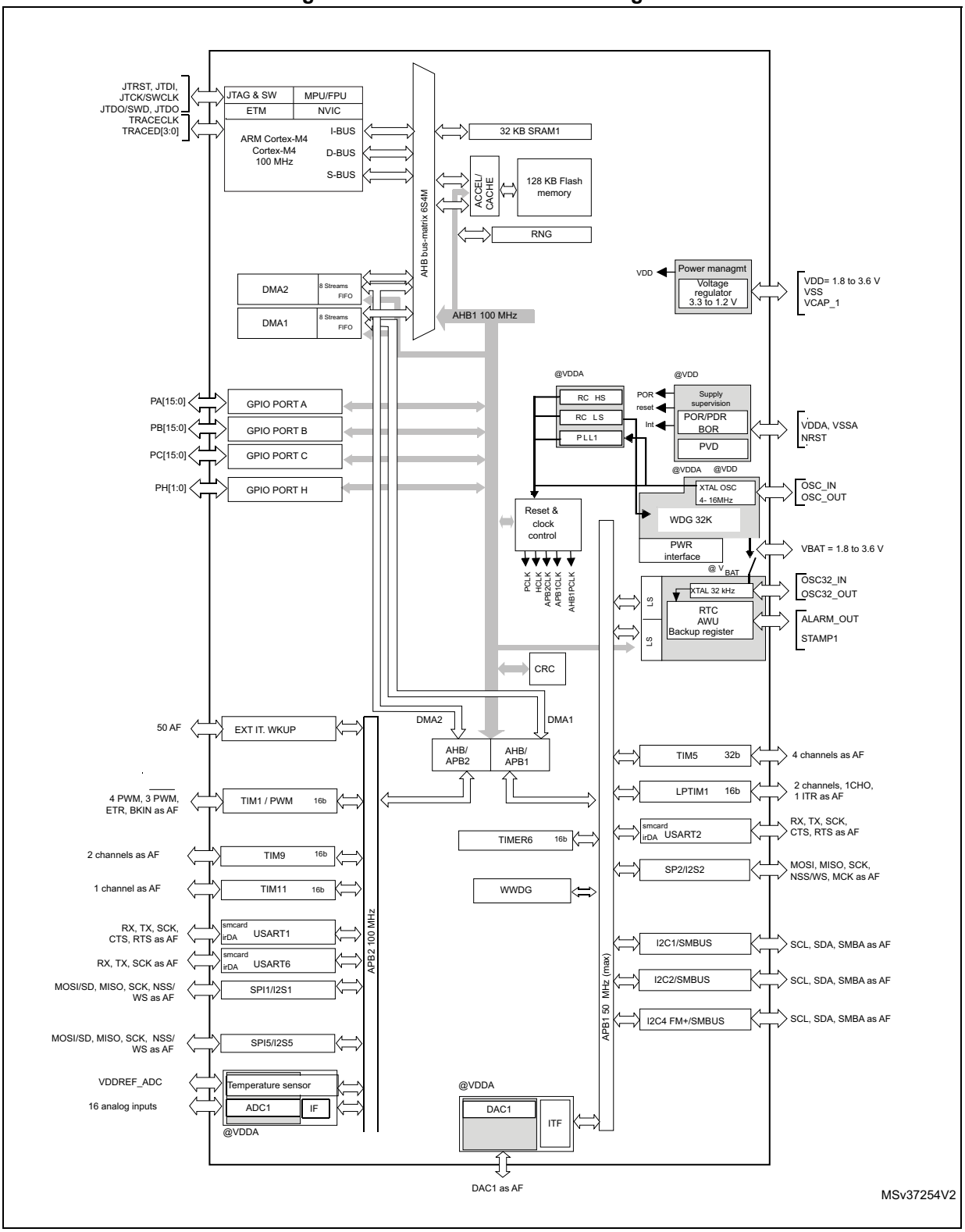
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410r8t6

Table 2. STM32F410x8/B features and peripheral counts

Peripherals		STM32 F410 T8Y	STM32 F410 TBY	STM32 F410 C8U	STM32 F410 CBU	STM32 F410 C8T	STM32 F410 CBT	STM32 F410 R8T	STM32 F410 RBT	STM32 F410 R8I	STM32 F410 RBI
Flash memory in Kbytes		64	128	64	128	64	128	64	128	64	128
SRAM in Kbytes	System	32									
Timers	General-purpose	4									
	Low-power timer	1									
	Advanced-control	1									
Random number generator		1									
Communication interfaces	SPI/ I^2S	1	3								
	I^2C	2	3								
	USART	2	3								
GPIOs		23	36					50			
12-bit ADC Number of channels		1									
		4	10					16			
12-bit DAC Number of channels		1 1									
Maximum CPU frequency		100 MHz									
Operating voltage		1.7 to 3.6 V	1.8 to 3.6 V			1.7 to 3.6 V		1.8 to 3.6 V		1.7 to 3.6 V	
Operating temperatures		Ambient temperatures: – 40 to +85 °C / – 40 to + 105 °C / – 40 to + 125 °C									
		Junction temperature: –40 to + 130 °C									
Package		WLCSP36	UFQFPN48			LQFP48		LQFP64		UFBGA64	

Figure 2. STM32F410x8/B block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 100 MHz.

Table 7. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X(1)	X	X	X	X	6.25	12.5	APB2 (max. 100 MHz)
USART2	X	X(1)	X	X(1)	X	X(1)	3.12	6.25	APB1 (max. 50 MHz)
USART6 (1)	X	N.A	X	X(1)(2)	X	X(1)(2)	6.25	12.5	APB2 (max. 50 MHz)

1. Not available on WLCSP36 package.
2. Not available on UFQFPN48 package.

3.23 Serial peripheral interface (SPI)

The devices feature three SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 and SPI5 can communicate at up to 50 Mbit/s, SPI2 can communicate at up to 25 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.24 Inter-integrated sound (I^2S)

Three standard I^2S interfaces (multiplexed with SPI1 to SPI5) are available. They can be operated in master or slave mode, in simplex communication modes and can be configured to operate with a 16-/32-bit resolution as an input or output channel. All the I2Sx audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

3.25 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

- Triangular-wave generation
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channel is triggered through TIM6 update output that is also connected to different DMA channels.

3.30 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

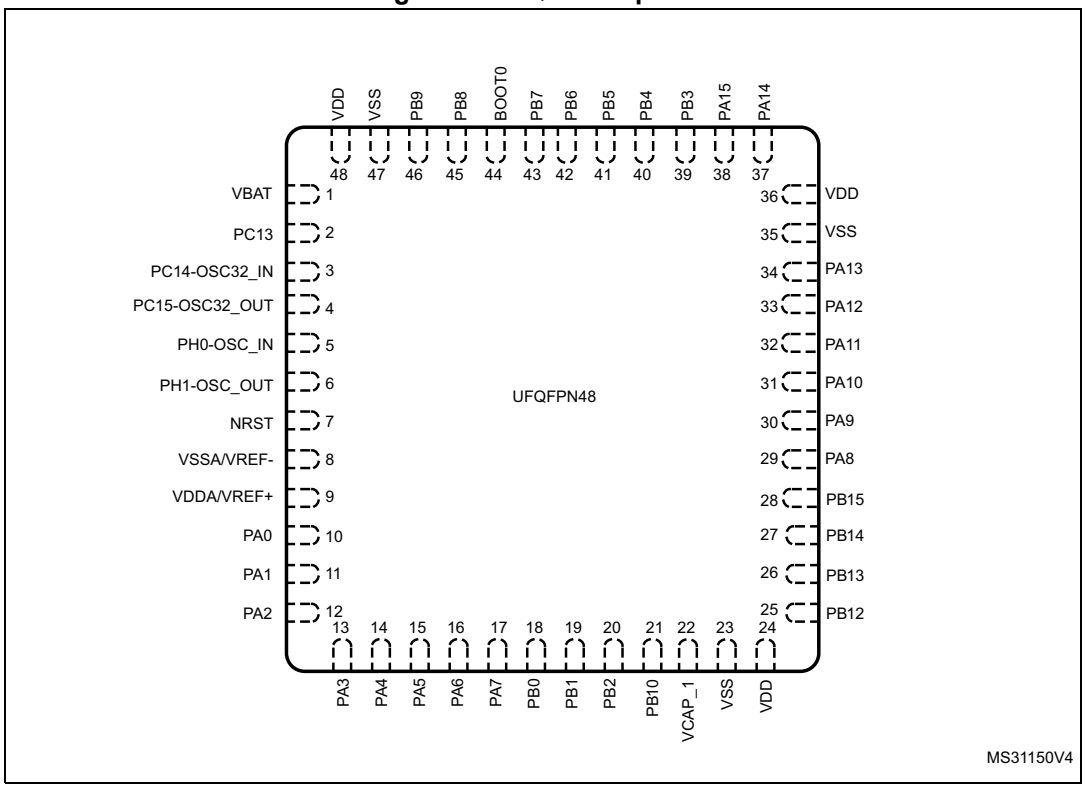
Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.31 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F410x8/B through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

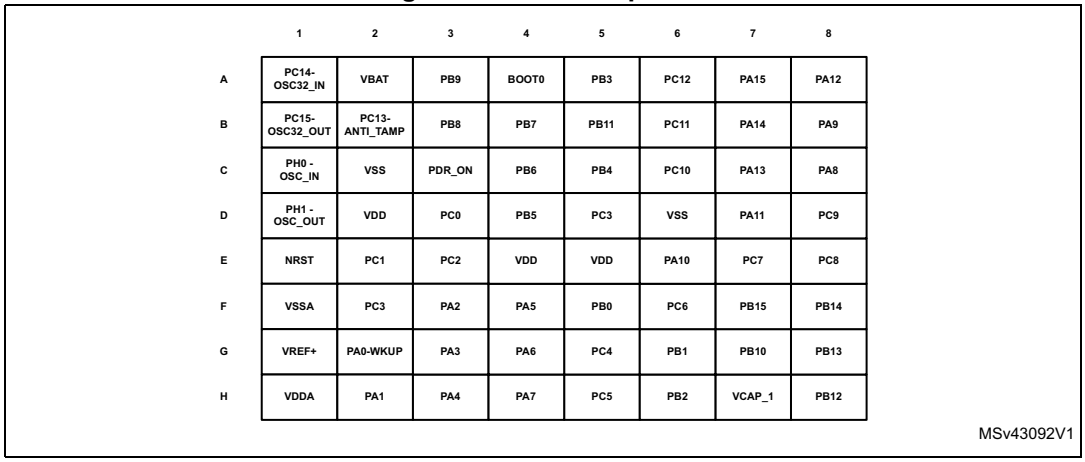
The Embedded Trace Macrocell operates with third party debugger software tools.

Figure 7. UFQFPN48 pinout



1. The above figure shows the package top view.

Figure 8. UFBGA64 pinout



1. The above figure shows the package top view.

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/LPTIM1	TIM5	TIM9/ TIM11	I2C1/I2C2 /I2C4	SPI1/I2S1/S PI2/I2S2	SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5	USART1/ USART2	USART6	I2C2/ I2C4	-	-	-	-	-	SYS_AF
Port B	PB0	-	TIM1_CH2N	-	-	-	-	SPI5_SCK/ I2S5_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	-	-	-	-	SPI5_NSS/ I2S5_WS	-	-	-	-	-	-	-	-	EVENTOUT
	PB2	-	LPTIM1_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO-SWO	-	-	-	I2C4_ SDA	SPI1_SCK/I 2S1_CK	-	USART1_ RX	-	I2C2_ SDA	-	-	-	-	-	EVENTOUT
	PB4	JTRST	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	LPTIM1_IN1	-	-	I2C1_ SMBA	SPI1_MOSI /I2S1_SD	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB6	-	LPTIM1_ETR	-	-	I2C1_ SCL	-	-	USART1_ TX	-	-	-	-	-	-	-	EVENTOUT
	PB7	-	LPTIM1_IN2	-	-	I2C1_ SDA	-	-	USART1_ RX	-	-	-	-	-	-	-	EVENTOUT
	PB8	-	LPTIM1_OUT	-	-	I2C1_ SCL	-	SPI5_MOSI /I2S5_SD	-	-	-	-	-	-	-	-	EVENTOUT
	PB9	-	-	-	TIM11_ CH1	I2C1_ SDA	SPI2_NSS/ I2S2_WS	-	-	-	I2C2_ SDA	-	-	-	-	-	EVENTOUT
	PB10	-	-	-	-	I2C2_ SCL	SPI2_SCK/ I2S2_CK	I2S1_MCK	-	-	I2C4_ SCL	-	-	-	-	-	EVENTOUT
	PB11	TRACED3	-	TIM5_ CH4	-	I2C2_ SDA	I2S2_CKIN	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	TIM5_ CH1	-	I2C2_ SMBA	SPI2_NSS/ I2S2_WS	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C4_ SMBA	SPI2_SCK /I2S2_CK	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	-	I2C4_ SDA	SPI2_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB15	RTC_ 50Hz	TIM1_CH3N	-	-	I2C4_ SCL	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 15. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_D	Maximum allowed package power dissipation at T_A = 85 °C (range 6) or 105 °C (range 7)(7)	LQFP48	-	-	364	mW
		LQFP64	-	-	435	
		UFQFPN48	-	-	606	
		WLCSP36	-	-	328	
		UFBGA64	-	-	253	
	Power dissipation at T_A = 125 °C for range 3(7)	LQFP48	-	-	91	
		LQFP64	-	-	108	
		UFQFPN48	-	-	151	
		WLCSP36	-	-	81	
		UFBGA64	-	-	63	
T_A	Ambient temperature for range 6	Maximum power dissipation	–40	-	85	°C
		Low power dissipation(8)	–40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	–40	-	105	
		Low power dissipation(8)	–40	-	125	
	Ambient temperature for range 3	Maximum power dissipation	-40	-	110	
		Low power dissipation(8)	-40	-	130	
T_J	Junction temperature range	Range 6	–40	-	105	
		Range 7	–40	-	125	
		Range 3	–40	-	130	

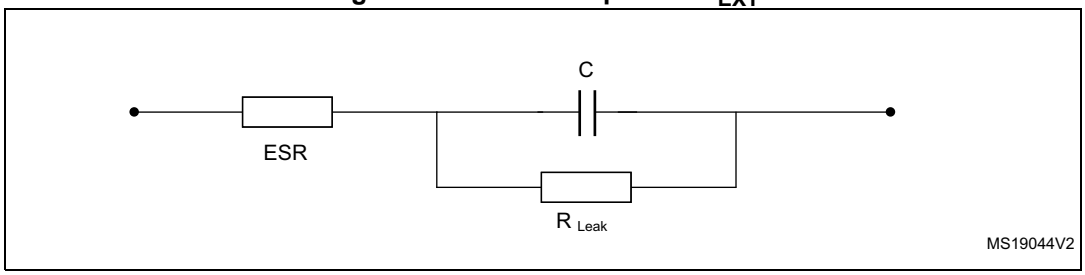
1. V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. When the ADC is used, refer to *Table 66: ADC characteristics*.
3. If VREF+ pin is present, it must respect the following condition: VDDA-VREF+ < 1.2 V.
4. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
5. Guaranteed by test in production.
6. To sustain a voltage higher than VDD+0.3, the internal Pull-up and Pull-Down resistors must be disabled
7. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}.
8. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax}.

6.3.2 VCAP_1 external capacitor

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 pin.

C_{EXT} is specified in *Table 17*.

Figure 15. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 17. VCAP_1 operating conditions

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	4.7 µF
ESR	ESR of external capacitor	< 1 Ω

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 19. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} rise time rate	Power-up	20	∞	
	V_{CAP_1} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 20* are derived from tests performed under ambient temperature and V_{DD} supply voltage @ 3.3V.

Table 20. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60(1)	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}$(2)	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}$(2)(3)	POR reset timing	-	0.5	1.5	3.0	ms

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(3)(4), External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	8.0	8.2(5)	9.0	9.4(6)	10.2(5)	mA
			84	S2	168	6.5	6.7	7.4	7.7	8.5	
			64	S3	128	4.6	4.7	5.2	5.5	6.3	
			50	S3	100	3.7	3.9	4.3	4.6	5.4	
			25	S3	100	2.2	2.3	2.6	2.9	3.8	
			20	S3	160	2.1	2.2	2.5	2.8	3.6	
		All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	1.1	1.2	1.5	1.9	2.7	
			1	S3	off	0.3	0.4	0.7	1.1	1.9	
		All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON	100	S1	200	8.4	8.7	9.5	9.9	10.7	
			84	S2	168	6.9	7.1	7.7	8.1	8.9	
			64	S3	128	4.9	5.1	5.5	5.9	6.7	
			50	S3	100	4.0	4.2	4.6	4.9	5.7	
			25	S3	100	2.5	2.6	2.9	3.2	4.0	
			20	S3	160	2.4	2.5	2.7	3.1	3.9	
		All peripherals enabled(3), HSI, PLL OFF, Flash memory ON	16	S3	off	1.4	1.4	1.8	2.2	3.0	
			1	S3	off	0.6	0.6	1.0	1.3	2.0	

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 52. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions		Class	Maximum value(2)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/JEDEC JS-001		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	UFQFPN48	4	500	
			WLCSP36	3	250	
			LQFP48	4	500	
			LQPF64	4	500	
			UFBGA64	TBD	TBD	

1. TBD stands for “to be defined”.
2. Guaranteed by characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 53. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Table 56. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6 V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 13*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 28* and *Table 57*, respectively.

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 57. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns

Table 64. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	11	13	ns
		Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	-	11	18.5	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge), 1.7 V < V_{DD} < 3.6 V	8	-	-	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	4	6	ns
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	0	-	-	ns

1. Guaranteed by characterization.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 32. SPI timing diagram - slave mode and CPHA = 0

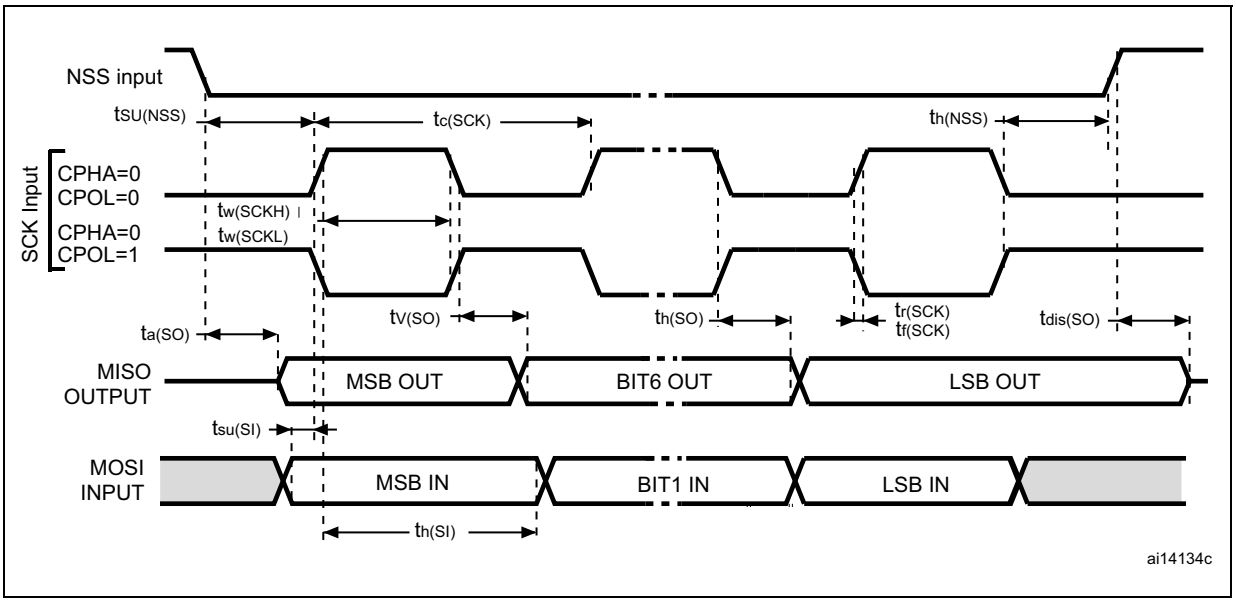


Table 68. ADC accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, $V_{DDA} - V_{REF}$ < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization.

Table 69. ADC accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization.

Table 70. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz $V_{DDA} = V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization.

Table 71. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz $V_{DDA} = V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

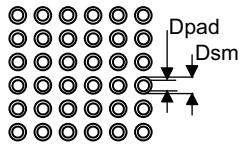
1. Guaranteed by characterization.

Table 79. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.518	2.553	2.588	0.1012	0.1026	0.1039
E	2.544	2.579	2.614	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-
F	-	0.2765	-	-	0.0119	-
G	-	0.2895	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

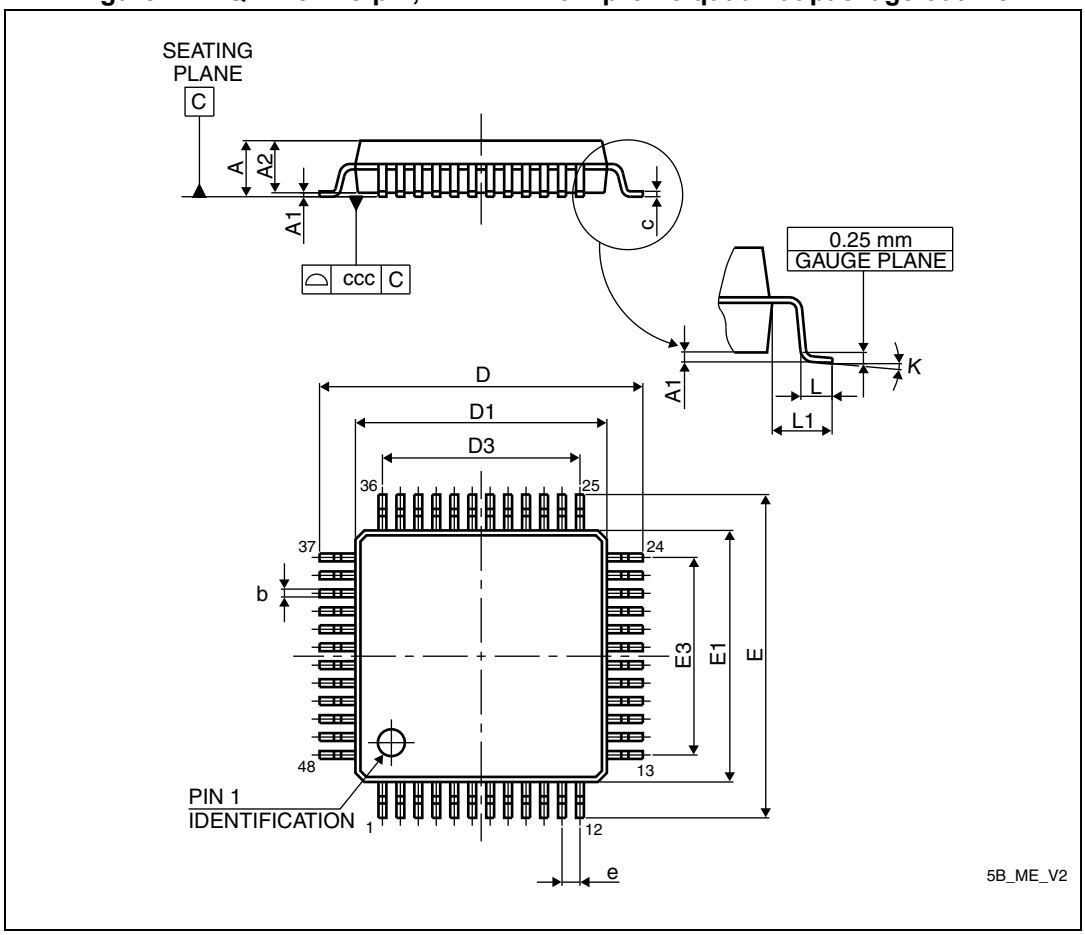
Figure 42. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



A05F_FP_V1

7.3 LQFP48 package information

Figure 47. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



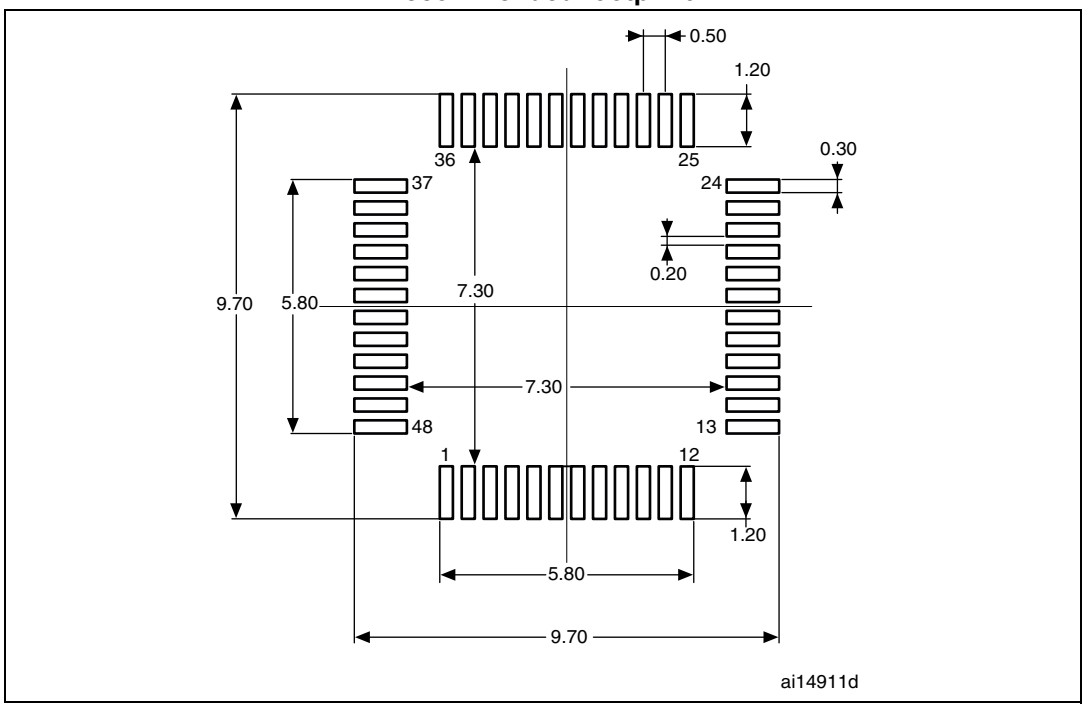
1. Drawing is not to scale.

Table 82. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3	-	5.500	-	-	0.2165	-
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



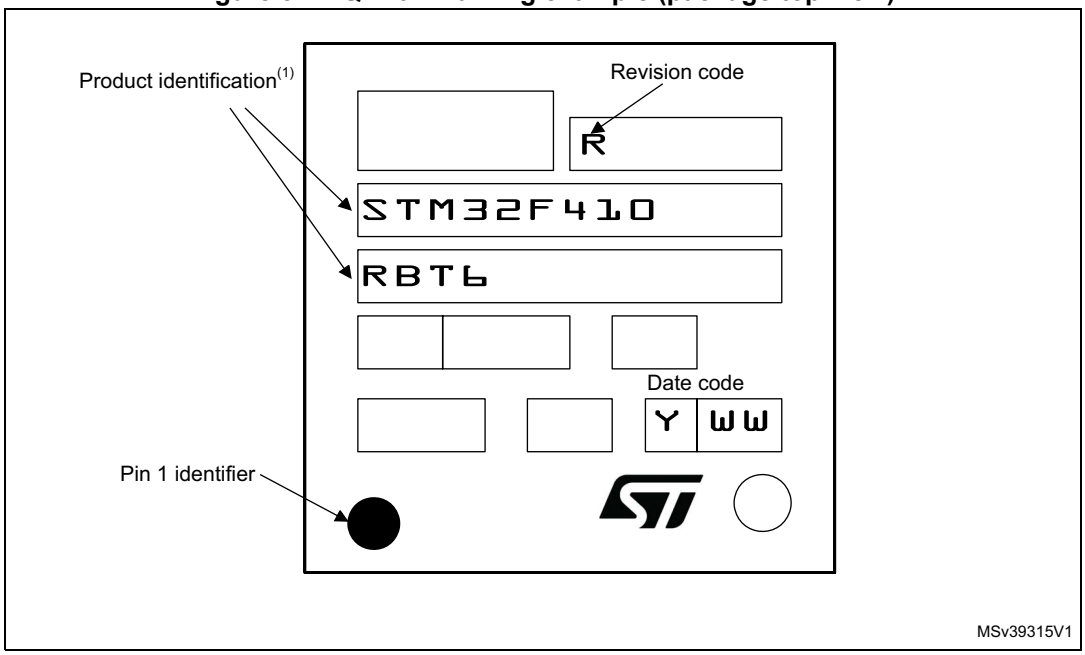
1. Dimensions are expressed in millimeters.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 52. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Appendix B Application block diagrams

B.1 Sensor Hub application example

Figure 56. Sensor hub application example 1

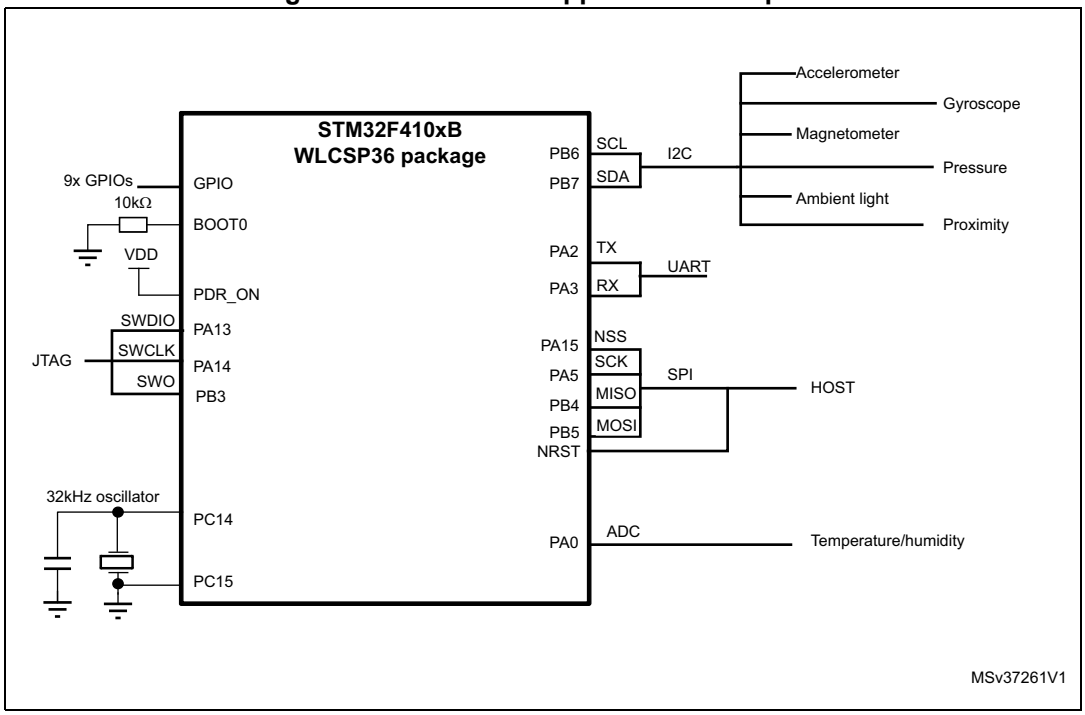


Figure 57. Sensor hub application example 2