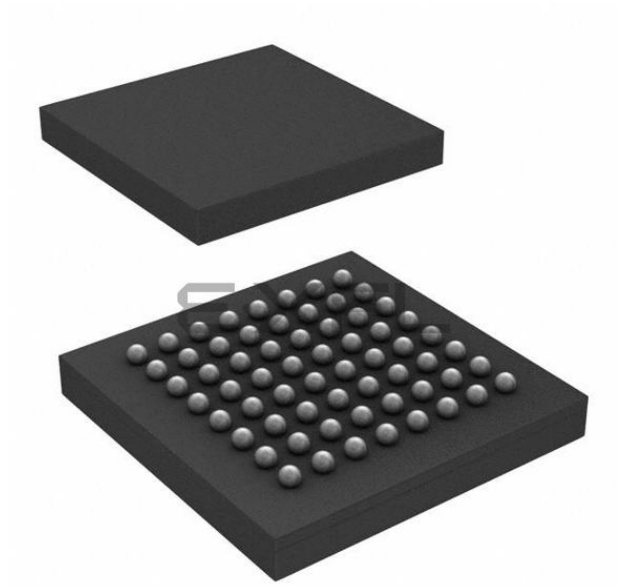

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410rbi3

List of tables

3.20.4 Low-power timer (LPTIM1)

The devices embed one low-power timer. This timer features an independent clock and runs in Stop mode if it is clocked by LSE, LSI or by an external clock. It is able to wake up the system from Stop mode.

The low-power timer main features are the following:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI or APB1 clock
  - External clock source over LPTIM input (working even when no internal clock source is running and used by pulse-counter applications).
- Programmable digital glitch filter
- Encoder mode
- Active in Stop mode.

3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.20.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

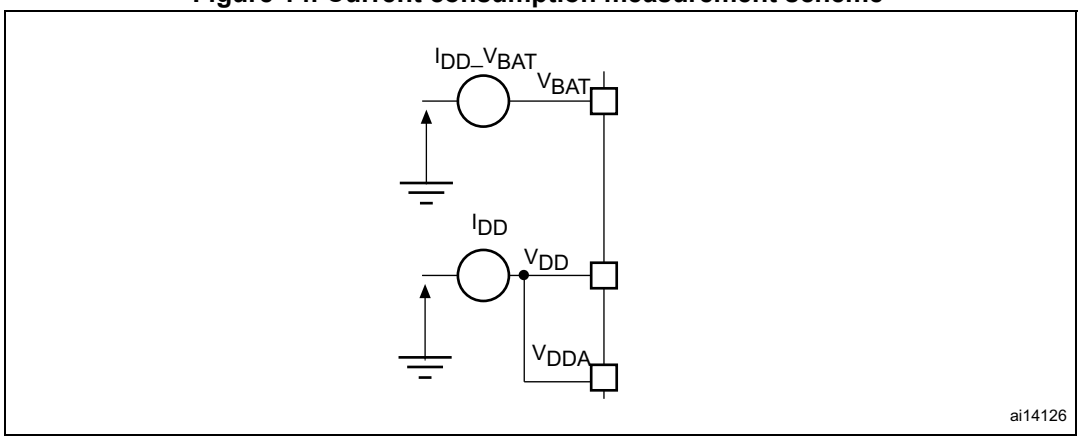
- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/LPTIM1	TIM5	TIM9/ TIM11	I2C1/I2C2 /I2C4	SPI1/I2S1/S PI2/I2S2	SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5	USART1/ USART2	USART6	I2C2/ I2C4	-	-	-	-	-	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC4	-	-	-	TIM9_ CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	-	TIM9_ CH2	I2C4_ SMBA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC6	TRACE CLK	-	-	-	I2C4_ SCL	I2S2_MCK	-	-	USART6 _TX	-	-	-	-	-	-	EVENTOUT
	PC7	-	-	-	-	I2C4_ SDA	SPI2_SCK/ I2S2_CK	I2S1_MCK	-	USART6 _RX	-	-	-	-	-	-	EVENTOUT
	PC8	-	-	-	-	-	-	-	-	USART6 _CK	-	-	-	-	-	-	EVENTOUT
	PC9	MCO_2	-	-	-	I2C4_ SDA	I2S2_CKIN	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC10	TRACED0	-	TIM5_ CH2	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC11	TRACED1	-	TIM5_ CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC12	TRACED2	-	-	TIM11_ CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 12: Voltage characteristics*, *Table 13: Current characteristics*, and *Table 14: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 12. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA}, V_{DD} and V_{BAT})(1)	–0.3	4.0	V
V_{IN}	Input voltage on FT and TC pins(2)	V_{SS}–0.3	V_{DD}+4.0	
	Input voltage on any other pin	V_{SS}–0.3	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.14: Absolute maximum ratings (electrical sensitivity)*		V

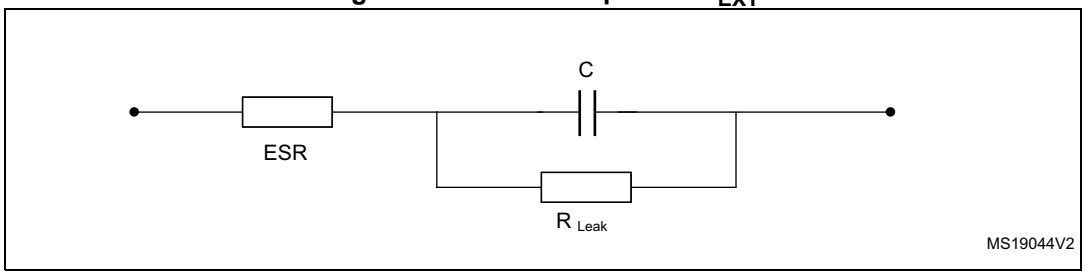
1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to *Table 13* for the values of the maximum allowed injected current.

6.3.2 VCAP_1 external capacitor

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 pin.

C_{EXT} is specified in *Table 17*.

Figure 15. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 17. VCAP_1 operating conditions

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor	4.7 µF
ESR	ESR of external capacitor	< 1 Ω

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A.

Table 18. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	µs/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A.

Table 19. Operating conditions at power-up / power-down (regulator OFF)(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	µs/V
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} rise time rate	Power-up	20	∞	
	V_{CAP_1} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	16.3	17.3(5)	17.1	17.5(6)	18.4(5)	mA
			84	S2	168	13.2	14.1	14.0	14.3	15.2	
			64	S3	128	9.3	10.0	9.9	10.2	11.1	
			50	S3	100	7.4	8.0	8.0	8.3	9.2	
			25	S3	100	4.2	4.7	4.8	5.0	5.9	
			20	S3	160	3.7	4.2	4.3	4.6	5.5	
		HSI, PLL OFF, all peripherals enabled(3)(4)	16	S3	off	2.4	2.8	3.0	3.4	4.3	
			1	S3	off	0.6	1.0	1.2	1.5	2.4	
		External clock, all peripherals disabled(3)	100	S1	200	10.6	11.4(5)	11.4	11.7(6)	12.6(5)	
			84	S2	168	8.7	9.4	9.3	9.7	10.6	
			64	S3	128	6.2	6.8	6.8	7.1	7.9	
			50	S3	100	5.0	5.5	5.5	5.8	6.8	
			25	S3	100	2.9	3.4	3.5	3.8	4.7	
			20	S3	160	2.7	3.1	3.2	3.5	4.4	
		HSI, PLL OFF, all peripherals disabled(3)	16	S3	off	1.7	2.1	2.3	2.6	3.5	
			1	S3	off	0.6	0.9	1.1	1.5	2.4	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production on temperature range 7 salestypes only.

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(3)(4), External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	8.0	8.2(5)	9.0	9.4(6)	10.2(5)	mA
			84	S2	168	6.5	6.7	7.4	7.7	8.5	
			64	S3	128	4.6	4.7	5.2	5.5	6.3	
			50	S3	100	3.7	3.9	4.3	4.6	5.4	
			25	S3	100	2.2	2.3	2.6	2.9	3.8	
			20	S3	160	2.1	2.2	2.5	2.8	3.6	
		All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	1.1	1.2	1.5	1.9	2.7	
			1	S3	off	0.3	0.4	0.7	1.1	1.9	
		All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON	100	S1	200	8.4	8.7	9.5	9.9	10.7	
			84	S2	168	6.9	7.1	7.7	8.1	8.9	
			64	S3	128	4.9	5.1	5.5	5.9	6.7	
			50	S3	100	4.0	4.2	4.6	4.9	5.7	
			25	S3	100	2.5	2.6	2.9	3.2	4.0	
			20	S3	160	2.4	2.5	2.7	3.1	3.9	
		All peripherals enabled(3), HSI, PLL OFF, Flash memory ON	16	S3	off	1.4	1.4	1.8	2.2	3.0	
			1	S3	off	0.6	0.6	1.0	1.3	2.0	

Table 30. Typical and maximum current consumptions in Stop mode - V_{DD} = 1.7 V

Symbol	Conditions		Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	105.6	117.1	385.1	665.7	1270.0	µA
		Low power regulator usage	39.5	48.7	287.5	548.4	1070.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	77.8	87.5	351.3	630.1	1222.0	
		Low power regulator usage	11.0	20.0	254.2	512.0	1006.0	
		Low power low voltage regulator usage	6.1	13.6	217.0	442.5	941.0	

1. Guaranteed by characterization.

Table 31. Typical and maximum current consumption in Stop mode - V_{DD}=3.6 V

Symbol	Conditions		Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	108.6	126(2)	392.8	675.4(3)	1280.0(2)	µA
		Low power regulator usage	41.03	50.31(2)	290.9	554.2(3)	1077.0(2)	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	80.32	94.0(2)	357.0	639.5(3)	1232.0(2)	
		Low power regulator usage	12.41	21.5(2)	258.1	518.1(3)	1010.0(2)	
		Low power low voltage regulator usage	7.53	15.2(2)	221.6	449.2(3)	947.0(2)	

1. Guaranteed by characterization.
2. Guaranteed by tests in production.
3. Guaranteed by test in production on temperature range 7 salestypes only.

Table 32. Typical and maximum current consumption in Standby mode - V_{DD}= 1.7 V

Symbol	Parameter	Conditions	Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE) and RTC ON	2.1	2.9	6.5	18.2	60.0	µA
		RTC and LSE OFF	1.2	1.9	5.5	17.1	59.0	

1. Guaranteed by characterization, unless otherwise specified.

Table 36. Peripheral current consumption (continued)

Peripheral		I_{DD} (Typ)			Unit
		Voltage scale1	Voltage scale2	Voltage scale3	
APB2 (up to 100 MHz)	APB2 to AHB	0,22	0,19	0,17	µA/MHz
	TIM1	6,62	6,36	5,66	
	USART1	3,19	3,10	2,77	
	USART6	3,10	2,99	2,66	
	ADC1	3,35	3,25	2,88	
	SPI1/I2S1	1,82	1,77	1,58	
	SYSCFG	0,83	0,81	0,72	
	EXTI	0,92	0,88	0,80	
	TIM9	2,90	2,81	2,48	
	TIM11	2,13	2,06	1,81	
	SPI5/I2S5	1,88	1,83	1,59	
Bus matrix		1.91	1.82	1.64	

1. Valid if all the DMA streams are activated (please refer to the reference manual RM0401).

Table 44. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization.

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 52. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions		Class	Maximum value(2)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/JEDEC JS-001		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	UFQFPN48	4	500	
			WLCSP36	3	250	
			LQFP48	4	500	
			LQPF64	4	500	
			UFBGA64	TBD	TBD	

1. TBD stands for “to be defined”.
2. Guaranteed by characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 53. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Table 56. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6 V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 13*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 13* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization results.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 28* and *Table 57*, respectively.

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 57. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns

Table 66. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Guaranteed by characterization.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 66*.

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 67. ADC accuracy at f_{ADC} = 18 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V V_{DDA} –V_{REF} < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization.

Table 68. ADC accuracy at f_{ADC} = 30 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, $V_{DDA} - V_{REF}$ < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±4	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization.

Table 69. ADC accuracy at f_{ADC} = 36 MHz(1)

Symbol	Parameter	Test conditions	Typ	Max(2)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Better performance could be achieved in restricted V_{DD}, frequency and temperature ranges.
2. Guaranteed by characterization.

Table 70. ADC dynamic accuracy at f_{ADC} = 18 MHz - limited test conditions(1)

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} =18 MHz $V_{DDA} = V_{REF+}$= 1.7 V Input Frequency = 20 KHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization.

Table 71. ADC dynamic accuracy at f_{ADC} = 36 MHz - limited test conditions(1)

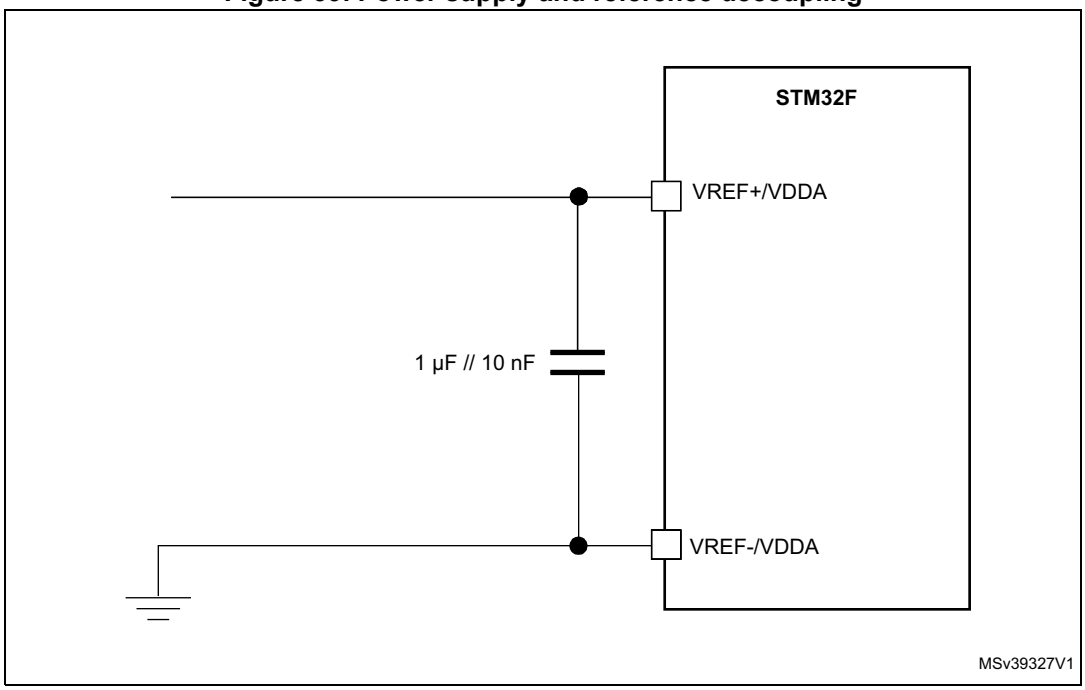
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	f_{ADC} = 36 MHz $V_{DDA} = V_{REF+}$ = 3.3 V Input Frequency = 20 KHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 39*. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 39. Power supply and reference decoupling



6.3.21 Temperature sensor characteristics

Table 72. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L (1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization.
2. Guaranteed by design.

Table 73. Temperature sensor calibration values

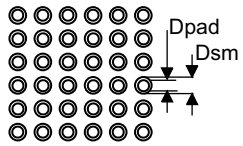
Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

Table 79. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.518	2.553	2.588	0.1012	0.1026	0.1039
E	2.544	2.579	2.614	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-
F	-	0.2765	-	-	0.0119	-
G	-	0.2895	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

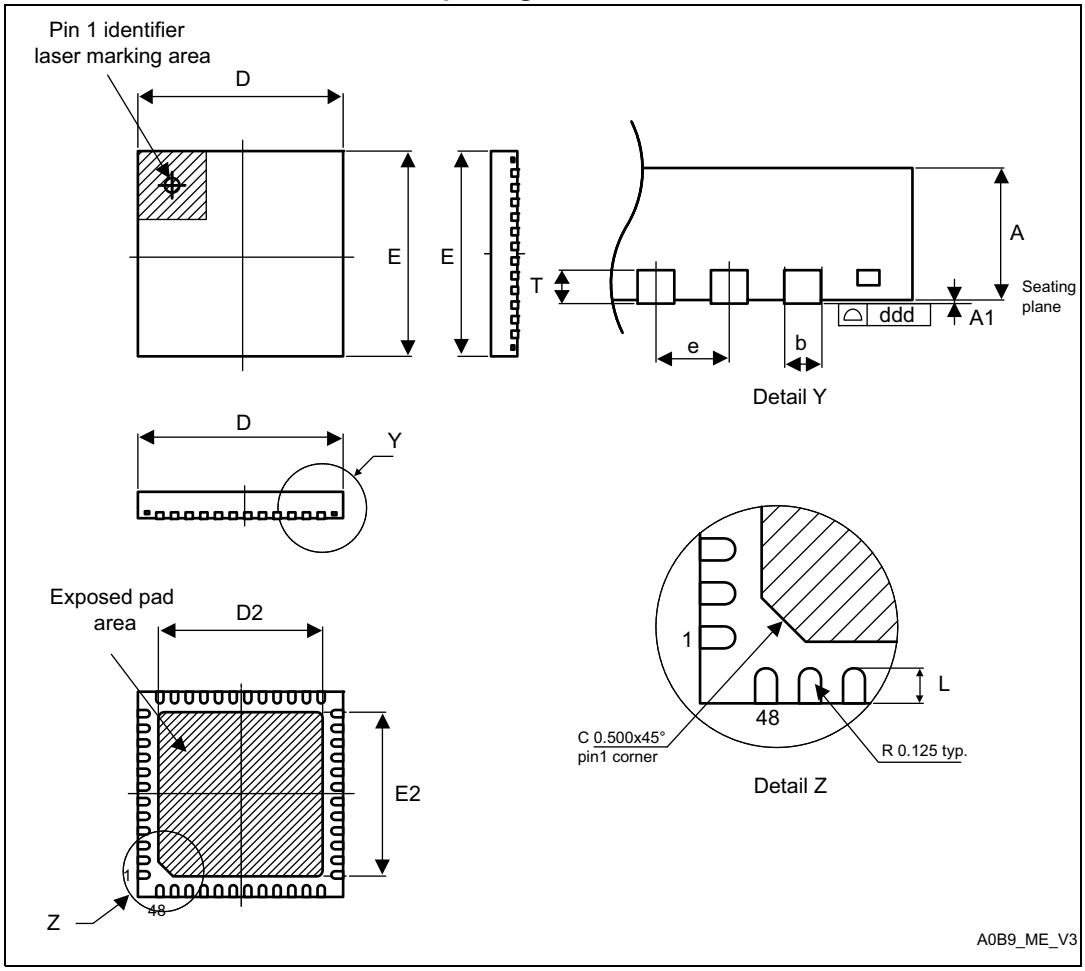
Figure 42. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



A05F_FP_V1

7.2 UFQFPN48 package information

Figure 44. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Revision history

Table 89. Document revision history

Date	Revision	Changes
28-Sep-2015	1	Initial release.
07-Dec-2015	2	Junction temperature range changed to –40 to + 110 °C for WLCSP49 package. Updated *Figure 7: UFQFPN48 pinout*.
10-Aug-2016	3	Updated: – *Table 2: STM32F410x8/B features and peripheral counts* – *Table 9: STM32F410x8/B pin definitions* – *Table 14: Thermal characteristics* – *Table 15: General operating conditions* – *Table 20: Embedded reset and power control block characteristics* – Tables from *Table 21: Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - VDD = 1.7 V* to *Table 34: Typical and maximum current consumptions in VBAT mode (LSE and RTC ON, LSE low- drive mode)* – *Table 42: HSI oscillator characteristics* – *Table 43: LSI oscillator characteristics* – *Table 49: Flash memory endurance and data retention* – *Table 52: ESD absolute maximum ratings* – *Table 55: I/O static characteristics* – *Table 66: ADC characteristics* – *Table 75: Embedded internal reference voltage* – *Table 77: DAC characteristics* – *Table 87: Ordering information scheme* – *Figure 16: Typical VBAT current consumption (LSE and RTC ON/LSE oscillator in “low power” mode selection* – *Section 7: Package information* Added: – *Figure 5: LQFP48 pinout* – *Figure 8: UFBGA64 pinout* – *Figure 49: LQFP48 marking example (package top view)* – *Figure 55: UFBGA64 marking example (package top view)*