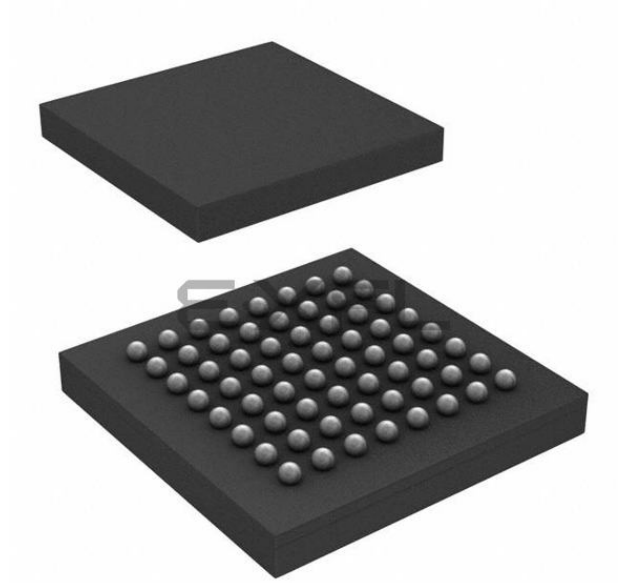

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA
Supplier Device Package	64-UFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410rbi6

3.4 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.5 Embedded Flash memory

The devices embed up to 128 Kbytes of Flash memory available for storing programs and data, plus 512 bytes of OTP memory organized in 16 blocks which can be independently locked.

To optimize the power consumption the Flash memory can also be switched off in Run or in Sleep mode (see *Section 3.18: Low-power modes*).

Two modes are available: Flash in Stop mode or in DeepSleep mode (trade off between power saving and startup time.

Before disabling the Flash, the code must be executed from the internal RAM.

3.6 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.7 Embedded SRAM

All devices embed 32 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complemen-tary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced -control	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	100
General purpose	TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	100
	TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	100
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	50	100
Low-power	LPTIM1	16-bit	Up	Between 1 and 128	No	2	No	50	100

Table 9. STM32F410x8/B pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP36	LQFP48	UFQFPN48	LQFP64	UFBGA64						
E3	21	21	29	G7	PB10	I/O	FT	-	I2C2_SCL, SPI2_SCK/I2S2_CK, I2S1_MCK, I2C4_SCL, EVENTOUT	-
E2	22	22	30	H7	VCAP_1	S	-	-	-	-
F2	23	23	31	D6	VSS	S	-	-	-	-
F1	24	24	32	E5	VDD	S	-	-	-	-
E1	25	25	33	H8	PB12	I/O	FT	-	TIM1_BKIN, TIM5_CH1, I2C2_SMBA, SPI2_NSS/I2S2_WS, EVENTOUT	-
-	26	26	34	G8	PB13	I/O	FT	-	TIM1_CH1N, I2C4_SMBA, SPI2_SCK/I2S2_CK, EVENTOUT	-
-	27	27	35	F8	PB14	I/O	FT	-	TIM1_CH2N, I2C4_SDA, SPI2_MISO, EVENTOUT	-
-	28	28	36	F7	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, I2C4_SCL, SPI2_MOSI/I2S2_SD, EVENTOUT	-
-	-	-	37	F6	PC6	I/O	FT	-	TRACECLK, I2C4_SCL, I2S2_MCK, USART6_TX, EVENTOUT	-
-	-	-	38	E7	PC7	I/O	FT	-	I2C4_SDA, SPI2_SCK/I2S2_CK, I2S1_MCK, USART6_RX, EVENTOUT	-
-	-	-	39	E8	PC8	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	40	D8	PC9	I/O	FT	-	MCO_2, I2C4_SDA, I2S2_CKIN, EVENTOUT	-

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/LPTIM1	TIM5	TIM9/ TIM11	I2C1/I2C2 /I2C4	SPI1/I2S1/S PI2/I2S2	SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5	USART1/ USART2	USART6	I2C2/ I2C4	-	-	-	-	-	SYS_AF
Port B	PB0	-	TIM1_CH2N	-	-	-	-	SPI5_SCK/ I2S5_CK	-	-	-	-	-	-	-	-	EVENTOUT
	PB1	-	TIM1_CH3N	-	-	-	-	SPI5_NSS/ I2S5_WS	-	-	-	-	-	-	-	-	EVENTOUT
	PB2	-	LPTIM1_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB3	JTDO-SWO	-	-	-	I2C4_ SDA	SPI1_SCK/I 2S1_CK	-	USART1_ RX	-	I2C2_ SDA	-	-	-	-	-	EVENTOUT
	PB4	JTRST	-	-	-	-	SPI1_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB5	-	LPTIM1_IN1	-	-	I2C1_ SMBA	SPI1_MOSI /I2S1_SD	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB6	-	LPTIM1_ETR	-	-	I2C1_ SCL	-	-	USART1_ TX	-	-	-	-	-	-	-	EVENTOUT
	PB7	-	LPTIM1_IN2	-	-	I2C1_ SDA	-	-	USART1_ RX	-	-	-	-	-	-	-	EVENTOUT
	PB8	-	LPTIM1_OUT	-	-	I2C1_ SCL	-	SPI5_MOSI /I2S5_SD	-	-	-	-	-	-	-	-	EVENTOUT
	PB9	-	-	-	TIM11_ CH1	I2C1_ SDA	SPI2_NSS/ I2S2_WS	-	-	-	I2C2_ SDA	-	-	-	-	-	EVENTOUT
	PB10	-	-	-	-	I2C2_ SCL	SPI2_SCK/ I2S2_CK	I2S1_MCK	-	-	I2C4_ SCL	-	-	-	-	-	EVENTOUT
	PB11	TRACED3	-	TIM5_ CH4	-	I2C2_ SDA	I2S2_CKIN	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB12	-	TIM1_BKIN	TIM5_ CH1	-	I2C2_ SMBA	SPI2_NSS/ I2S2_WS	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB13	-	TIM1_CH1N	-	-	I2C4_ SMBA	SPI2_SCK /I2S2_CK	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB14	-	TIM1_CH2N	-	-	I2C4_ SDA	SPI2_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PB15	RTC_ 50Hz	TIM1_CH3N	-	-	I2C4_ SCL	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 13. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	-160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	-120	
$I_{INJ(PIN)}$ (3)	Injected current on FT and TC pins (4)	–5/+0	
	Injected current on NRST and B pins (4)		
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 14. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	130	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP36, LQFP48, LQFP64, UFQFPN48, UFBGA64)	see note (1)	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

Table 16. Features depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states (1)(2)	I/O operation	Clock output frequency on I/O pins(3)	Possible Flash memory operations
V_{DD} =1.7 to 2.1 V(4)	Conversion time up to 1.2 Msps	16 MHz(5)	100 MHz with 6 wait states	– No I/O compensation	up to 30 MHz	8-bit erase and program operations only
V_{DD} = 2.1 to 2.4 V	Conversion time up to 1.2 Msps	18 MHz	100 MHz with 5 wait states	– No I/O compensation	up to 30 MHz	16-bit erase and program operations
V_{DD} = 2.4 to 2.7 V	Conversion time up to 2.4 Msps	24 MHz	100 MHz with 4 wait states	– I/O compensation works	up to 50 MHz	16-bit erase and program operations
V_{DD} = 2.7 to 3.6 V	Conversion time up to 2.4 Msps	30 MHz	100 MHz with 3 wait states	– I/O compensation works	– up to 100 MHz when V_{DD} = 3.0 to 3.6 V – up to 50 MHz when V_{DD} = 2.7 to 3.0 V	32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. Refer to *Table 57: I/O AC characteristics* for frequencies vs. external load.
4. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
5. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.

Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	16.3	17.3(5)	17.1	17.5(6)	18.4(5)	mA
			84	S2	168	13.2	14.1	14.0	14.3	15.2	
			64	S3	128	9.3	10.0	9.9	10.2	11.1	
			50	S3	100	7.4	8.0	8.0	8.3	9.2	
			25	S3	100	4.2	4.7	4.8	5.0	5.9	
			20	S3	160	3.7	4.2	4.3	4.6	5.5	
		HSI, PLL OFF, all peripherals enabled(3)(4)	16	S3	off	2.4	2.8	3.0	3.4	4.3	
			1	S3	off	0.6	1.0	1.2	1.5	2.4	
		External clock, all peripherals disabled(3)	100	S1	200	10.6	11.4(5)	11.4	11.7(6)	12.6(5)	
			84	S2	168	8.7	9.4	9.3	9.7	10.6	
			64	S3	128	6.2	6.8	6.8	7.1	7.9	
			50	S3	100	5.0	5.5	5.5	5.8	6.8	
			25	S3	100	2.9	3.4	3.5	3.8	4.7	
			20	S3	160	2.7	3.1	3.2	3.5	4.4	
		HSI, PLL OFF, all peripherals disabled(3)	16	S3	off	1.7	2.1	2.3	2.6	3.5	
			1	S3	off	0.6	0.9	1.1	1.5	2.4	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production on temperature range 7 salestypes only.

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD} (continued)	Supply current in **Sleep mode** (continued)	All peripherals disabled, External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	2.2	2.3(5)	2.6	3.0(6)	3.8(5)	mA
			84	S2	168	1.8	1.9	2.2	2.6	3.4	
			64	S3	128	1.4	1.5	1.8	2.1	2.9	
			50	S3	100	1.2	1.3	1.6	1.9	2.7	
			25	S3	100	0.9	1.0	1.3	1.7	2.5	
			20	S3	160	1.0	1.2	1.4	1.7	2.5	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.3	0.4	0.7	1.1	1.9	
			1	S3	off	0.3	0.3	0.7	1.0	1.8	
		All peripherals disabled, External clock, PLL ON, Flash memory ON	100	S1	200	2.6	2.7	3.0	3.4	4.2	
			84	S2	168	2.2	2.3	2.6	3.0	3.8	
			64	S3	128	1.8	1.9	2.1	2.5	3.3	
			50	S3	100	1.5	1.6	1.9	2.2	3.1	
			25	S3	100	1.2	1.4	1.6	2.0	2.8	
			20	S3	160	1.3	1.4	1.7	2.0	2.8	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.6	0.6	1.0	1.3	2.0	
			1	S3	off	0.5	0.6	0.9	1.3	2.0	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production on temperature range 7 salestypes only.

Table 29. Typical and maximum current consumption in Sleep mode - V_{DD} = 1.7 V (continued)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz)(1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD} (continued)	Supply current in **Sleep mode** (continued)	All peripherals disabled, External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	1.9	2,0	2,4	2,7	3.5	mA
			84	S2	168	1.6	1,7	2,0	2,4	3.2	
			64	S3	128	1.1	1,2	1,5	1,9	2.7	
			50	S3	100	0.9	1,0	1,3	1,7	2.5	
			25	S3	100	0.7	0,8	1,1	1,4	2.2	
			20	S3	160	0.8	0,8	1,2	1,5	2.3	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.3	0,4	0,7	1,0	1.8	
			1	S3	off	0.2	0,3	0,6	1,0	1.8	
		All peripherals disabled, External clock, PLL ON, Flash memory ON	100	S1	200	2.3	2,4	2,9	3,3	4.0	
			84	S2	168	2.0	2,1	2,4	2,8	3.6	
			64	S3	128	1.5	1,6	1,9	2,3	3.1	
			50	S3	100	1.3	1,4	1,7	2,0	2.8	
			25	S3	100	1.0	1,1	1,4	1,7	2.5	
			20	S3	160	1.0	1,2	1,5	1,8	2.6	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.6	0,6	1,0	1,4	2.1	
			1	S3	off	0.5	0,6	0,9	1,3	2.0	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

Table 30. Typical and maximum current consumptions in Stop mode - V_{DD} = 1.7 V

Symbol	Conditions		Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	105.6	117.1	385.1	665.7	1270.0	µA
		Low power regulator usage	39.5	48.7	287.5	548.4	1070.0	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	77.8	87.5	351.3	630.1	1222.0	
		Low power regulator usage	11.0	20.0	254.2	512.0	1006.0	
		Low power low voltage regulator usage	6.1	13.6	217.0	442.5	941.0	

1. Guaranteed by characterization.

Table 31. Typical and maximum current consumption in Stop mode - V_{DD}=3.6 V

Symbol	Conditions		Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	108.6	126(2)	392.8	675.4(3)	1280.0(2)	µA
		Low power regulator usage	41.03	50.31(2)	290.9	554.2(3)	1077.0(2)	
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	80.32	94.0(2)	357.0	639.5(3)	1232.0(2)	
		Low power regulator usage	12.41	21.5(2)	258.1	518.1(3)	1010.0(2)	
		Low power low voltage regulator usage	7.53	15.2(2)	221.6	449.2(3)	947.0(2)	

1. Guaranteed by characterization.
2. Guaranteed by tests in production.
3. Guaranteed by test in production on temperature range 7 salestypes only.

Table 32. Typical and maximum current consumption in Standby mode - V_{DD}= 1.7 V

Symbol	Parameter	Conditions	Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE) and RTC ON	2.1	2.9	6.5	18.2	60.0	µA
		RTC and LSE OFF	1.2	1.9	5.5	17.1	59.0	

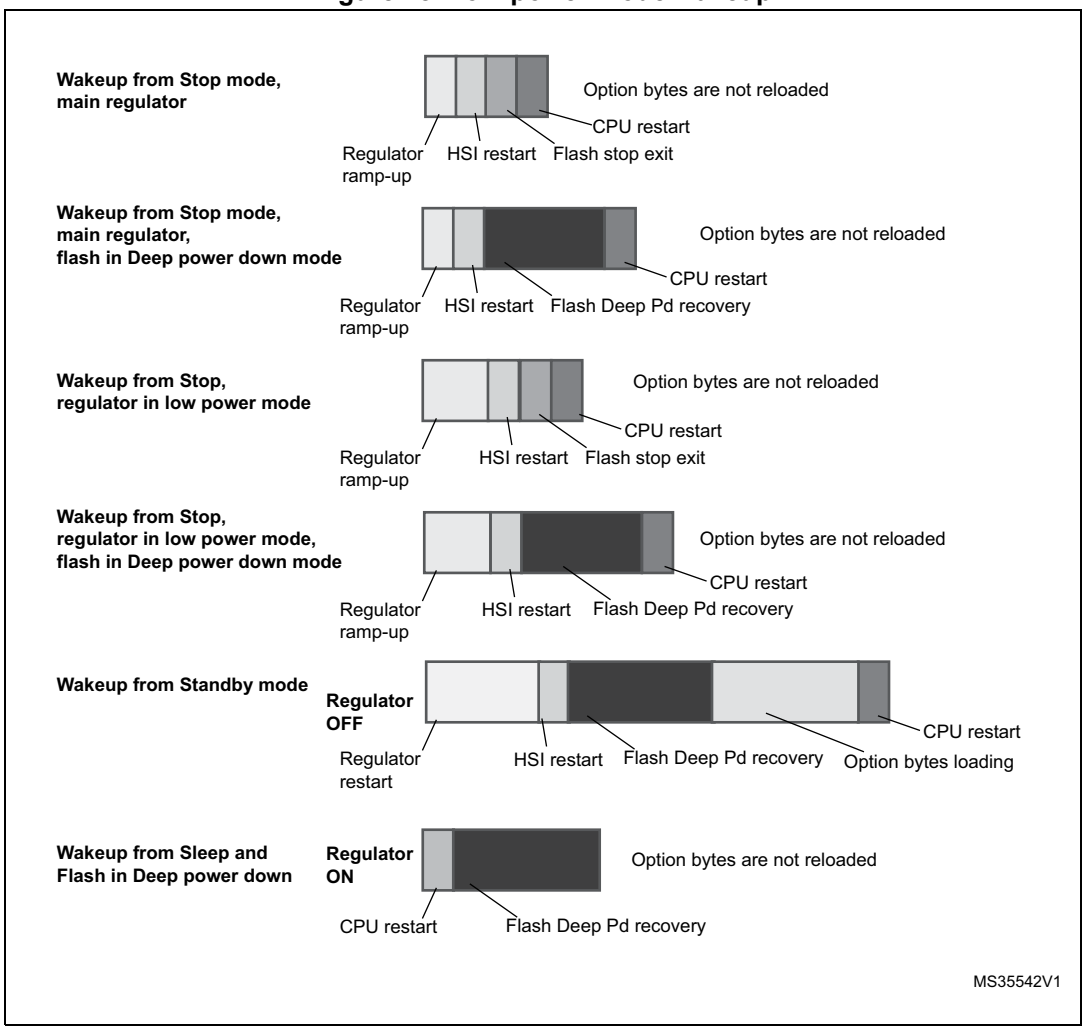
1. Guaranteed by characterization, unless otherwise specified.

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 37* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

Figure 18. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

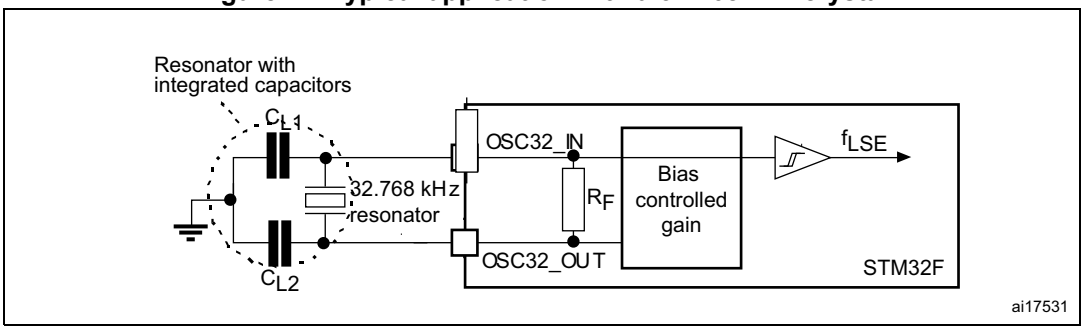
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	µA
		High-drive mode	-	-	3	
G_m_crit_max	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	µA/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}$ (2)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0401.

Figure 22. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in *Table 42* and *Table 43* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

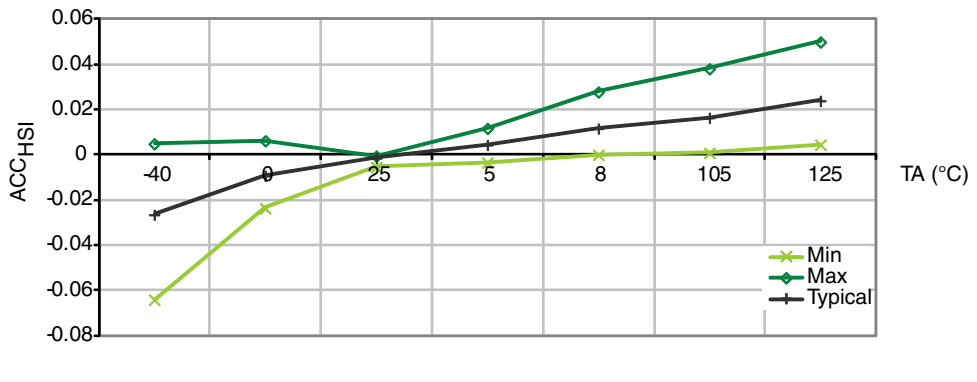
High-speed internal (HSI) RC oscillator

Table 42. HSI oscillator characteristics (1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	16	-	MHz
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1	%
		Factory-calibrated	T_A = –40 to 125 °C(3)	–8	-	5.5	%
			T_A = –10 to 85 °C(3)	–4	-	4	%
			T_A = 25 °C(4)	–1	-	1	%
$t_{su(HSI)}$(2)	HSI oscillator startup time	-		-	2.2	4	µs
$I_{DD(HSI)}$(2)	HSI oscillator power consumption	-		-	60	80	µA

1. V_{DD} = 3.3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. Factory calibrated non-soldered parts.

Figure 23. ACC_{HSI} versus temperature



1. Guaranteed by characterization.

Table 44. Main PLL characteristics (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LOCK}	PLL lock time	VCO freq = 100 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	
$I_{DD(PLL)}$(4)	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz		0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}$(4)	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz		0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization.

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 52. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions		Class	Maximum value(2)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/JEDEC JS-001		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	UFQFPN48	4	500	
			WLCSP36	3	250	
			LQFP48	4	500	
			LQPF64	4	500	
			UFBGA64	TBD	TBD	

1. TBD stands for “to be defined”.
2. Guaranteed by characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 53. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Table 62. SCL frequency (f_{PCLK1}= 42 MHz.,V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 31. FMPI^{2}C timing diagram and measurement circuit

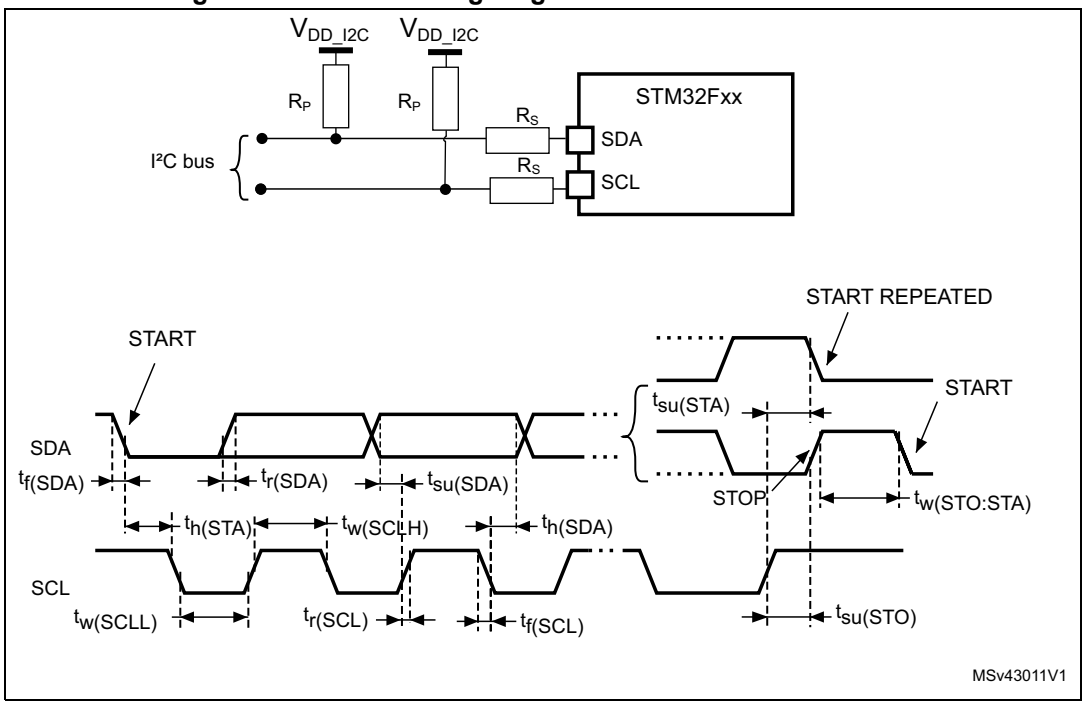
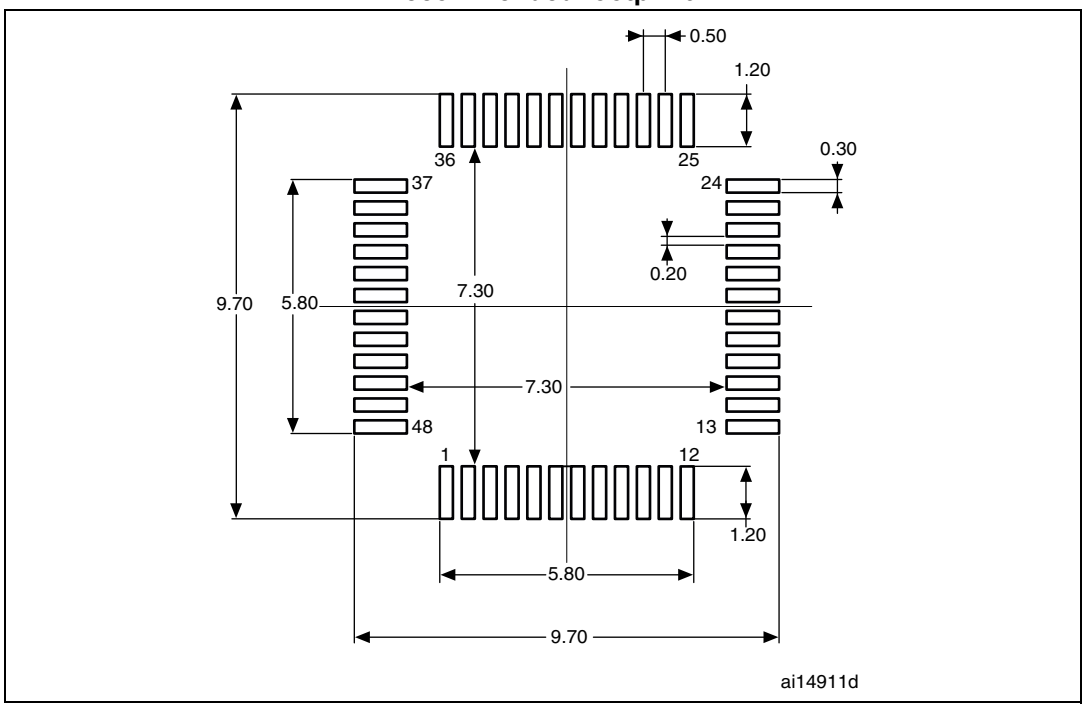


Figure 48. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



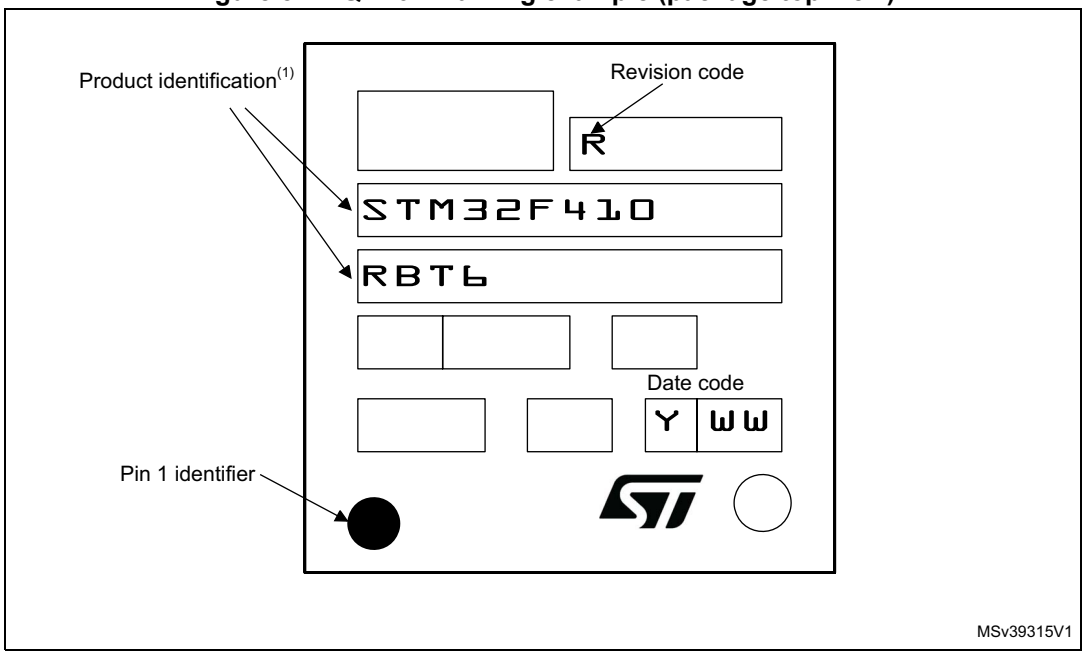
1. Dimensions are expressed in millimeters.

LQFP64 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 52. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Appendix A Recommendations when using the internal reset OFF

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BRO) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- VBAT functionality is no more available and VBAT pin should be connected to VDD.

A.1 Operating conditions

Table 88. Limitations depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait state ($f_{Flashmax}$)	Maximum Flash memory access frequency with no wait states(1) (2)	I/O operation	Possible Flash memory operations
V_{DD} = 1.7 to 2.1 V(3)	Conversion time up to 1.2 Msps	20 MHz(4)	100 MHz with 6 wait states	No I/O compensation	8-bit erase and program operations only

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART Accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART Accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to *Section 3.15.1: Internal reset ON*).
4. Prefetch is not available. Refer to AN3430 application note for details on how to adjust performance and power.