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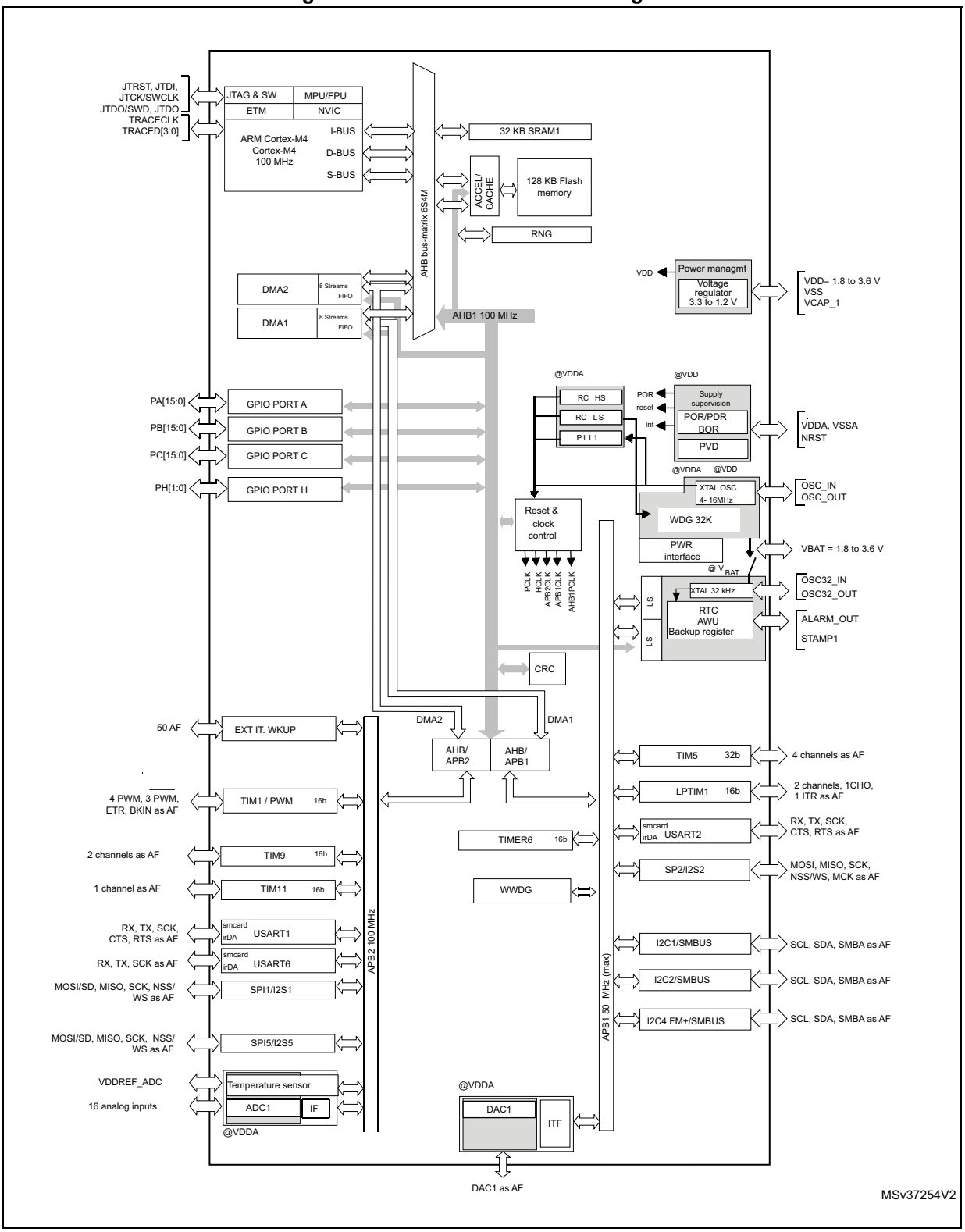
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410rbt6tr

Figure 2. STM32F410x8/B block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 100 MHz.

3.15 Power supply supervisor

3.15.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

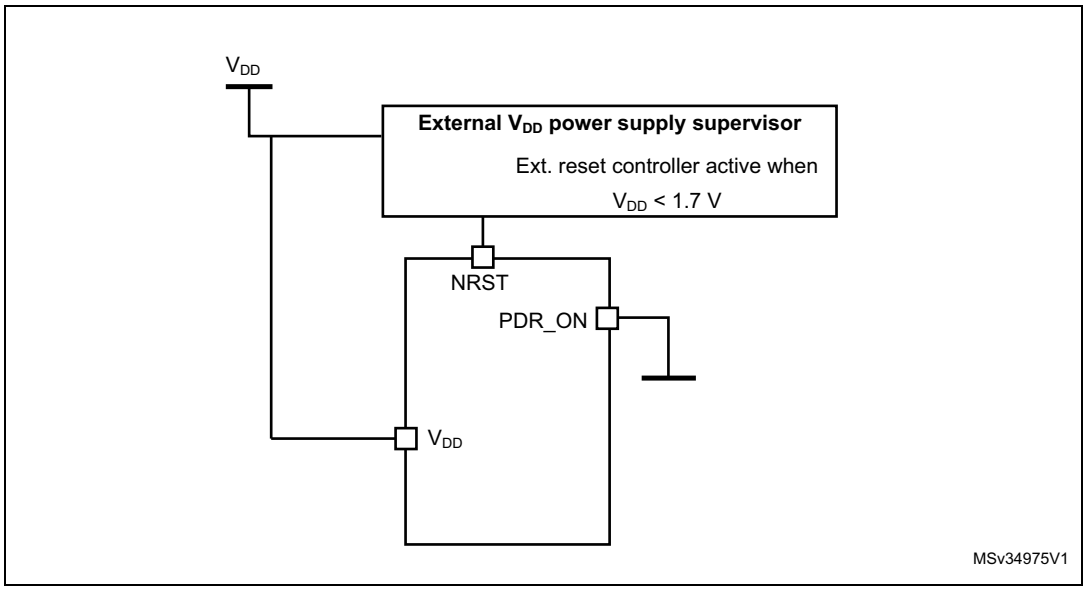
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available on WLCSP36 package only. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 4: Power supply supervisor interconnection with internal reset OFF*.

Figure 4. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available on WLCSP36 package only.

Table 5. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complemen-tary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced -control	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	100	100
General purpose	TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	50	100
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	100	100
	TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	100	100
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No	50	100
Low-power	LPTIM1	16-bit	Up	Between 1 and 128	No	2	No	50	100

3.21 Inter-integrated circuit interface (I^2C)

The devices feature up to three I^2C bus interfaces which can operate in multimaster and slave modes:

- One I^2C interface supports the Standard mode (up to 100 kHz), Fast-mode (up to 400 kHz) modes and Fast-mode plus (up to 1 MHz).
- Two I^2C interfaces support the Standard mode (up to 100 KHz) and the Fast mode (up to 400 KHz). Their frequency can be increased up to 1 MHz. For more details on the complete solution, refer to the nearest STMicroelectronics sales office.

All I^2C interfaces features 7/10-bit addressing mode and 7-bit addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 6*).

Table 6. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

3.22 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART6).

These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 12.5 Mbit/s. The USART2 interface communicates at up to 6.25 bit/s.

USART1 and USART2 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 9. STM32F410x8/B pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP36	LQFP48	UFQFPN48	LQFP64	UFBGA64						
E3	21	21	29	G7	PB10	I/O	FT	-	I2C2_SCL, SPI2_SCK/I2S2_CK, I2S1_MCK, I2C4_SCL, EVENTOUT	-
E2	22	22	30	H7	VCAP_1	S	-	-	-	-
F2	23	23	31	D6	VSS	S	-	-	-	-
F1	24	24	32	E5	VDD	S	-	-	-	-
E1	25	25	33	H8	PB12	I/O	FT	-	TIM1_BKIN, TIM5_CH1, I2C2_SMBA, SPI2_NSS/I2S2_WS, EVENTOUT	-
-	26	26	34	G8	PB13	I/O	FT	-	TIM1_CH1N, I2C4_SMBA, SPI2_SCK/I2S2_CK, EVENTOUT	-
-	27	27	35	F8	PB14	I/O	FT	-	TIM1_CH2N, I2C4_SDA, SPI2_MISO, EVENTOUT	-
-	28	28	36	F7	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, I2C4_SCL, SPI2_MOSI/I2S2_SD, EVENTOUT	-
-	-	-	37	F6	PC6	I/O	FT	-	TRACECLK, I2C4_SCL, I2S2_MCK, USART6_TX, EVENTOUT	-
-	-	-	38	E7	PC7	I/O	FT	-	I2C4_SDA, SPI2_SCK/I2S2_CK, I2S1_MCK, USART6_RX, EVENTOUT	-
-	-	-	39	E8	PC8	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	40	D8	PC9	I/O	FT	-	MCO_2, I2C4_SDA, I2S2_CKIN, EVENTOUT	-

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/LPTIM1	TIM5	TIM9/ TIM11	I2C1/I2C2 /I2C4	SPI1/I2S1/S PI2/I2S2	SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5	USART1/ USART2	USART6	I2C2/ I2C4	-	-	-	-	-	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC4	-	-	-	TIM9_ CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	-	TIM9_ CH2	I2C4_ SMBA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC6	TRACE CLK	-	-	-	I2C4_ SCL	I2S2_MCK	-	-	USART6 _TX	-	-	-	-	-	-	EVENTOUT
	PC7	-	-	-	-	I2C4_ SDA	SPI2_SCK/ I2S2_CK	I2S1_MCK	-	USART6 _RX	-	-	-	-	-	-	EVENTOUT
	PC8	-	-	-	-	-	-	-	-	USART6 _CK	-	-	-	-	-	-	EVENTOUT
	PC9	MCO_2	-	-	-	I2C4_ SDA	I2S2_CKIN	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC10	TRACED0	-	TIM5_ CH2	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC11	TRACED1	-	TIM5_ CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC12	TRACED2	-	-	TIM11_ CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 22. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	17.7	19.1(5)	19.3	19.7(6)	20.5(5)	mA
			84	S2	168	14.4	15.3(5)	15.7	16.0(6)	16.8(5)	
			64	S3	128	10.1	10.6(5)	11.0	11.3(6)	12.0(5)	
			50	S3	100	8.0	8.4	8.8	9.1	9.8	
			25	S3	100	4.4	4.7	4.9	5.2	5.9	
			20	S3	160	3.8	4.1	4.3	4.6	5.3	
		HSI, PLL off, all peripherals enabled(3)(4)	16	S3	off	2.5	2.6	2.9	3.2	4.0	
			1	S3	off	0.4	0.5	0.8	1.2	2.0	
		External clock, all peripherals disabled(3)	100	S1	200	12.1	13.1(5)	13.1	13.5(6)	14.3(5)	
			84	S2	168	9.8	10.6(5)	10.7	11.0(6)	11.8(5)	
			64	S3	128	7.0	7.4(5)	7.6	7.9(6)	8.6(5)	
			50	S3	100	5.6	5.9	6.1	6.4	7.2	
			25	S3	100	3.1	3.3	3.5	3.9	4.8	
			20	S3	160	2.8	3.0	3.2	3.5	4.4	
		HSI, PLL off, all peripherals disabled(3)	16	S3	off	1.7	1.8	2.1	2.4	3.3	
			1	S3	off	0.4	0.4	0.7	1.1	1.8	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production for temperature range 7 salestypes only.

Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	16.3	17.3(5)	17.1	17.5(6)	18.4(5)	mA
			84	S2	168	13.2	14.1	14.0	14.3	15.2	
			64	S3	128	9.3	10.0	9.9	10.2	11.1	
			50	S3	100	7.4	8.0	8.0	8.3	9.2	
			25	S3	100	4.2	4.7	4.8	5.0	5.9	
			20	S3	160	3.7	4.2	4.3	4.6	5.5	
		HSI, PLL OFF, all peripherals enabled(3)(4)	16	S3	off	2.4	2.8	3.0	3.4	4.3	
			1	S3	off	0.6	1.0	1.2	1.5	2.4	
		External clock, all peripherals disabled(3)	100	S1	200	10.6	11.4(5)	11.4	11.7(6)	12.6(5)	
			84	S2	168	8.7	9.4	9.3	9.7	10.6	
			64	S3	128	6.2	6.8	6.8	7.1	7.9	
			50	S3	100	5.0	5.5	5.5	5.8	6.8	
			25	S3	100	2.9	3.4	3.5	3.8	4.7	
			20	S3	160	2.7	3.1	3.2	3.5	4.4	
		HSI, PLL OFF, all peripherals disabled(3)	16	S3	off	1.7	2.1	2.3	2.6	3.5	
			1	S3	off	0.6	0.9	1.1	1.5	2.4	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production on temperature range 7 salestypes only.

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(3)(4), External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	8.0	8.2(5)	9.0	9.4(6)	10.2(5)	mA
			84	S2	168	6.5	6.7	7.4	7.7	8.5	
			64	S3	128	4.6	4.7	5.2	5.5	6.3	
			50	S3	100	3.7	3.9	4.3	4.6	5.4	
			25	S3	100	2.2	2.3	2.6	2.9	3.8	
			20	S3	160	2.1	2.2	2.5	2.8	3.6	
		All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	1.1	1.2	1.5	1.9	2.7	
			1	S3	off	0.3	0.4	0.7	1.1	1.9	
		All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON	100	S1	200	8.4	8.7	9.5	9.9	10.7	
			84	S2	168	6.9	7.1	7.7	8.1	8.9	
			64	S3	128	4.9	5.1	5.5	5.9	6.7	
			50	S3	100	4.0	4.2	4.6	4.9	5.7	
			25	S3	100	2.5	2.6	2.9	3.2	4.0	
			20	S3	160	2.4	2.5	2.7	3.1	3.9	
		All peripherals enabled(3), HSI, PLL OFF, Flash memory ON	16	S3	off	1.4	1.4	1.8	2.2	3.0	
			1	S3	off	0.6	0.6	1.0	1.3	2.0	

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD} (continued)	Supply current in **Sleep mode** (continued)	All peripherals disabled, External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	2.2	2.3(5)	2.6	3.0(6)	3.8(5)	mA
			84	S2	168	1.8	1.9	2.2	2.6	3.4	
			64	S3	128	1.4	1.5	1.8	2.1	2.9	
			50	S3	100	1.2	1.3	1.6	1.9	2.7	
			25	S3	100	0.9	1.0	1.3	1.7	2.5	
			20	S3	160	1.0	1.2	1.4	1.7	2.5	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.3	0.4	0.7	1.1	1.9	
			1	S3	off	0.3	0.3	0.7	1.0	1.8	
		All peripherals disabled, External clock, PLL ON, Flash memory ON	100	S1	200	2.6	2.7	3.0	3.4	4.2	
			84	S2	168	2.2	2.3	2.6	3.0	3.8	
			64	S3	128	1.8	1.9	2.1	2.5	3.3	
			50	S3	100	1.5	1.6	1.9	2.2	3.1	
			25	S3	100	1.2	1.4	1.6	2.0	2.8	
			20	S3	160	1.3	1.4	1.7	2.0	2.8	
		All peripherals disabled, HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	0.6	0.6	1.0	1.3	2.0	
			1	S3	off	0.5	0.6	0.9	1.3	2.0	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production on temperature range 7 salestypes only.

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 36. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Voltage scale1	Voltage scale2	Voltage scale3	
AHB1 (up to 100 MHz)	GPIOA	1.68	1.62	1.42	µA/MHz
	GPIOB	1.67	1.60	1.41	
	GPIOC	1.63	1.56	1.39	
	GPIOH	0.61	0.61	0.52	
	CRC	0.31	0.32	0.25	
	DMA1(1)	1.67N + 3.12	1.60N + 2.96	1.43N + 2.64	
	DMA2(1)	1.59N + 2.83	1.52N + 2.65	1.36N + 2.41	
	RNG	0.90	0.88	0.75	
APB1 (up to 50 MHz)	APB1 to AHB	0,78	0,74	0,63	µA/MHz
	TIM5	13,38	12,76	11,41	
	TIM6	2,14	1,98	1,75	
	LPTIM	8,22	7,88	7,06	
	WWDG	0,64	0,64	0,56	
	SPI2/I2S2	2,42	2,33	2,06	
	USART2	3,38	3,29	2,91	
	I2C1	3,46	3,33	2,97	
	I2C2	3,50	3,31	2,97	
	I2C4	4,82	4,64	4,09	
	PWR	0,66	0,64	0,62	
	DAC	0,84	0,81	0,78	

Figure 19. High-speed external clock source AC timing diagram

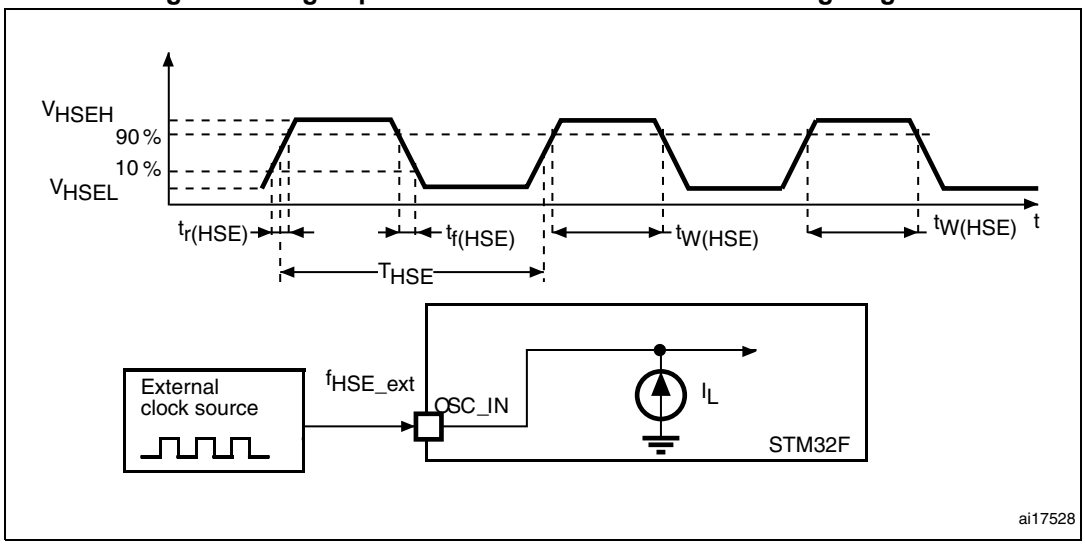
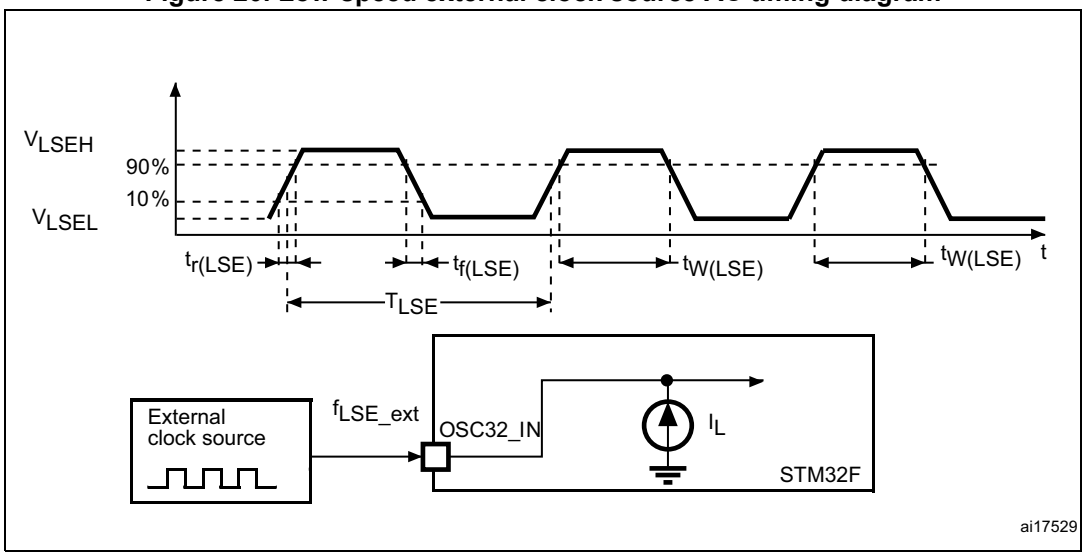


Figure 20. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 40*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 41. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) (1)

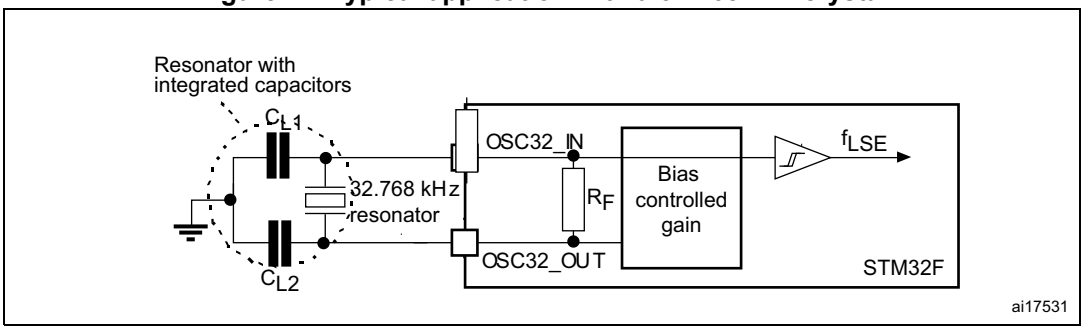
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	MΩ
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	µA
		High-drive mode	-	-	3	
G_m_crit_max	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	µA/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}$ (2)	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0401.

Figure 22. Typical application with a 32.768 kHz crystal



6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I²C characteristics are described in *Table 60*. Refer also to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.

Table 60. I²C characteristics

Symbol	Parameter	Standard mode I²C(1)(2)		Fast mode I²C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0	3450(3)	0	900(4)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
t_{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	0	50(5)	0	50(5)	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Table 62. SCL frequency (f_{PCLK1}= 42 MHz.,V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 65* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 65. I²S dynamic characteristics(1)

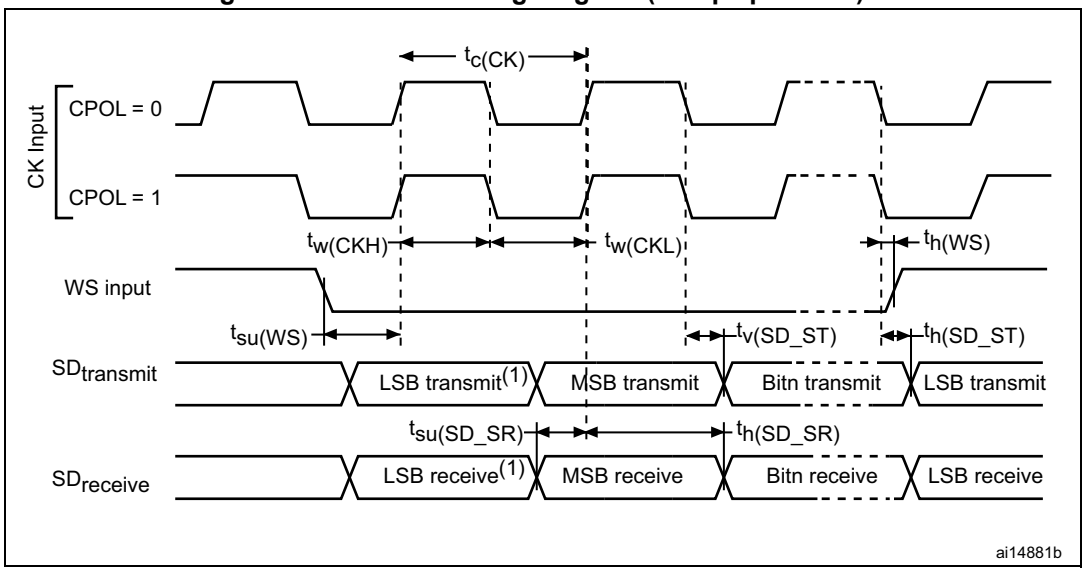
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	7	ns
$t_{h(WS)}$	WS hold time	Master mode	1.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	1.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	3	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	1	-	
$t_{su(SD\_SR)}$		Slave receiver	2.5	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	7	-	
$t_{h(SD\_SR)}$		Slave receiver	2.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	6	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	8	-	
$t_{h(SD\_MT)}$		Master transmitter (after enable edge)	2	-	

1. Guaranteed by characterization.
2. The maximum value of 256xFs is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0401 reference manual for more details on the sampling frequency (F_S).

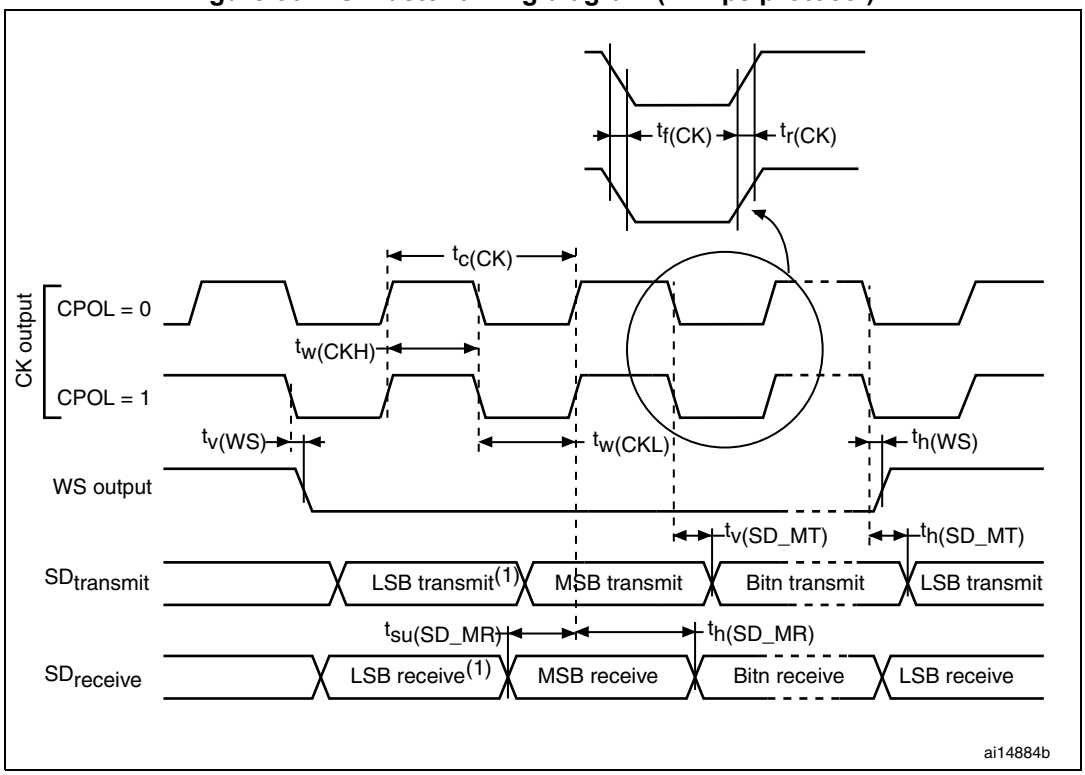
*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 35. I²S slave timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 36. I²S master timing diagram (Philips protocol)(1)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Table 80. WLCSP36 recommended PCB design rules (0.4 mm pitch)

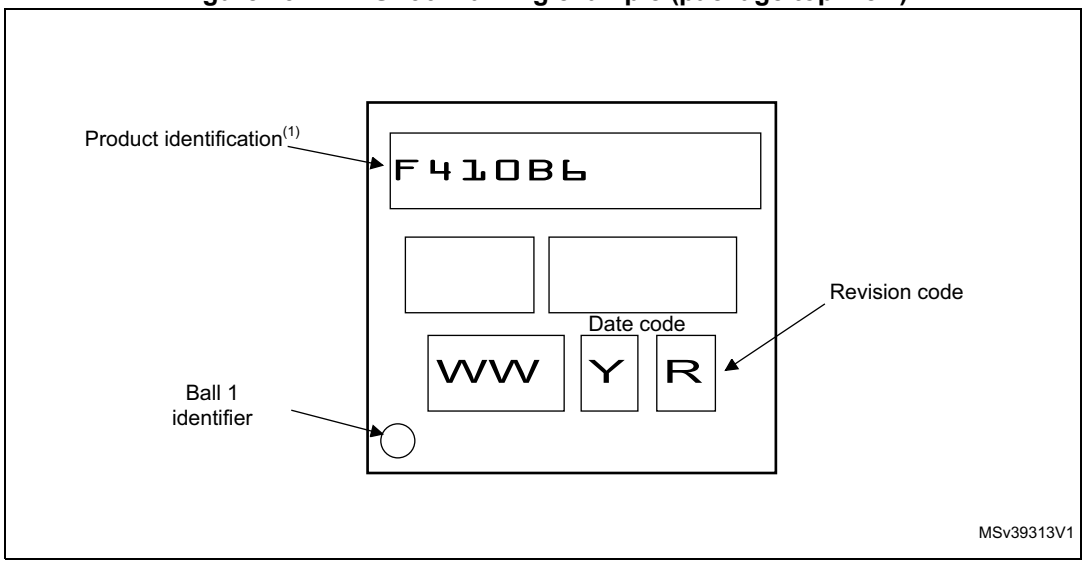
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

WLCSP36 device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

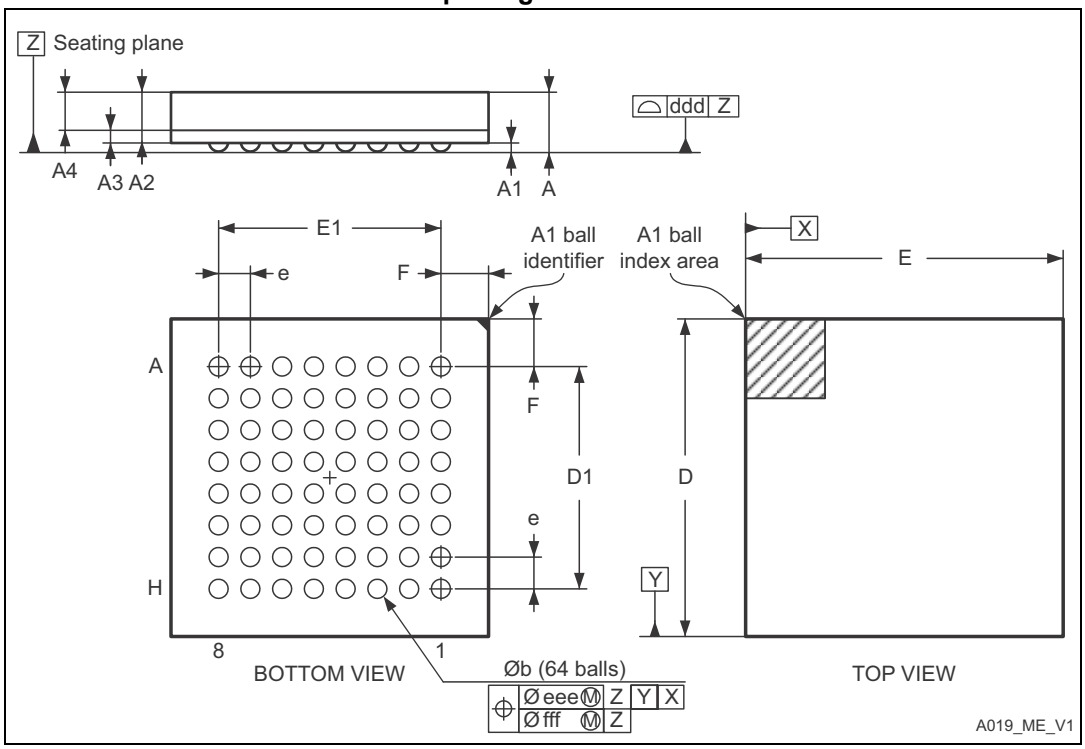
Figure 43. WLCSP36 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.5 UFBGA64 package information

Figure 53. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 84. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-

Appendix B Application block diagrams

B.1 Sensor Hub application example

Figure 56. Sensor hub application example 1

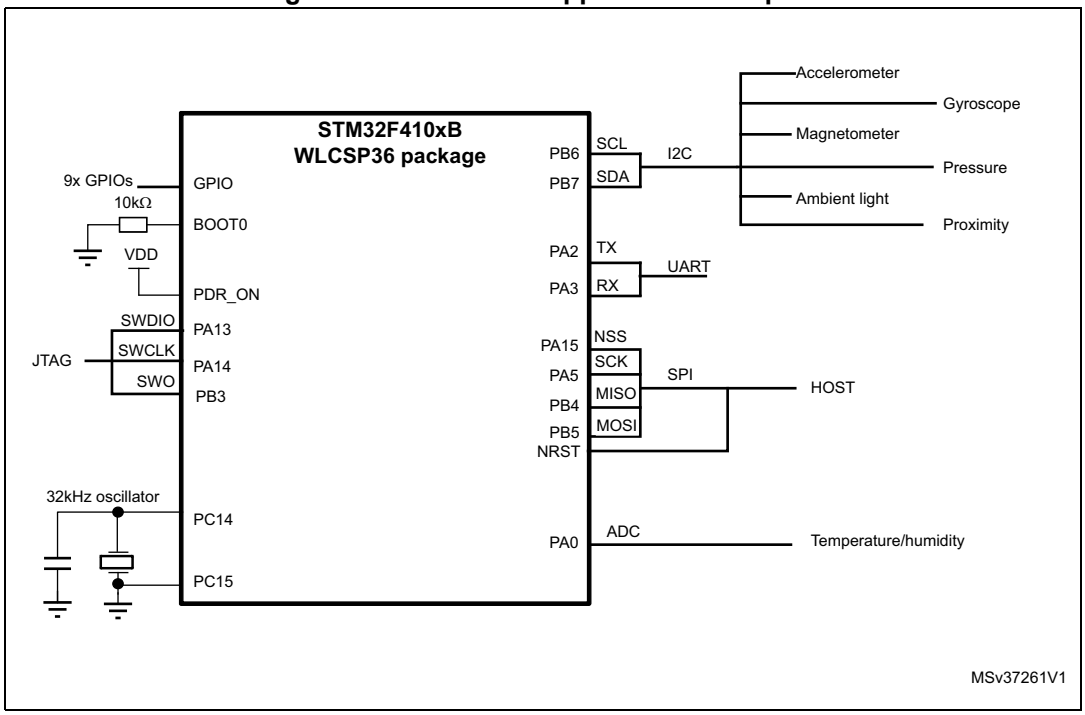


Figure 57. Sensor hub application example 2