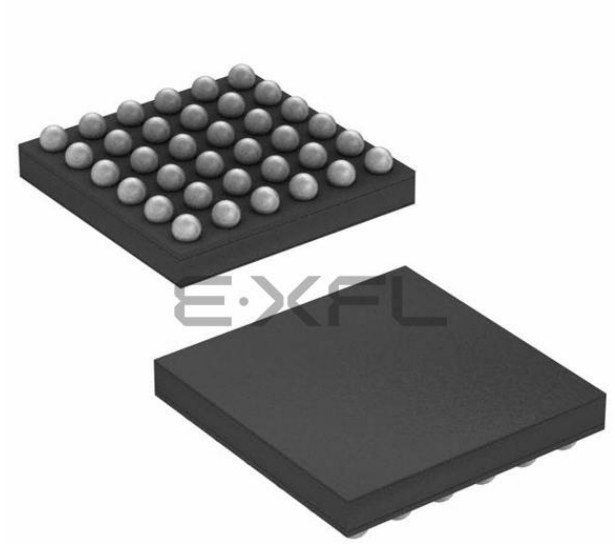

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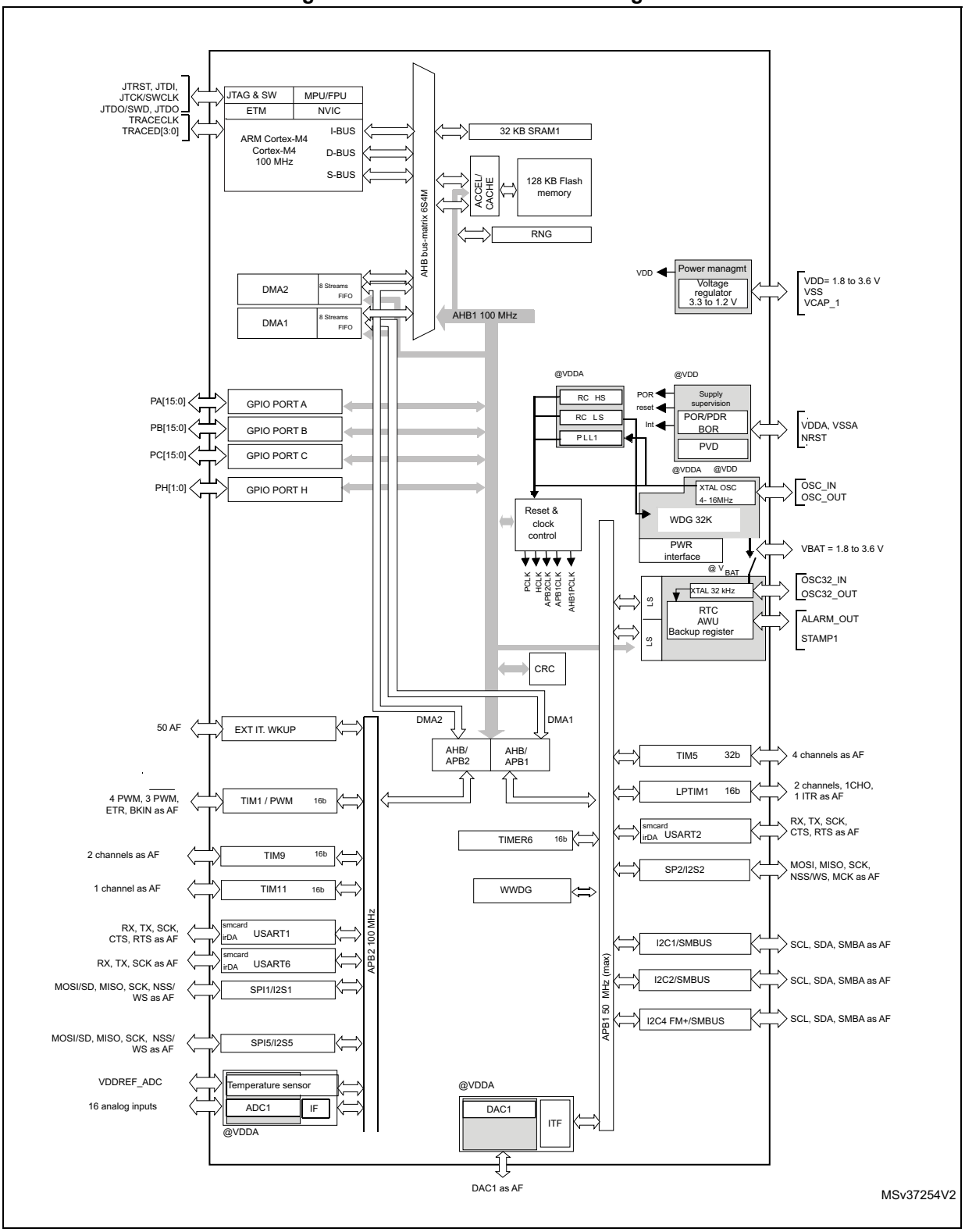
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410t8y6tr

Figure 2. STM32F410x8/B block diagram



1. The timers connected to APB2 are clocked from TIMxCLK up to 100 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 100 MHz.

3.15 Power supply supervisor

3.15.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

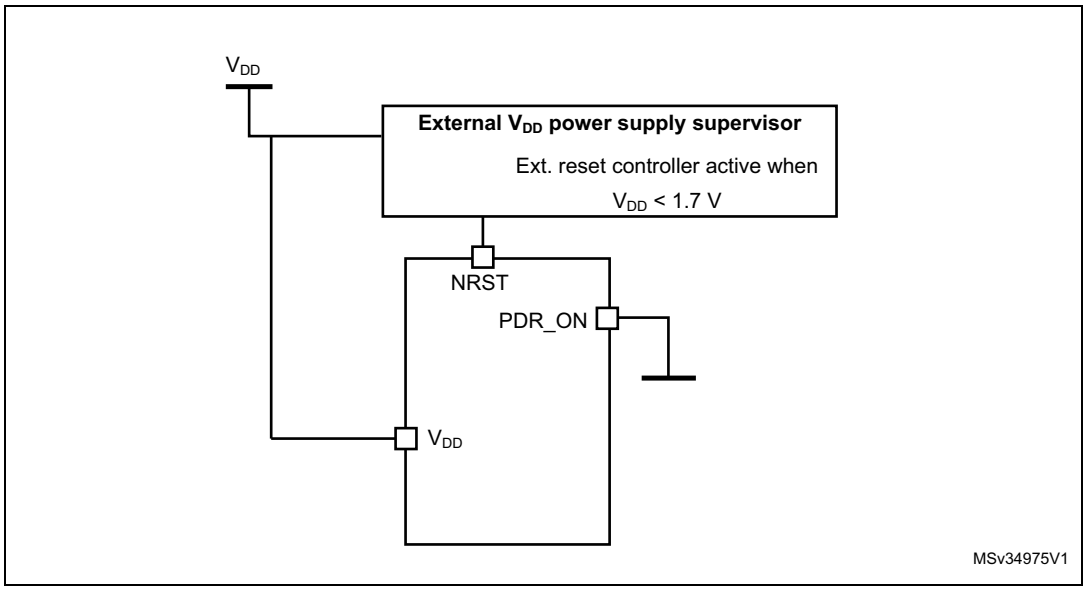
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available on WLCSP36 package only. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 4: Power supply supervisor interconnection with internal reset OFF*.

Figure 4. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available on WLCSP36 package only.

Table 9. STM32F410x8/B pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP36	LQFP48	UFQFPN48	LQFP64	UFBGA64						
E3	21	21	29	G7	PB10	I/O	FT	-	I2C2_SCL, SPI2_SCK/I2S2_CK, I2S1_MCK, I2C4_SCL, EVENTOUT	-
E2	22	22	30	H7	VCAP_1	S	-	-	-	-
F2	23	23	31	D6	VSS	S	-	-	-	-
F1	24	24	32	E5	VDD	S	-	-	-	-
E1	25	25	33	H8	PB12	I/O	FT	-	TIM1_BKIN, TIM5_CH1, I2C2_SMBA, SPI2_NSS/I2S2_WS, EVENTOUT	-
-	26	26	34	G8	PB13	I/O	FT	-	TIM1_CH1N, I2C4_SMBA, SPI2_SCK/I2S2_CK, EVENTOUT	-
-	27	27	35	F8	PB14	I/O	FT	-	TIM1_CH2N, I2C4_SDA, SPI2_MISO, EVENTOUT	-
-	28	28	36	F7	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, I2C4_SCL, SPI2_MOSI/I2S2_SD, EVENTOUT	-
-	-	-	37	F6	PC6	I/O	FT	-	TRACECLK, I2C4_SCL, I2S2_MCK, USART6_TX, EVENTOUT	-
-	-	-	38	E7	PC7	I/O	FT	-	I2C4_SDA, SPI2_SCK/I2S2_CK, I2S1_MCK, USART6_RX, EVENTOUT	-
-	-	-	39	E8	PC8	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	40	D8	PC9	I/O	FT	-	MCO_2, I2C4_SDA, I2S2_CKIN, EVENTOUT	-

Table 10. Alternate function mapping (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/LPTIM1	TIM5	TIM9/ TIM11	I2C1/I2C2 /I2C4	SPI1/I2S1/S PI2/I2S2	SPI1/I2S1/ SPI2/I2S2/ SPI5/I2S5	USART1/ USART2	USART6	I2C2/ I2C4	-	-	-	-	-	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC1	-	LPTIM1_OUT	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC2	-	LPTIM1_IN2	-	-	-	SPI2_MISO	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC3	-	LPTIM1_ETR	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC4	-	-	-	TIM9_ CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC5	-	-	-	TIM9_ CH2	I2C4_ SMBA	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC6	TRACE CLK	-	-	-	I2C4_ SCL	I2S2_MCK	-	-	USART6 _TX	-	-	-	-	-	-	EVENTOUT
	PC7	-	-	-	-	I2C4_ SDA	SPI2_SCK/ I2S2_CK	I2S1_MCK	-	USART6 _RX	-	-	-	-	-	-	EVENTOUT
	PC8	-	-	-	-	-	-	-	-	USART6 _CK	-	-	-	-	-	-	EVENTOUT
	PC9	MCO_2	-	-	-	I2C4_ SDA	I2S2_CKIN	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC10	TRACED0	-	TIM5_ CH2	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC11	TRACED1	-	TIM5_ CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC12	TRACED2	-	-	TIM11_ CH1	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENTOUT

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	27.1	28.9	28.9	29.5	30.5	mA
			84	S2	168	23.2	24.8	24.9	25.5	26.5	
			64	S3	128	17.0	18.3	18.4	18.8	19.8	
			50	S3	100	13.6	14.7	14.7	15.2	16.2	
			25	S3	100	7.5	8.2	8.3	8.7	9.7	
			20	S3	160	6.5	7.1	7.2	7.5	8.5	
		HSI, PLL OFF, all peripherals enabled(3)(4)	16	S3	off	4.7	5.3	5.5	5.9	6.9	
			1	S3	off	0.8	1.2	1.4	1.8	2.8	
		External clock, all peripherals disabled(3)	100	S1	200	21.5	23.0	23.2	23.8	24.8	
			84	S2	168	18.7	20.0	20.3	20.8	21.8	
			64	S3	128	14.0	15.1	15.2	15.7	16.7	
			50	S3	100	11.2	12.2	12.3	12.7	13.7	
			25	S3	100	6.3	7.0	7.1	7.4	8.4	
			20	S3	160	5.4	6.0	6.2	6.5	7.5	
		HSI, PLL OFF, all peripherals disabled(3)	16	S3	off	4.0	4.5	4.8	5.1	6.1	
			1	S3	off	0.8	1.1	1.4	1.7	2.7	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

Table 28. Typical and maximum current consumption in Sleep mode - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Sleep mode**	All peripherals enabled(3)(4), External clock, PLL ON, Flash memory in Deep power down mode	100	S1	200	8.0	8.2(5)	9.0	9.4(6)	10.2(5)	mA
			84	S2	168	6.5	6.7	7.4	7.7	8.5	
			64	S3	128	4.6	4.7	5.2	5.5	6.3	
			50	S3	100	3.7	3.9	4.3	4.6	5.4	
			25	S3	100	2.2	2.3	2.6	2.9	3.8	
			20	S3	160	2.1	2.2	2.5	2.8	3.6	
		All peripherals enabled(3)(4), HSI, PLL OFF, Flash memory in Deep power down mode	16	S3	off	1.1	1.2	1.5	1.9	2.7	
			1	S3	off	0.3	0.4	0.7	1.1	1.9	
		All peripherals enabled(3)(4), External clock, PLL ON, Flash memory ON	100	S1	200	8.4	8.7	9.5	9.9	10.7	
			84	S2	168	6.9	7.1	7.7	8.1	8.9	
			64	S3	128	4.9	5.1	5.5	5.9	6.7	
			50	S3	100	4.0	4.2	4.6	4.9	5.7	
			25	S3	100	2.5	2.6	2.9	3.2	4.0	
			20	S3	160	2.4	2.5	2.7	3.1	3.9	
		All peripherals enabled(3), HSI, PLL OFF, Flash memory ON	16	S3	off	1.4	1.4	1.8	2.2	3.0	
			1	S3	off	0.6	0.6	1.0	1.3	2.0	

Table 35. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
IDDIO	I/O switching current	V_{DD} = 3.3 V C = C_{INT}	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		V_{DD} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		V_{DD} = 3.3 V C_{EXT} =10 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		V_{DD} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		V_{DD} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT} + C_S	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature is 25 °C and V_{DD}=3.3 V.

Table 36. Peripheral current consumption

Peripheral		I_{DD} (Typ)			Unit
		Voltage scale1	Voltage scale2	Voltage scale3	
AHB1 (up to 100 MHz)	GPIOA	1.68	1.62	1.42	µA/MHz
	GPIOB	1.67	1.60	1.41	
	GPIOC	1.63	1.56	1.39	
	GPIOH	0.61	0.61	0.52	
	CRC	0.31	0.32	0.25	
	DMA1(1)	1.67N + 3.12	1.60N + 2.96	1.43N + 2.64	
	DMA2(1)	1.59N + 2.83	1.52N + 2.65	1.36N + 2.41	
	RNG	0.90	0.88	0.75	
APB1 (up to 50 MHz)	APB1 to AHB	0,78	0,74	0,63	µA/MHz
	TIM5	13,38	12,76	11,41	
	TIM6	2,14	1,98	1,75	
	LPTIM	8,22	7,88	7,06	
	WWDG	0,64	0,64	0,56	
	SPI2/I2S2	2,42	2,33	2,06	
	USART2	3,38	3,29	2,91	
	I2C1	3,46	3,33	2,97	
	I2C2	3,50	3,31	2,97	
	I2C4	4,82	4,64	4,09	
	PWR	0,66	0,64	0,62	
	DAC	0,84	0,81	0,78	

Table 38. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency(1)	-	1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 55*. However, the recommended clock input waveform is shown in *Figure 20*.

The characteristics given in *Table 39* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 15*.

Table 39. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design.

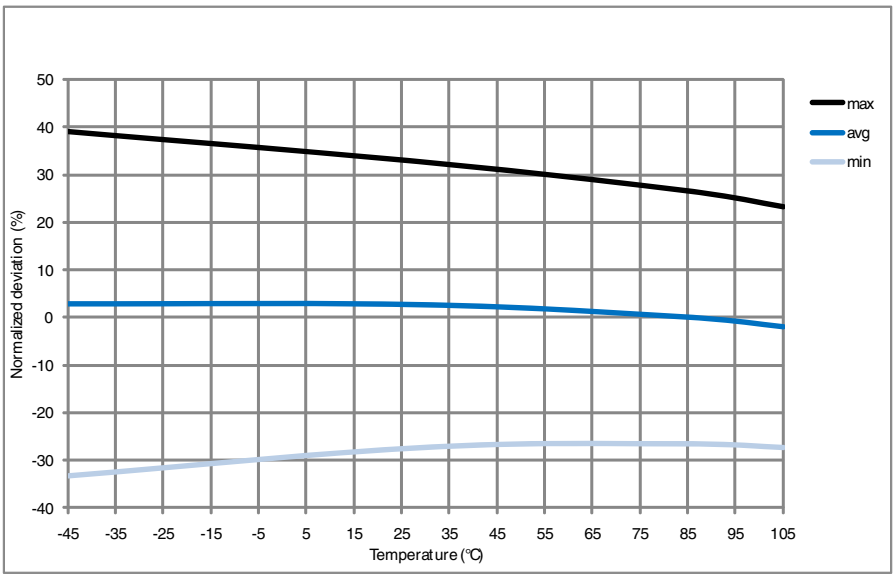
Low-speed internal (LSI) RC oscillator

Table 43. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 125 °C unless otherwise specified.
2. Guaranteed by characterization.
3. Guaranteed by design.

Figure 24. ACC_{LSI} versus temperature



MS19013V1

6.3.10 PLL characteristics

The parameters given in *Table 44* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 15*.

Table 44. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)	-	0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	100	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock	-	-	48	75	MHz
f_{VCO_OUT}	PLL VCO output	-	100	-	432	MHz

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 52. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions		Class	Maximum value(2)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to ANSI/JEDEC JS-001		2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to ANSI/ESD STM5.3.1	UFQFPN48	4	500	
			WLCSP36	3	250	
			LQFP48	4	500	
			LQPF64	4	500	
			UFBGA64	TBD	TBD	

1. TBD stands for “to be defined”.
2. Guaranteed by characterization.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 53. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +125 °C conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

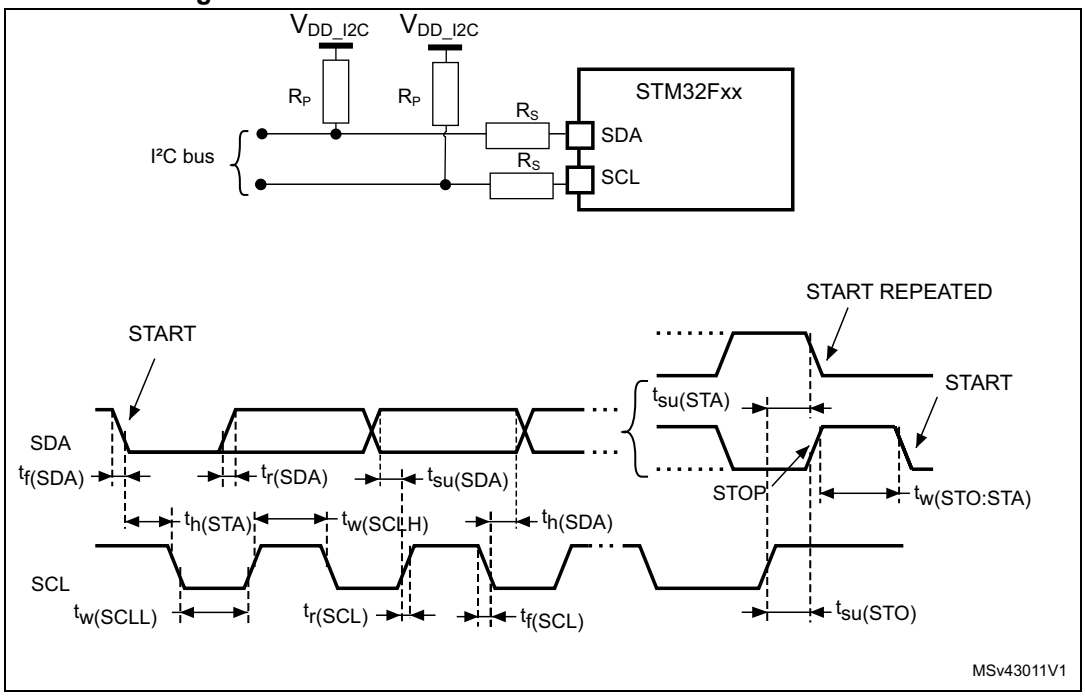
Table 57. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	12.5	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 40 pF, V_{DD} ≥ 2.70 V	-	-	50(4)	MHz
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	100(4)	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD}≥ 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	6	
11	$F_{max(IO)out}$	Maximum frequency(3)	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	100(4)	MHz
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	50(4)	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	6	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by characterization.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 28*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max)

Figure 30. I²C bus AC waveforms and measurement circuit



1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I2C bus power supply.

Table 61. SCL frequency (f_{PCLK1}= 50 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

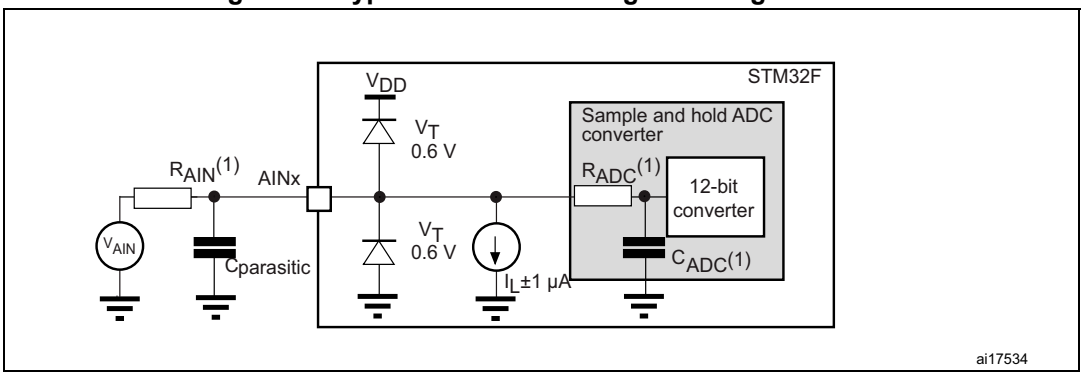
1. R_P = External pull-up resistance, f_{SCL} = I²C speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed is ±2%. These variations depend on the accuracy of the external components used to design the application.

Table 62. SCL frequency (f_{PCLK1}= 42 MHz.,V_{DD} = V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I^2C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

Figure 38. Typical connection diagram using the ADC



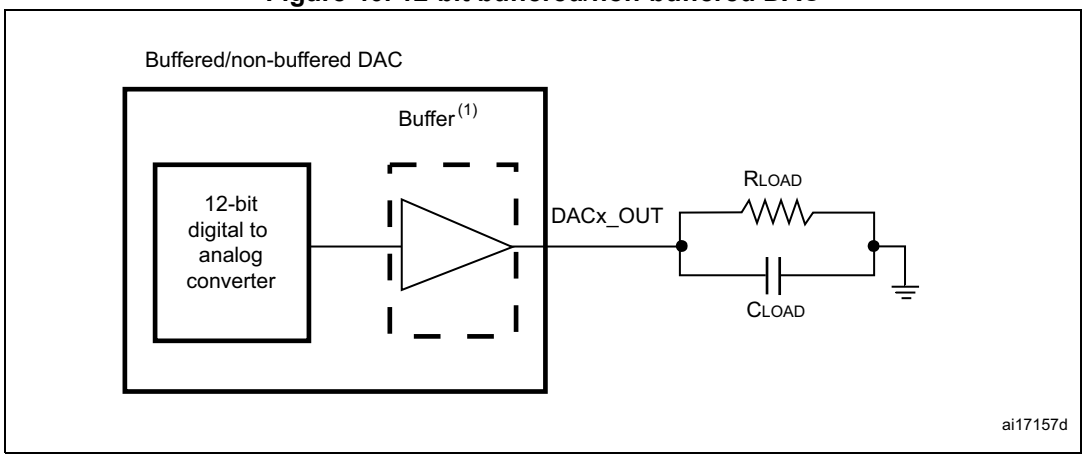
1. Refer to *Table 66* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

Table 77. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
t_{WAKEUP}(4)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ (2)	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	- –67	- 40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to *Section 3.15.2: Internal reset OFF*).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed based on test during characterization.

Figure 40. 12-bit buffered/non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.25 RTC characteristics

Table 78. RTC characteristics

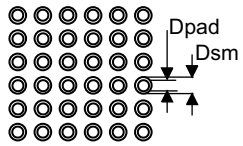
Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Table 79. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.170	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.518	2.553	2.588	0.1012	0.1026	0.1039
E	2.544	2.579	2.614	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-
F	-	0.2765	-	-	0.0119	-
G	-	0.2895	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

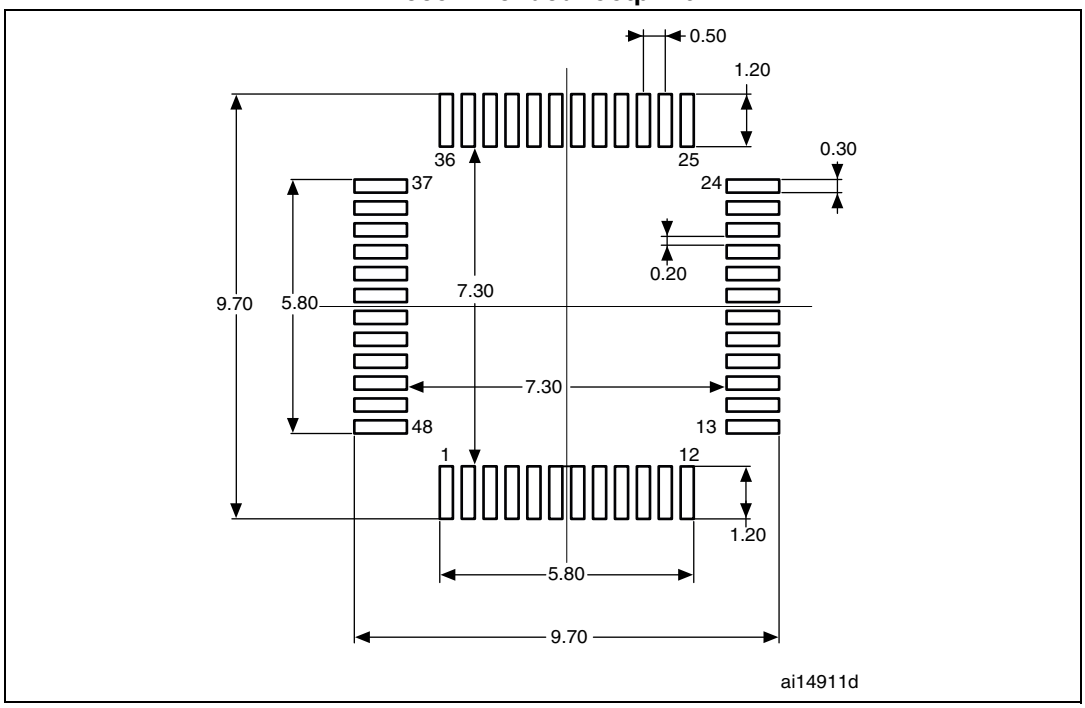
1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 42. WLCSP36 - 36-pin, 2.553 x 2.579 mm, 0.4 mm pitch wafer level chip scale package recommended footprint



A05F_FP_V1

Figure 48. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

7.6 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 15: General operating conditions on page 53*.

The maximum chip-junction temperature, T_J max., in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (PD max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- PD max is the sum of P_{INT} max and $P_{I/O}$ max (PD max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 86. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48	55	°C/W
	Thermal resistance junction-ambient LQFP64	46	
	Thermal resistance junction-ambient UFQFPN48	33	
	Thermal resistance junction-ambient WLCSP36	61	
	Thermal resistance junction-ambient UFBGA64	79	

7.6.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.