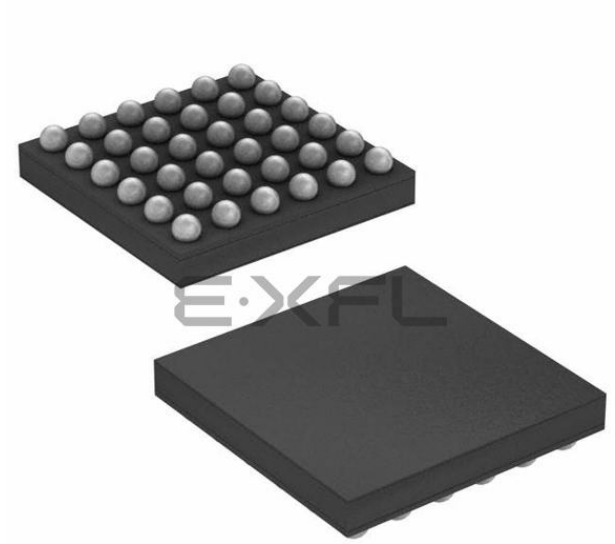

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	23
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 4x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	36-UFBGA, WLCSP
Supplier Device Package	36-WLCSP (2.55x2.58)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f410tby3tr

3 Functional overview

3.1 ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F410x8/B devices are compatible with all ARM tools and software.

Figure 2 shows the general block diagram of the STM32F410x8/B.

Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 125 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 100 MHz.

3.3 Batch Acquisition mode (BAM)

The Batch acquisition mode allows enhanced power efficiency during data batching. It enables data acquisition through any communication peripherals directly to memory using the DMA in reduced power consumption as well as data processing while the rest of the system is in low-power mode (including the flash and ART). For example in an audio system, a smart combination of PDM audio sample acquisition and processing from the I2S directly to RAM (flash and ART™ stopped) with the DMA using BAM followed by some very short processing from flash allows to drastically reduce the power consumption of the application. A dedicated application note (AN4515) describes how to implement the STM32F410x8/B BAM to allow the best power efficiency.

3.15 Power supply supervisor

3.15.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

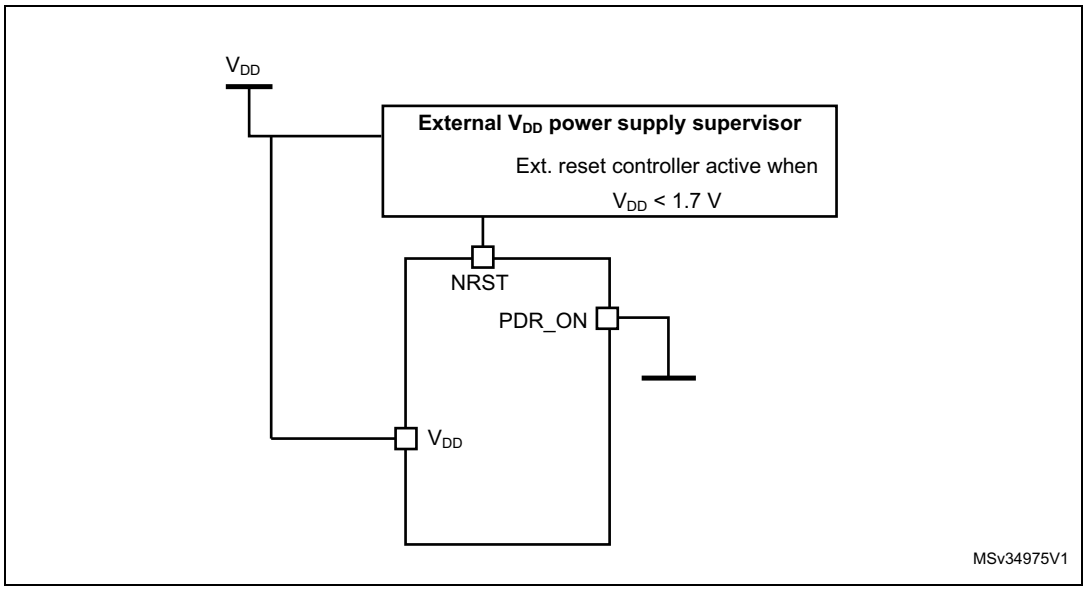
The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.15.2 Internal reset OFF

This feature is available on WLCSP36 package only. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should set the device in reset mode when V_{DD} is below 1.7 V. NRST should be connected to this external power supply supervisor. Refer to *Figure 4: Power supply supervisor interconnection with internal reset OFF*.

Figure 4. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is available on WLCSP36 package only.

3.20.4 Low-power timer (LPTIM1)

The devices embed one low-power timer. This timer features an independent clock and runs in Stop mode if it is clocked by LSE, LSI or by an external clock. It is able to wake up the system from Stop mode.

The low-power timer main features are the following:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous/ one shot mode
- Selectable software/hardware input trigger
- Selectable clock source
  - Internal clock sources: LSE, LSI, HSI or APB1 clock
  - External clock source over LPTIM input (working even when no internal clock source is running and used by pulse-counter applications).
- Programmable digital glitch filter
- Encoder mode
- Active in Stop mode.

3.20.5 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.20.6 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.20.7 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

- Triangular-wave generation
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channel is triggered through TIM6 update output that is also connected to different DMA channels.

3.30 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.31 Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F410x8/B through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

Table 9. STM32F410x8/B pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP36	LQFP48	UFQFPN48	LQFP64	UFBGA64						
E4	12	12	16	F3	PA2	I/O	FT	-	TIM5_CH3, TIM9_CH1, I2S2_CKIN, USART2_TX, EVENTOUT	ADC1_2
F5	13	13	17	G3	PA3	I/O	FT	-	TIM5_CH4, TIM9_CH2, I2S2_MCK, USART2_RX, EVENTOUT	ADC1_3
-	-	-	18	D5	VSS	S	-	-	-	-
-	-	-	19	E4	VDD	S	-	-	-	-
-	14	14	20	H3	PA4	I/O	FT	-	SPI1_NSS/I2S1_WS, USART2_CK, EVENTOUT	ADC1_4
F4	15	15	21	F4	PA5	I/O	TC	-	SPI1_SCK/I2S1_CK, EVENTOUT	ADC1_5, DAC_OUT1
-	16	16	22	G4	PA6	I/O	FT	-	TIM1_BKIN, SPI1_MISO, I2S2_MCK, EVENTOUT	ADC1_6
-	17	17	23	H4	PA7	I/O	FT	-	TIM1_CH1N, SPI1_MOSI/I2S1_SD, EVENTOUT	ADC1_7
-	-	-	24	G5	PC4	I/O	FT	-	TIM9_CH1, EVENTOUT	ADC1_14
-	-	-	25	H5	PC5	I/O	FT	-	TIM9_CH2, I2C4_SMBA, EVENTOUT	ADC1_15
-	18	18	26	F5	PB0	I/O	FT	-	TIM1_CH2N, SPI5_SCK/I2S5_CK, EVENTOUT	ADC1_8
-	19	19	27	G6	PB1	I/O	TC	-	TIM1_CH3N, SPI5_NSS/I2S5_WS, EVENTOUT	ADC1_9
F3	20	20	28	H6	PB2	I/O	FT	-	LPTIM1_OUT, EVENTOUT	BOOT1

Table 9. STM32F410x8/B pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
WLCSP36	LQFP48	UFQFPN48	LQFP64	UFBGA64						
E3	21	21	29	G7	PB10	I/O	FT	-	I2C2_SCL, SPI2_SCK/I2S2_CK, I2S1_MCK, I2C4_SCL, EVENTOUT	-
E2	22	22	30	H7	VCAP_1	S	-	-	-	-
F2	23	23	31	D6	VSS	S	-	-	-	-
F1	24	24	32	E5	VDD	S	-	-	-	-
E1	25	25	33	H8	PB12	I/O	FT	-	TIM1_BKIN, TIM5_CH1, I2C2_SMBA, SPI2_NSS/I2S2_WS, EVENTOUT	-
-	26	26	34	G8	PB13	I/O	FT	-	TIM1_CH1N, I2C4_SMBA, SPI2_SCK/I2S2_CK, EVENTOUT	-
-	27	27	35	F8	PB14	I/O	FT	-	TIM1_CH2N, I2C4_SDA, SPI2_MISO, EVENTOUT	-
-	28	28	36	F7	PB15	I/O	FT	-	RTC_50Hz, TIM1_CH3N, I2C4_SCL, SPI2_MOSI/I2S2_SD, EVENTOUT	-
-	-	-	37	F6	PC6	I/O	FT	-	TRACECLK, I2C4_SCL, I2S2_MCK, USART6_TX, EVENTOUT	-
-	-	-	38	E7	PC7	I/O	FT	-	I2C4_SDA, SPI2_SCK/I2S2_CK, I2S1_MCK, USART6_RX, EVENTOUT	-
-	-	-	39	E8	PC8	I/O	FT	-	USART6_CK, EVENTOUT	-
-	-	-	40	D8	PC9	I/O	FT	-	MCO_2, I2C4_SDA, I2S2_CKIN, EVENTOUT	-

5 Memory mapping

The memory map is shown in *Figure 10*.

Figure 10. Memory map

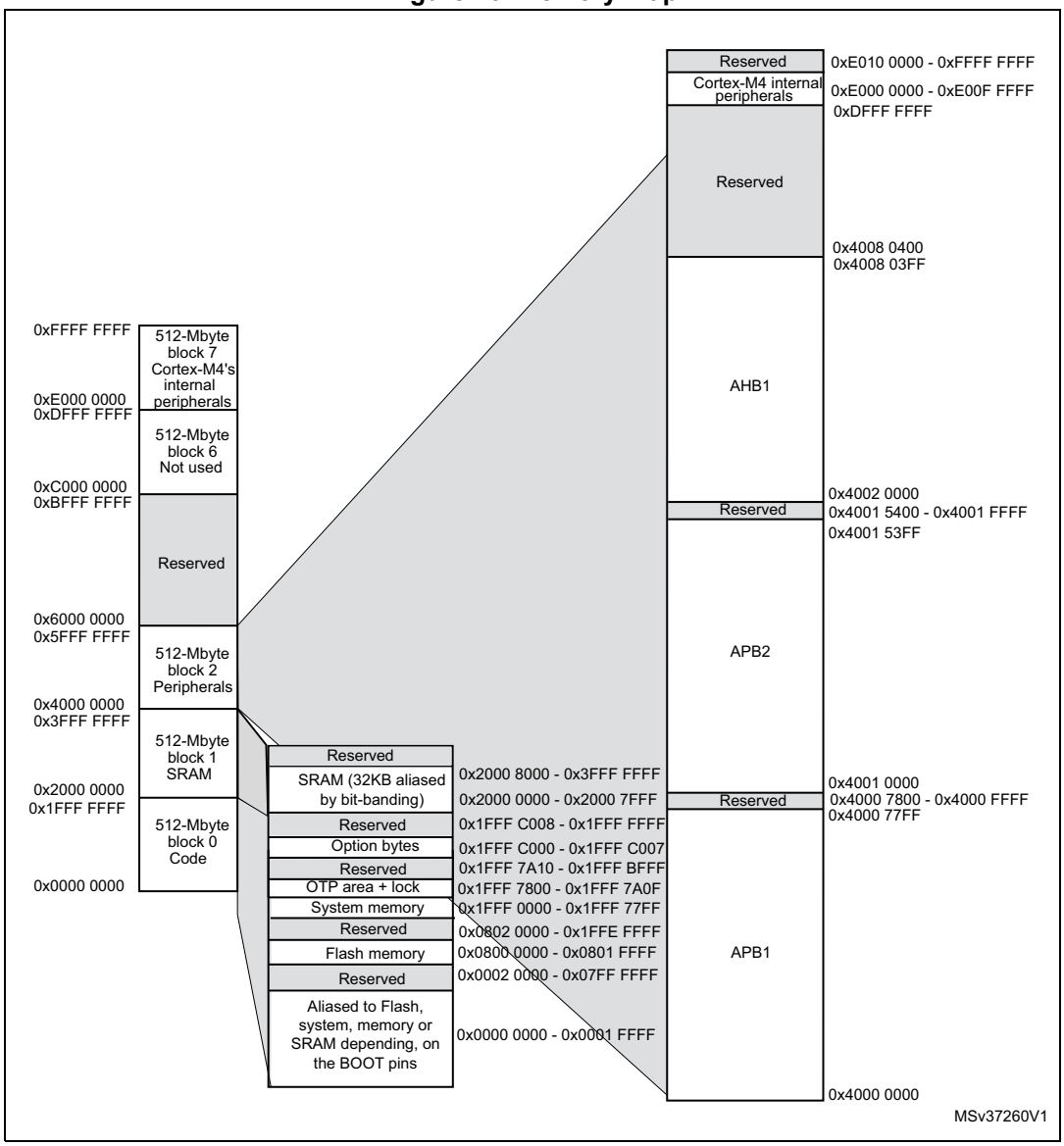


Table 22. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A= 25 °C	T_A= 85 °C	T_A= 105 °C	T_A= 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	17.7	19.1(5)	19.3	19.7(6)	20.5(5)	mA
			84	S2	168	14.4	15.3(5)	15.7	16.0(6)	16.8(5)	
			64	S3	128	10.1	10.6(5)	11.0	11.3(6)	12.0(5)	
			50	S3	100	8.0	8.4	8.8	9.1	9.8	
			25	S3	100	4.4	4.7	4.9	5.2	5.9	
			20	S3	160	3.8	4.1	4.3	4.6	5.3	
		HSI, PLL off, all peripherals enabled(3)(4)	16	S3	off	2.5	2.6	2.9	3.2	4.0	
			1	S3	off	0.4	0.5	0.8	1.2	2.0	
		External clock, all peripherals disabled(3)	100	S1	200	12.1	13.1(5)	13.1	13.5(6)	14.3(5)	
			84	S2	168	9.8	10.6(5)	10.7	11.0(6)	11.8(5)	
			64	S3	128	7.0	7.4(5)	7.6	7.9(6)	8.6(5)	
			50	S3	100	5.6	5.9	6.1	6.4	7.2	
			25	S3	100	3.1	3.3	3.5	3.9	4.8	
			20	S3	160	2.8	3.0	3.2	3.5	4.4	
		HSI, PLL off, all peripherals disabled(3)	16	S3	off	1.7	1.8	2.1	2.4	3.3	
			1	S3	off	0.4	0.4	0.7	1.1	1.8	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)
5. Guaranteed by tests in production.
6. Guaranteed by test in production for temperature range 7 salestypes only.

Table 23. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.7 V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Voltage scale	PLL VCO (MHz) (1)	Typ	Max(2)				Unit
						T_A= 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(3)(4)	100	S1	200	15.7	16.5	16.5	16.9	17.8	mA
			84	S2	168	12.7	13.3	13.4	13.8	14.6	
			64	S3	128	8.8	9.3	9.4	9.7	10.6	
			50	S3	100	7.0	7.4	7.5	7.8	8.6	
			25	S3	100	3.9	4.1	4.3	4.7	5.6	
			20	S3	160	3.4	3.6	3.8	4.2	5.1	
		HSI, PLL OFF, all peripherals enabled(3)(4)	16	S3	off	2.4	2.5	2.8	3.2	4.1	
			1	S3	off	0.6	0.7	1.0	1.4	2.3	
		External clock, all peripherals disabled(3)	100	S1	200	10.1	10.7	10.8	11.2	12.0	
			84	S2	168	8.2	8.6	8.7	9.1	10.0	
			64	S3	128	5.7	6.1	6.2	6.6	7.4	
			50	S3	100	4.6	4.9	5.0	5.4	6.3	
			25	S3	100	2.6	2.8	3.0	3.4	4.3	
			20	S3	160	2.4	2.5	2.8	3.1	4.0	
		HSI, PLL OFF, all peripherals disabled(3)	16	S3	off	1.7	1.8	2.1	2.4	3.3	
			1	S3	off	0.6	0.6	1.0	1.4	2.2	

1. Refer to *Table 44* and RM0401 for the possible PLL VCO setting
2. Guaranteed by characterization, unless otherwise specified.
3. When the ADC is ON (ADON bit set in ADC_CR2), an additional power consumption of 1.6 mA must be added.
4. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register)

Table 33. Typical and maximum current consumption in Standby mode - V_{DD}= 3.6 V

Symbol	Parameter	Conditions	Typ	Max				Unit
			T_A = 25 °C	T_A = 25 °C(1)	T_A = 85 °C	T_A = 105 °C(1)	T_A = 125 °C(1)	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE) and RTC ON	3.4	4.3	8.9	22.8	65.0	µA
		RTC and LSE OFF	2.5	3.3(2)	7.8	21.6(3)	64.0(2)	

1. Guaranteed by characterization, unless otherwise specified.
2. Guaranteed by tests in production.
3. Guaranteed by test in production on temperature range 7 salestypes only.

Table 34. Typical and maximum current consumptions in V_{BAT} mode (LSE and RTC ON, LSE low- drive mode)

Symbol	Parameter	Conditions(1)	Typ			Max(2)			Unit
			T_A = 25 °C			T_A = 85 °C	T_A = 105 °C	T_A = 125 °C	
			V_{BAT}= 1.7 V	V_{BAT}= 2.4 V	V_{BAT} = 3.3 V	V_{BAT} = 3.6 V			
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.7	0.8	1.1	2.8	4.2	5.6	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.4	1.6	1.9	4.2	7.0	8.6	
		RTC and LSE OFF	0.1	0.1	0.1	2.0	4.0	5.8	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.
2. Guaranteed by characterization.

Figure 16. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator in "low power" mode selection

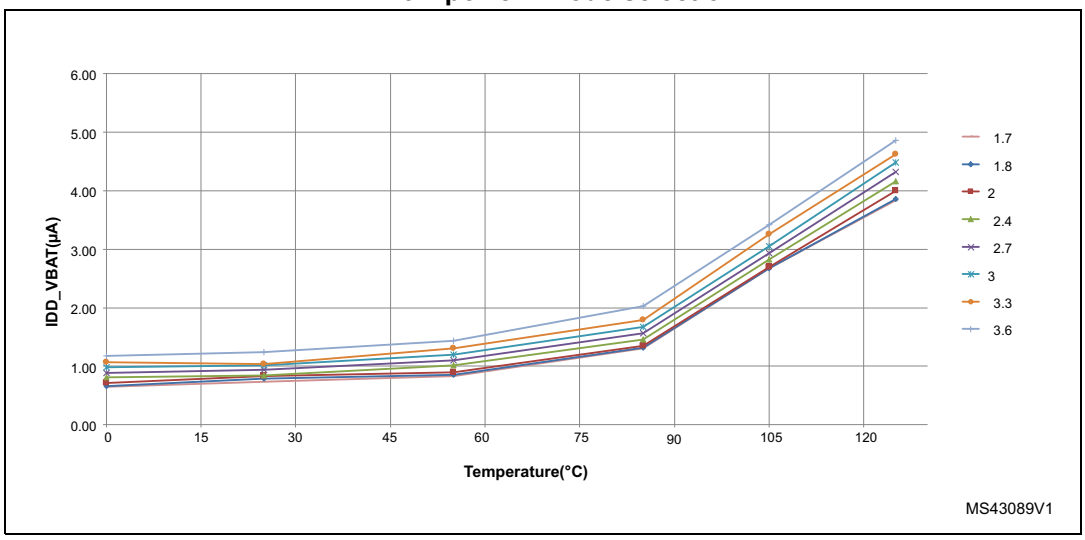
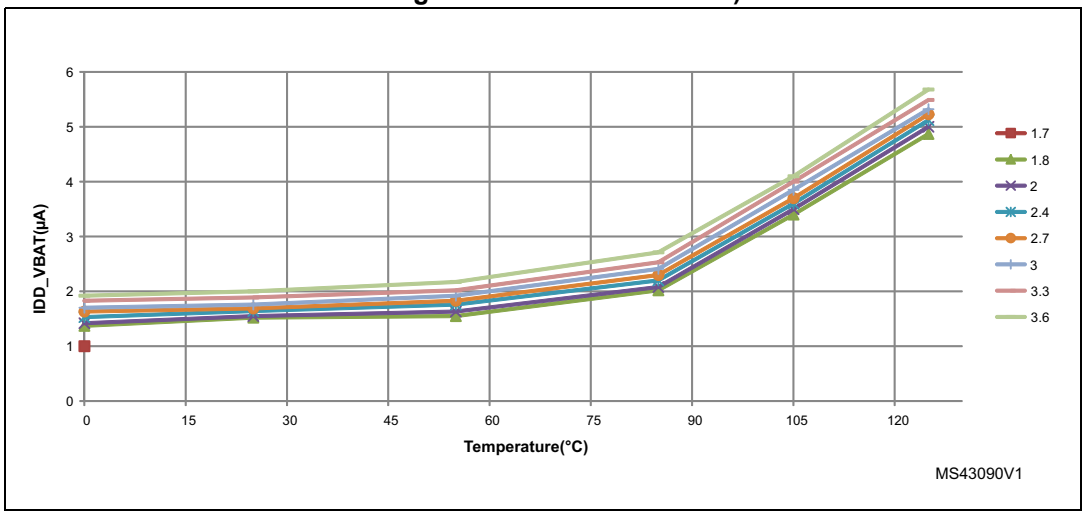


Figure 17. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator in "high-drive" mode selection)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 55: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 36: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Figure 25 and *Figure 26* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 25. PLL output clock waveforms in center spread mode

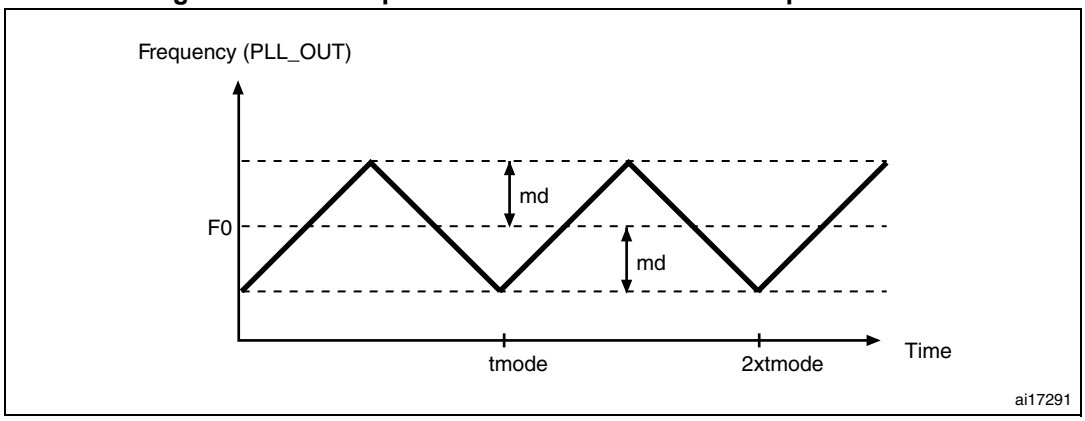
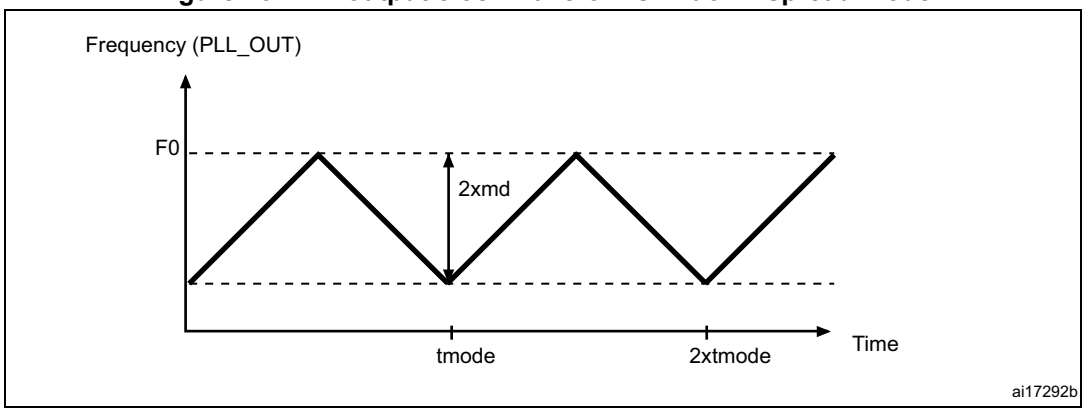


Figure 26. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 46. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 49. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = - 40 to +85 °C (6 suffix versions) T_A = - 40 to +105 °C (7 suffix versions) T_A = - 40 to +125 °C (3 suffix versions)	10	Kcycle
tRET	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		1 kcycle(2) at T_A = 125 °C	3	
		10 kcycle(2) at T_A = 55 °C	20	

1. Guaranteed by characterization.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 51*. They are based on the EMS levels and classes defined in application note AN1709.

Table 50. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 100 MHz, conforms to IEC 61000-4-4	4A

Table 55. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	FT, TC and NRST I/O input high level voltage(5)		1.7 V≤V_{DD}≤3.6 V	0.7V_{DD}(1)	-	-	V
	BOOT0 I/O input high level voltage		1.75 V≤V_{DD} ≤3.6 V, -40 °C≤T_A ≤ 125 °C	0.17V_{DD}+ 0.7(2)	-	-	
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤ 125 °C				
V_{HYS}	FT, TC and NRST I/O input hysteresis		1.7 V≤V_{DD}≤3.6 V	-	10% V_{DD}(3)	-	V
	BOOT0 I/O input hysteresis		1.75 V≤V_{DD} ≤3.6 V, - 40 °C≤T_A ≤ 125 °C	-	100	-	mV
			1.7 V≤V_{DD} ≤3.6 V, 0 °C≤T_A ≤ 125 °C				
I_{lkg}	I/O input leakage current (4)		V_{SS} ≤V_{IN} ≤V_{DD}	-	-	±1	µA
	I/O FT/TC input leakage current (5)		V_{IN} = 5 V	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(6)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{SS}	30	40	50	kΩ
		PA10 (OTG_FS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor(7)	All pins except for PA10 (OTG_FS_ID)	V_{IN} = V_{DD}	30	40	50	
		PA10 (OTG_FS_ID)	-	7	10	14	
C_{IO}(8)	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by tests in production.
2. Guaranteed by design.
3. With a minimum of 200 mV.
4. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins, Refer to *Table 54: I/O current injection susceptibility*
5. To sustain a voltage higher than VDD +0.3 V, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins.Refer to *Table 54: I/O current injection susceptibility*
6. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
7. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).
8. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in *Figure 27*.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 64* for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 15*, with the following configuration:

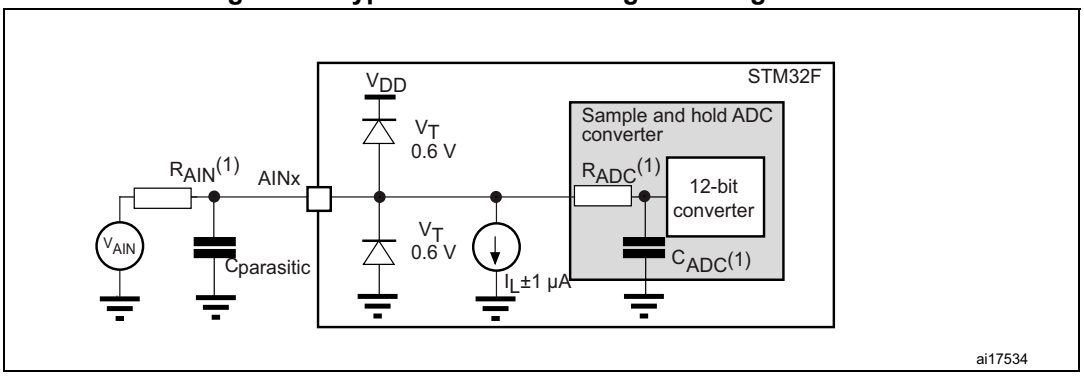
- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 64. SPI dynamic characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master full duplex/receiver mode, 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	42	MHz
		Master full duplex/receiver mode, 3.0 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master transmitter mode 1.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Master mode 1.7 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
		Slave transmitter/full duplex mode 2.7 V < V_{DD} < 3.6 V SPI1/4/5	-	-	38(2)	
		Slave receiver mode, 1.8 V < V_{DD} < 3.6 V SPI1/4/5	-	-	50	
		Slave mode, 1.8 V < V_{DD} < 3.6 V SPI1/2/3/4/5	-	-	25	
Duty(SCK)	Duty cycle of SPI clock frequency	Slave mode	30	50	70	%
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, SPI presc = 2	T_{PCLK} - 1.5	T_{PCLK}	T_{PCLK} +1.5	ns
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$3T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2T_{PCLK}$	-	-	ns
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	2.5	-	-	ns
$t_{h(MI)}$	Data input hold time	Master mode	7.5	-	-	ns
$t_{h(SI)}$		Slave mode	3.5	-	-	ns

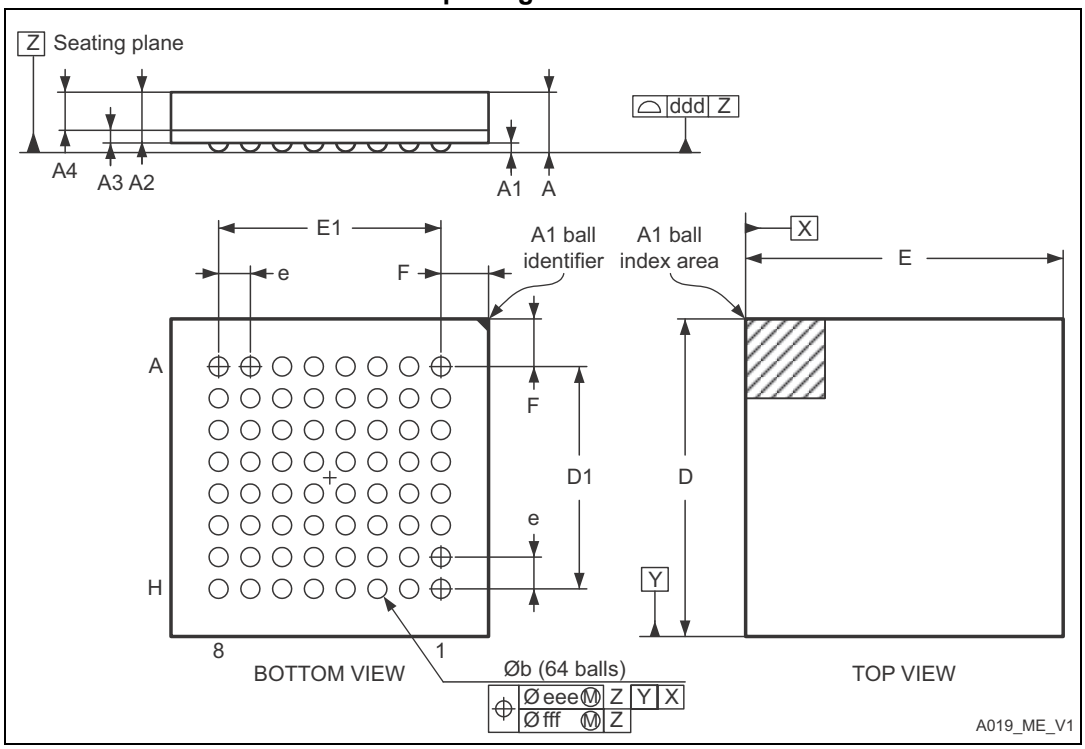
Figure 38. Typical connection diagram using the ADC



1. Refer to *Table 66* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

7.5 UFBGA64 package information

Figure 53. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 84. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	0.080	0.130	0.180	0.0031	0.0051	0.0071
A4	0.270	0.320	0.370	0.0106	0.0126	0.0146
b	0.170	0.280	0.330	0.0067	0.0110	0.0130
D	4.850	5.000	5.150	0.1909	0.1969	0.2028
D1	3.450	3.500	3.550	0.1358	0.1378	0.1398
E	4.850	5.000	5.150	0.1909	0.1969	0.2028
E1	3.450	3.500	3.550	0.1358	0.1378	0.1398
e	-	0.500	-	-	0.0197	-

8 Part numbering

Table 87. Ordering information scheme

Example: STM32 F 410 C B Y 6 TR

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Device subfamily

410 = 410 line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

Flash memory size

8 = 64 Kbytes of Flash memory

B = 128 Kbytes of Flash memory

Package

I = UFBGA

T = LQFP

U = UFQFPN

Y = WLCSP

Temperature range

6 = Industrial temperature range, - 40 to 85 °C

3 = Industrial temperature range, - 40 to 125 °C

Packing

TR = tape and reel

No character = tray or tube