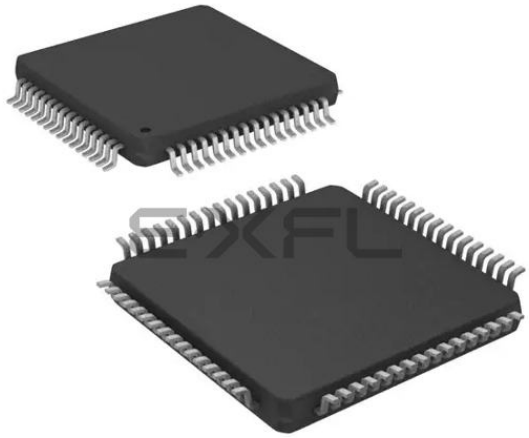
Microchip Technology - PIC18F65J94T-I/PT Datasheet



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Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	64MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, HLVD, LCD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	32KB (16K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f65j94t-i-pt

TABLE 4: 100-PIN ALLOCATION TABLE (PIC18F9XJ94) (CONTINUED)

I/O	100-Pin TQFP	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	EMB	PPS-Lite(1)	Pull-up	Basic
RF2	23	AN7	C2INB	—	CTMUI	—	SEG20	—	—	—	—	—	RP36	Y	—
RF3	22	—	—	—	—	D-	—	—	—	—	—	—	—	Y	—
RF4	20	—	—	—	—	D+	—	—	—	—	—	—	—	Y	—
RF5	19	AN10	C1INB/ CVREF	—	—	—	SEG23	—	—	—	—	—	RP35	Y	—
RF6	18	AN11	C1INA	—	—	—	SEG24	—	—	—	—	—	RP40	Y	—
RF7	17	AN5	—	—	—	—	SEG25	—	—	—	—	—	RP38	Y	—
RG0	6	AN8	—	—	—	—	COM4/ SEG28	—	—	—	—	—	RP46	Y	—
RG1	7	AN19	—	—	—	—	COM5/ SEG29	—	—	—	—	—	RP39	Y	—
RG2	8	AN18	C3INA	—	—	—	COM6/ SEG30	—	—	—	—	—	RP42	Y	—
RG3	9	AN17	C3INB	—	—	—	COM7/ SEG31	—	—	—	—	—	RP43	Y	—
RG4	12	AN16	C3INC	—	—	—	SEG26	—	—	—	—	—	RP44	Y	—
RG5/ MCLR	11	—	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{\text{MCLR}}$
RG6	89	—	—	—	—	—	—	—	—	—	—	—	—	Y	—
RG7	96	—	—	—	—	—	—	—	—	—	—	—	—	Y	—
RH0	99	AN23	—	—	—	—	SEG47	—	—	—	—	A16	—	Y	—
RH1	100	AN22	—	—	—	—	SEG46	—	—	—	—	A17	—	Y	—
RH2	1	AN21	—	—	—	—	SEG45	—	—	—	—	A18	—	Y	—
RH3	2	AN20	—	—	—	—	SEG44	—	—	—	—	A19	—	Y	—
RH4	27	AN12	C2INC	—	—	—	SEG40	—	—	—	—	—	—	Y	—
RH5	26	AN13	C2IND	—	—	—	SEG41	—	—	—	—	—	—	Y	—
RH6	25	AN14	C1INC	—	—	—	SEG42	—	—	—	—	—	—	Y	—
RH7	24	AN15	—	—	—	—	SEG43	—	—	—	—	—	—	Y	—
RJ0	77	—	—	—	—	—	SEG32	—	—	—	—	ALE	—	Y	—
RJ1	76	—	—	—	—	—	SEG33	—	—	—	—	$\overline{\text{OE}}$	—	Y	—
RJ2	75	—	—	—	—	—	SEG34	—	—	—	—	$\overline{\text{WRL}}$	—	Y	—
RJ3	74	—	—	—	—	—	SEG35	—	—	—	—	$\overline{\text{WRH}}$	—	Y	—
RJ4	49	—	—	—	—	—	SEG39	—	—	—	—	BA0	—	Y	—
RJ5	50	—	—	—	—	—	SEG38	—	—	—	—	$\overline{\text{CE}}$	—	Y	—
RJ6	51	—	—	—	—	—	SEG37	—	—	—	—	$\overline{\text{LB}}$	—	Y	—
RJ7	52	—	—	—	—	—	SEG36	—	—	—	—	$\overline{\text{UB}}$	—	Y	—
RK0	46	—	—	—	—	—	SEG56	—	—	—	—	—	—	Y	—
RK1	55	—	—	—	—	—	SEG57	—	—	—	—	—	—	Y	—
RK2	60	—	—	—	—	—	SEG58	—	—	—	—	—	—	Y	—
RK3	63	—	—	—	—	—	SEG59	—	—	—	—	—	—	Y	—
RK4	66	—	—	—	—	—	SEG60	—	—	—	—	—	—	Y	—
RK5	71	—	—	—	—	—	SEG61	—	—	—	—	—	—	Y	—
RK6	80	—	—	—	—	—	SEG62	—	—	—	—	—	—	Y	—
RK7	85	—	—	—	—	—	SEG63	—	—	—	—	—	—	Y	—
RL0	91	—	—	—	—	—	SEG48	—	—	—	—	—	—	Y	—
RL1	10	—	—	—	—	—	SEG49	—	—	—	—	—	—	Y	—
RL2	13	—	—	—	—	—	SEG50	—	—	—	—	—	—	Y	—
RL3	16	—	—	—	—	—	SEG51	—	—	—	—	—	—	Y	—
RL4	21	—	—	—	—	—	SEG52	—	—	—	—	—	—	Y	—
RL5	30	—	—	—	—	—	SEG53	—	—	—	—	—	—	Y	—

4.0 POWER-MANAGED MODES

All PIC18F97J94 Family devices offer a number of built-in strategies for reducing power consumption. These strategies can be particularly useful in applications, which are both power-constrained (such as battery operation), yet require periods of full-power operation for timing-sensitive routines (such as serial communications).

Aside from their low-power architecture, these devices include an expanded range of dedicated hardware features that allow the microcontroller to reduce power consumption to even lower levels when long-term hibernation is required, and still be able to resume operation on short notice.

The device has four power-saving features:

- Instruction-Based Power-Saving Modes
- Hardware-Based Power Reduction Features
- Microcontroller Clock Manipulation
- Selective Peripheral Control

Combinations of these methods can be used to selectively tailor an application's power consumption, while still maintaining critical or timing-sensitive application features. However, it is more convenient to discuss the strategies separately.

4.1 Overview of Power-Saving Modes

In addition to full-power operation, otherwise known as Run mode, PIC18F97J94 Family devices offer three instruction-based, power-saving modes and one hardware-based mode. In descending order of power consumption, they are:

- Idle
- Sleep (including retention Sleep)
- Deep Sleep (with and without retention)
- V_{BAT} (with and without RTCC)

By powering down all four modes, different functional areas of the microcontroller allow progressive reductions of operating and Idle power consumption. In addition, three of the modes can be tailored for more power reduction at a trade-off of some operating features. Table 4-1 lists all of the operating modes (including Run mode, for comparison) in order of increasing power savings and summarizes how the microcontroller exits the different modes.

5.5 Configuration Mismatch Reset (CM)

The Configuration Mismatch (CM) Reset is designed to detect, and attempt to recover from, random memory corrupting events. These include Electrostatic Discharge (ESD) events, which can cause widespread, single bit changes throughout the device and result in catastrophic failure.

In PIC18FXXJXX Flash devices, device Configuration registers (located in the configuration memory space) are continuously monitored during operation by comparing their values to complimentary shadow registers. If a mismatch is detected between the two sets of registers, a CM Reset automatically occurs. These events are captured by the $\overline{CM}$ bit (RCON<5>) being set to '0'.

This bit does not change for any other Reset event. A CM Reset behaves similarly to a Master Clear Reset, RESET instruction, WDT Time-out Reset or Stack Event Reset. As with all hard and power Reset events, the device's Configuration Words are reloaded from the Flash Configuration Words in program memory as the device restarts.

5.6 Brown-out Reset (BOR) Features

The PIC97J94 family has four different types of BOR circuits:

- Brown-out Reset (BOR)
- V_{DDCORE} Brown-out Reset (VDDBOR)
- V_{BAT} Brown-out Reset (VBATBOR)
- Deep Sleep Brown-out Reset (DSBOR)

All four BOR circuits monitor a voltage and put the device in a Reset condition while the voltage is in a specified region. SFRs will reset to the BOR state, including the Deep Sleep semaphore holding registers, DSGPR0 and DSGPR1. Upon BOR exit, the device remains in Reset until the associated trip point voltage is exceeded. Any I/O pins configured as outputs will be tri-stated. BOR, VDDBOR and DSBOR exit into Run mode; VBATBOR remains in V_{BAT} mode.

These features differ by their power mode, monitored voltage source, trip points, control and status. Refer to Table 5-1 for the PIC18F97J94 BOR differences.

TABLE 5-1: BOR FEATURE SUMMARY(1)

Feature	Mode	Source	Trip Points	Enable
BOR	Run, Idle, Sleep	V_{DDCORE}	1.6V (typ)	Always Enabled
VDDBOR	Run, Idle, Sleep	V_{DD}	V_{VDDBOR}	BOREN (CONFIG1H<0>)
VBATBOR	V_{BAT}	V_{BAT}	$V_{VBATBOR}$	VBTBOR (CONFIG7L<2>)
DSBOR	Deep Sleep	V_{DD}	V_{DSBOR}	DSBOREN (CONFIG7L<3>)

Note 1: Refer to Table for details.

REGISTER 10-20: IPR5: PERIPHERAL INTERRUPT PRIORITY REGISTER 5

U-0	R/W-1	R/W-1	R/W-1	U-0	R/W-1	R/W-1	R/W-1
—	ACTORSIP	ACTLOCKIP	TMR8IP	—	TMR6IP	TMR5IP	TMR4IP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6 **ACTORSIP:** Active Clock Tuning Out-of-Range Interrupt Priority bit
1 = High priority
0 = Low priority

bit 5 **ACTLOCKIP:** Active Clock Tuning Lock Interrupt Priority bit
1 = High priority
0 = Low priority

bit 4 **TMR8IP:** TMR8 to PR8 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 3 **Unimplemented:** Read as '0'

bit 2 **TMR6IP:** TMR6 to PR6 Match Interrupt Priority bit
1 = High priority
0 = Low priority

bit 1 **TMR5IP:** TMR5 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority

bit 0 **TMR4IP:** TMR4 to PR4 Match Interrupt Priority bit
1 = High priority
0 = Low priority

10.9 INTx Pin Interrupts

External interrupts on INT0, INT1, INT2 and INT3 are edge-triggered. INT0 is multiplexed with RB0 pin whereas INT1, INT2 and INT3 can only be used via remappable pins as shown in Table 11-13. If the corresponding INTEDGx bit in the INTCON2 register is set (= 1), the interrupt is triggered by a rising edge. If that bit is clear, the trigger is on the falling edge.

When a valid edge appears on the RBx/INTx pin, the corresponding flag bit, INTxIF, is set. This interrupt can be disabled by clearing the corresponding enable bit, INTxIE. Before re-enabling the interrupt, the flag bit (INTxIF) must be cleared in software in the Interrupt Service Routine.

All external interrupts (INT0, INT1, INT2 and INT3) can wake-up the processor from the power-managed modes if bit, INTxIE, was set prior to going into the power-managed modes. If the Global Interrupt Enable bit (GIE) is set, the processor will branch to the interrupt vector following wake-up.

The interrupt priority for INT1, INT2 and INT3 is determined by the value contained in the Interrupt Priority bits, INT1IP (INTCON3<6>), INT2IP (INTCON3<7>) and INT3IP (INTCON2<1>).

There is no priority bit associated with INT0. It is always a high-priority interrupt source.

10.10 TMR0 Interrupt

In 8-bit mode (the default), an overflow in the TMR0 register (FFh → 00h) will set flag bit, TMR0IF. In 16-bit mode, an overflow in the TMR0H:TMR0L register pair (FFFFh → 0000h) will set TMR0IF.

The interrupt can be enabled/disabled by setting/clearing enable bit, TMR0IE (INTCON<5>). Interrupt priority for Timer0 is determined by the value contained in the interrupt priority bit, TMR0IP (INTCON2<2>). For further details on the Timer0 module, see **Section 14.0 "Timer0 Module"**.

10.11 Edge-Selectable Interrupt-on-Change

Interrupt-on-change pins are selected via the PPS register settings and have the option of generating an interrupt on positive or negative transitions, or both. Positive edge events are enabled by setting the corresponding bits in the IOCP register, while negative edge events are enabled by setting the corresponding bits in the IOCN register. For compatibility with the previous interrupt-on-change feature, both the IOCP and IOCN bits should be set. The interrupt can be enabled by setting/clearing the IOCIE (INTCON<3>) bit. Each individual pin can be disabled by clearing both of the corresponding IOCN/IOCP bits. A change event (either positive or negative edge) will cause the corresponding IOCF flag to be set.

Interrupt priority for the edge selectable interrupt-on-change is determined by the interrupt priority bit, IOCIP (INTCON2<0>).

TABLE 11-9: PORTJ FUNCTIONS (CONTINUED)

Pin Name	Function	TRIS Setting	I/O	I/O Type	Description
RJ6/SEG37/$\overline{LB}$	RJ6	0	O	DIG	LATJ<6> data output.
		1	I	ST	PORTJ<6> data input.
	SEG37	0	O	ANA	LCD Segment 37 output; disables all other pin functions.
	$\overline{LB}$	x	O	DIG	External Memory Bus Lower Byte ($\overline{LB}$) signal.
RJ7/SEG36/$\overline{UB}$	RJ7	0	O	DIG	LATJ<7> data output.
		1	I	ST	PORTJ<7> data input.
	SEG36	0	O	ANA	LCD Segment 36 output; disables all other pin functions.
	$\overline{UB}$	x	O	DIG	External Memory Bus Upper Byte ($\overline{UB}$) signal.

Legend: O = Output, I = Input, ANA = Analog Signal, DIG = Digital Output, ST = Schmitt Trigger Buffer Input,
x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

REGISTER 11-4: PSPCON: PARALLEL SLAVE PORT CONTROL REGISTER

R-0	R-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
IBF	OBF	IBOV	PSPMODE	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **IBF:** Input Buffer Full Status bit
1 = A word has been received and is waiting to be read by the CPU
0 = No word has been received

bit 6 **OBF:** Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read

bit 5 **IBOV:** Input Buffer Overflow Detect bit
1 = A write occurred when a previously input word had not been read (must be cleared in software)
0 = No overflow occurred

bit 4 **PSPMODE:** Parallel Slave Port Mode Select bit
1 = Parallel Slave Port mode
0 = General Purpose I/O mode

bit 3-0 **Unimplemented:** Read as ‘0’

FIGURE 11-4: PARALLEL SLAVE PORT WRITE WAVEFORMS

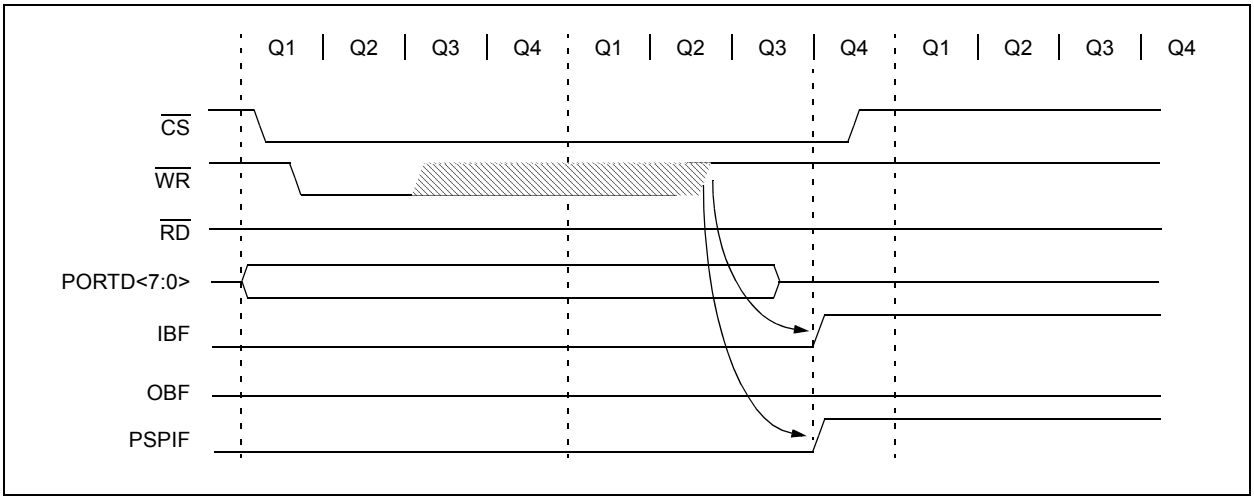
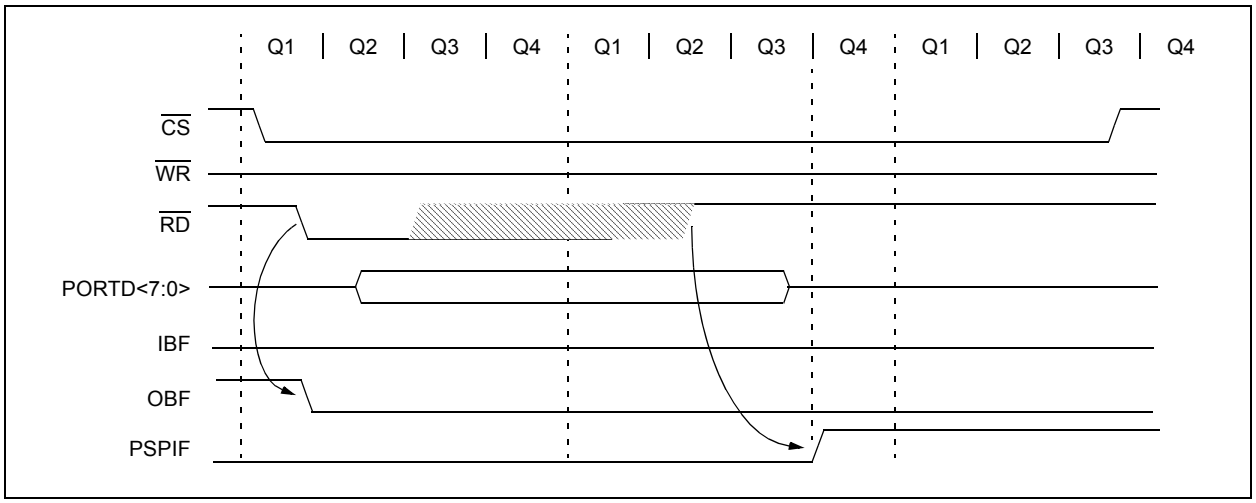


FIGURE 11-5: PARALLEL SLAVE PORT READ WAVEFORMS



11.14 Virtual PORT

This device includes a single virtual port, which is used to construct a logically addressed 8-bit PORT from 8 physically unrelated pins on the device. The virtual PORT is controlled through the PORTVP, LATVP and TRISVP registers. These function identically to the PORT, LAT and TRIS registers of the actual I/O ports. Refer to **Section 11.1 "I/O Port Pin Capabilities"** for more information.

11.15 PPS-Lite

Previous PIC18 devices had I/O pins that were "hard-wired" to a set of peripherals. For example, a port pin might have had the option of serving as an I/O pin, an analog input or as an interrupt source. In an effort to increase the flexibility of the parts, PIC18FXXJ94 devices contain PPS-Lite (Peripheral Pin Select-Lite), which allows the developer to connect an internal peripheral to a subset of pins. PPS-Lite is similar to PPS (available on PIC18F products), but limits the user to interconnections within four sets of pin/peripheral groups.

The PPS-Lite feature allows some flexibility in choosing which peripheral connects to any particular pin. This allows designs to be maximized for layout efficiency, and also may allow component changes without changing the printed circuit board design. The Peripheral Pin Select feature operates over a fixed subset of digital I/O pins (those designated as RPn pins). Users may independently map the input and/or output of most digital peripherals to a limited set of these I/O pins. The PPS-Lite configuration is performed in software and does not require the device to be reprogrammed. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.15.1 AVAILABLE PINS

The PPS-Lite feature is used with a range of pins. All devices in the PIC18FXXJ94 family contain a total of 47 remappable peripheral pins, labeled RP0 through RP46. Pins that support PPS-Lite feature include the designation, "RPn" in their full pin designation, where "RP" designates a remappable peripheral and "n" is the remappable pin number. For PIC18FXXJ94 devices, RP41 through RP45 are digital inputs only.

11.15.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all "digital only" peripherals. These include general serial communications (USART and SPI), general purpose timer clock inputs, timer related peripherals (input capture and output compare) and external interrupt inputs.

In comparison, some digital only peripheral modules are not currently included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include I^2C, USB, change notification inputs, RTCC alarm output and all modules with analog inputs, such as the A/D Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given, regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

15.0 TIMER1/3/5 MODULES

The Timer1/3/5 timer/counter modules incorporate these features:

- Software-selectable operation as a 16-bit timer or counter
- Readable and writable 8-bit registers (TMRxH and TMRxL)
- Selectable clock source (internal or external) with device clock or SOSC Oscillator internal options
- Interrupt-on-overflow
- Module Reset on ECCP Special Event Trigger

Note: Throughout this section, generic references are used for register and bit names that are the same – except for an 'x' variable that indicates the item's association with the Timer1, Timer3 or Timer5 module. For example, the control register is named TxCON and refers to T1CON, T3CON and T5CON.

A simplified block diagram of the Timer1/3/5 module is shown in Figure 15-1.

The Timer1/3/5 module is controlled through the TxCON register (Register 15-1). It also selects the clock source options for the ECCP modules. (For more information, see **Section 18.1.1 "ECCP Module and Timer Resources"**).

The FOSC clock source should not be used with the ECCP capture/compare features. If the timer will be used with the capture or compare features, always select one of the other timer clocking options.

15.6 Timer1/3/5 Interrupt

The TMRx register pair (TMRxH:TMRxL) increments from 0000h to FFFFh and overflows to 0000h. The Timerx interrupt, if enabled, is generated on overflow and is latched in the interrupt flag bit, TMRxIF. Table 15-3 gives each module's flag bit.

TABLE 15-3: TIMER1/3/5 INTERRUPT FLAG BITS

Timer Module	Flag Bit
1	PIR1<0>
3	PIR2<1>
5	PIR5<1>

This interrupt can be enabled or disabled by setting or clearing the TMRxIE bit, respectively. Table 15-4 gives each module's enable bit.

TABLE 15-4: TIMER1/3/5 INTERRUPT ENABLE BITS

Timer Module	Flag Bit
1	PIE1<0>
3	PIE2<1>
5	PIE5<1>

15.7 Resetting Timer1/3/5 Using the ECCP Special Event Trigger

If the ECCP modules are configured to use Timerx and to generate a Special Event Trigger in Compare mode (CCPxM<3:0> = 1011), this signal will reset Timerx. The trigger from ECCP2 will also start an A/D conversion if the A/D module is enabled (For more information, see **Section 18.3.4 "Special Event Trigger"**.)

The module must be configured as either a timer or synchronous counter to take advantage of this feature. When used this way, the CCPRxH:CCPRxL register pair effectively becomes a Period register for Timerx.

If Timerx is running in Asynchronous Counter mode, the Reset operation may not work.

In the event that a write to Timerx coincides with a Special Event Trigger from an ECCP module, the write will take precedence.

Note:	The Special Event Triggers from the ECCPx module will only clear the TMR3 register's content, but not set the TMR3IF interrupt flag bit (PIR1<0>).

Note:	The CCP and ECCP modules use Timers, 1 through 8, for some modes. The assignment of a particular timer to a CCP/ECCP module is determined by the Timer to CCP enable bits in the CCPTMRSx registers. For more details, see Register 18-2, Register 18-3 and Register 19-2

17.0 REAL-TIME CLOCK AND CALENDAR (RTCC)

The key features of the Real-Time Clock and Calendar (RTCC) module are:

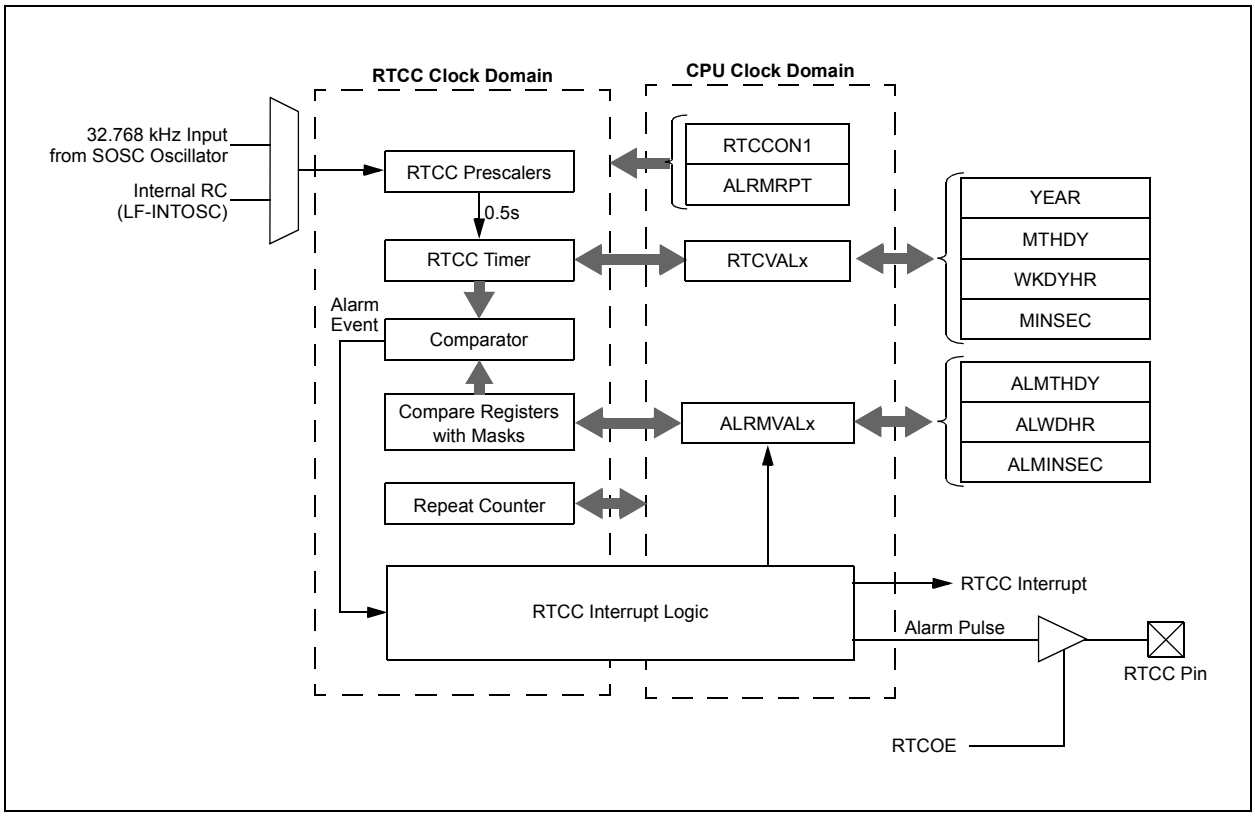
- Hardware Real-Time Clock and Calendar (RTCC)
- Provides hours, minutes and seconds using 24- hour format
- Visibility of one-half second period
- Provides calendar – weekday, date, month and year
- Alarm configurable for half a second, one second, 10 seconds, one minute, 10 minutes, one hour, one day, one week or one month
- Alarm repeat with decrementing counter
- Alarm with indefinite repeat – chime
- Year 2000 to 2099 leap year correction
- BCD format for smaller software overhead
- Optimized for long term battery operation
- Fractional second synchronization
- Multiple clock sources
  - SOSC
  - LPRC
  - 50 Hz
  - 60 Hz
- User calibration of the 32.768 kHz clock crystal frequency with periodic auto-adjust
- Calibration to within ±2.64 seconds error per month
- Calibrates up to 260 ppm of crystal error

The RTCC module is intended for applications where accurate time must be maintained for an extended period with minimum to no intervention from the CPU. The module is optimized for low-power usage in order to provide extended battery life, while keeping track of time.

The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

Hours are measured in 24-hour (military time) format. The clock provides a granularity of one second with half-second visibility to the user.

FIGURE 17-1: RTCC BLOCK DIAGRAM



21.3.2 EUSARTx SYNCHRONOUS MASTER RECEPTION

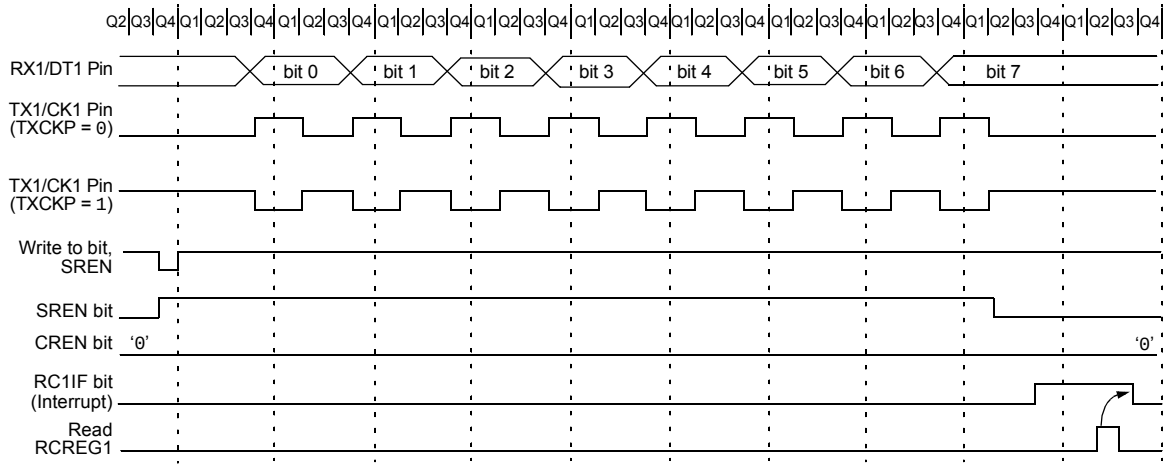
Once Synchronous mode is selected, reception is enabled by setting either the Single Receive Enable bit, SREN (RCSTAx<5>) or the Continuous Receive Enable bit, CREN (RCSTAx<4>). Data is sampled on the RXx pin on the falling edge of the clock.

If enable bit, SREN, is set, only a single word is received. If enable bit, CREN, is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

1. Initialize the SPBRGHx:SPBRGx registers for the appropriate baud rate. Set or clear the BRG16 bit, as required, to achieve the desired baud rate.
2. Enable the Master Synchronous Serial Port by setting bits, SYNC, SPEN and CSRC.
3. Ensure bits, CREN and SREN, are clear.
4. If interrupts are desired, set enable bit, RCxIE.
5. If 9-bit reception is desired, set bit, RX9.
6. If a single reception is required, set bit, SREN. For continuous reception, set bit, CREN.
7. Interrupt flag bit, RCxIF, will be set when reception is complete and an interrupt will be generated if the enable bit, RCxIE, was set.
8. Read the RCSTAx register to get the 9th bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREGx register.
10. If any error occurred, clear the error by clearing bit CREN.
11. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 21-13: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit, SREN = 1, and bit, BRGH = 0. This example is equally applicable to EUSART2 (TX2/CK2 and RX2/DT2).

REGISTER 22-6: ADCON2H: A/D CONTROL REGISTER 2 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PVCFG1	PVCFG0	NVCFG0	OFFCAL	BUFREGEN	CSCNA	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **PVCFG<1:0>:** Converter Positive Voltage Reference Configuration bits
1x =Unimplemented, do not use
01 =External V_{REF+}
00 =AV_{DD}

bit 5 **NVCFG0:** Converter Negative Voltage Reference Configuration bit
1 = External V_{REF-}
0 = AV_{SS}

bit 4 **OFFCAL:** Offset Calibration Mode Select bit
1 = Inverting and non-inverting inputs of channel Sample-and-Hold are connected to AV_{SS}
0 = Inverting and non-inverting inputs of channel Sample-and-Hold are connected to normal inputs

bit 3 **BUFREGEN:** A/D Buffer Register Enable bit
1 = Conversion result is loaded into the buffer location determined by the converted channel
0 = A/D result buffer is treated as a FIFO

bit 2 **CSCNA:** Scan Input Selections for CH0+ During Sample A bit
1 = Scans inputs
0 = Does not scan inputs

bit 1-0 **Unimplemented:** Read as '0'

FIGURE 22-15: OUTSIDE WINDOW COMPARISON OPERATION (UNDER THRESHOLD 1)

Before Conversion and Comparison

ADC1BUF15	—
ADC1BUF14	—
ADC1BUF13	—
ADC1BUF12	—
ADC1BUF11	—
ADC1BUF10	Threshold 2
ADC1BUF9	—
ADC1BUF8	—
ADC1BUF7	—
ADC1BUF6	—
ADC1BUF5	—
ADC1BUF4	—
ADC1BUF3	—
ADC1BUF2	Threshold 1
ADC1BUF1	—
ADC1BUF0	—

After Conversion and Comparison

	Compare Only (‘10’)	Compare and Store (‘01’)
ADC1BUF15	—	—
ADC1BUF14	—	—
ADC1BUF13	—	—
ADC1BUF12	—	—
ADC1BUF11	—	—
ADC1BUF10	Threshold 2	Threshold 2
ADC1BUF9	—	—
ADC1BUF8	—	—
ADC1BUF7	—	—
ADC1BUF6	—	—
ADC1BUF5	—	—
ADC1BUF4	—	—
ADC1BUF3	—	—
ADC1BUF2	Threshold 1	**Conversion Value**
ADC1BUF1	—	—
ADC1BUF0	—	—

AD1CHITL							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

AD1CHITL							
15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	6	5	4	3	**2**	1	0
0	0	0	0	0	**1**	0	0

22.8 Examples

22.8.1 INITIALIZATION

Example 22-1 shows a simple initialization code example for the A/D module. Operation in Idle mode is disabled, output data is in unsigned fractional format, and AVDD and AVSS are used for VR+ and VR-. The start of sampling, as well as the start of conversion (conversion trigger), are performed directly in software. Scanning of inputs is disabled and an interrupt occurs after every sample/convert sequence (one conversion result) with only one channel (AN0) being converted. The A/D conversion clock is TCY/2.

In this particular configuration, all 16 analog input pins are set up as analog inputs. It is important to note that with this A/D module, I/O pins are configured for analog or digital operation at the I/O port with the ANSn Analog Select registers. The use of these registers is described in detail in the I/O Port chapter of the specific device data sheet.

This example shows one method of controlling a sample/convert sequence by manually setting and clearing the SAMP bit (ADCON1L<1>). This method, among others, is more fully discussed in **Section 22.4 “Controlling the Sampling Process”** and **Section 22.5 “Controlling the Conversion Process”**.

EXAMPLE 22-6: CONVERTING A SINGLE CHANNEL, ONCE PER INTERRUPT, DUAL BUFFER MODE

A/D Configuration:

- Select AN3 for S/H+ Input (CH0SA<4:0> = 00011)
- Select VR- for S/H- Input (CH0NA<2:0> = 000)
- Configure for No Input Scan (CSCNA = 0)
- Use Only MUX A for Sampling (ALTS = 0)
- Set AD1IF on Every Sample (SMPI<4:0> = 00000)
- Configure Buffer as Dual, 8-Word Segments (BUFM = 1)

Operational Sequence:

1. Sample MUX A Input, AN3; Convert and Write to Buffer 0h.
2. Set AD1IF Flag (and generate interrupt, if enabled); Write Access Automatically Switches to Alternate Buffer.
3. Sample MUX A Input, AN3; Convert and Write to Buffer 8h.
4. Set AD1IF Flag (and generate interrupt, if enabled); Write Access Automatically Switches to Alternate Buffer.
5. Repeat (1-4).

Results Stored in Buffer (after 2 cycles):

Buffer Address	Buffer Contents at 1st AD1IF Event	Buffer Contents at 2nd AD1IF Event
ADC1BUF0	Sample 1 (AN3, Sample 1)	(undefined)
ADC1BUF1	(undefined)	(undefined)
ADC1BUF2	(undefined)	(undefined)
ADC1BUF3	(undefined)	(undefined)
ADC1BUF4	(undefined)	(undefined)
ADC1BUF5	(undefined)	(undefined)
ADC1BUF6	(undefined)	(undefined)
ADC1BUF7	(undefined)	(undefined)
ADC1BUF8	(undefined)	Sample 2 (AN3, Sample 2)
ADC1BUF9	(undefined)	(undefined)
ADC1BUFA	(undefined)	(undefined)
ADC1BUFB	(undefined)	(undefined)
ADC1BUFC	(undefined)	(undefined)
ADC1BUFD	(undefined)	(undefined)
ADC1BUFE	(undefined)	(undefined)
ADC1BUFF	(undefined)	(undefined)

22.8.3.1 Using Alternating MUX A and MUX B Input Selections

Figure 22-19 and Example 22-7 demonstrate alternate sampling of the inputs assigned to MUX A and MUX B. Setting the ALTS bit enables alternating input selections. The first sample uses the MUX A inputs specified by the CH0SAx and CH0NAx bits. The next sample uses the MUX B inputs, specified by the CH0SBx and CH0NBx bits.

This example also demonstrates use of the dual, 8-word buffers. An interrupt occurs after every 8th sample, resulting in filling eight words into the buffer on each interrupt.

23.7 Comparator Operation During Sleep

When a comparator is active and the device is placed in Sleep mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake-up the device from Sleep mode when enabled. Each operational comparator will consume additional current.

To minimize power consumption while in Sleep mode, turn off the comparators (CON = 0) before entering Sleep. If the device wakes up from Sleep, the contents of the CMxCON register are not affected.

23.8 Effects of a Reset

A device Reset forces the CMxCON registers to their Reset state. This forces both comparators and the voltage reference to the OFF state.

REGISTER 28-9: CONFIG5H: CONFIGURATION REGISTER 5 HIGH (BYTE ADDRESS 300009h)

U-1	U-1	U-1	U-1	R/WO-1	R/WO-1	R/WO-1	R/WO-1
—	—	—	—	MSSPMSK1	MSSPMSK2	LS48MHZ	IOL1WAY
bit 7							bit 0

Legend:	P = Programmable bit	WO = Write-Once bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-4 **Unimplemented:** Program the corresponding Flash Configuration bit to '1'

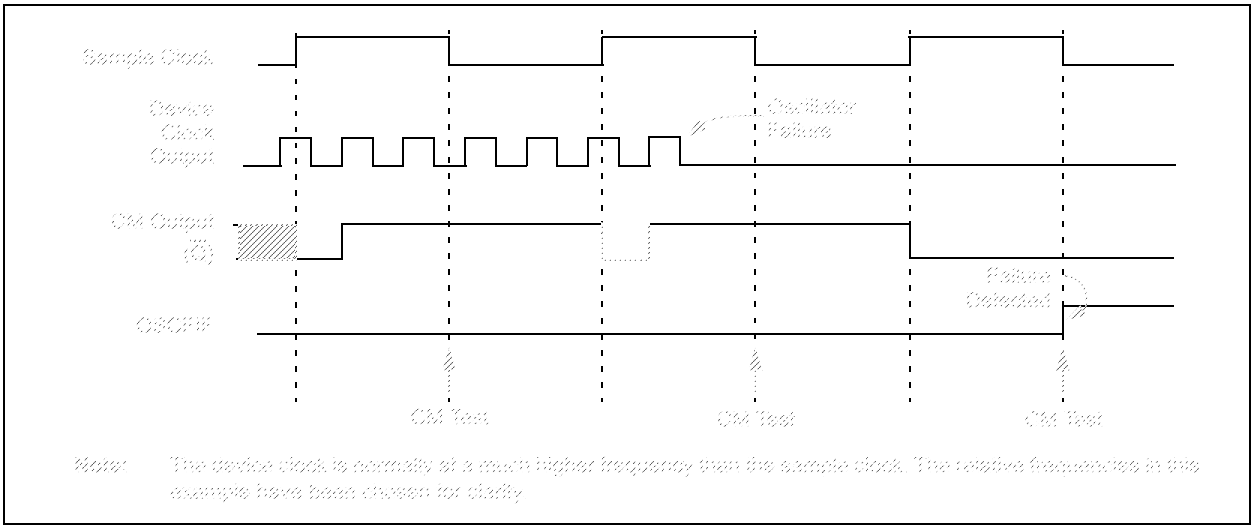
bit 3 **MSSPMSK1:** MSSP1 7-Bit Address Masking Mode Enable bit
1 = 7-Bit Address Masking mode enable
0 = 5-Bit Address Masking mode enable

bit 2 **MSSPMSK2:** MSSP2 7-Bit Address Masking Mode Enable bit
1 = 7-Bit Address Masking mode enable
0 = 5-Bit Address Masking mode enable

bit 1 **LS48MHZ:** Low-Speed USB Clock Selection bit
1 = 48 MHz system clock is expected; divide-by-8 generates low-speed USB clock
0 = 24 MHz system clock is expected; divide-by-4 generates low-speed USB clock

bit 0 **IOL1WAY:** IOLOCK Bit One-Way Set Enable bit
1 = The IOLOCK bit can only be set once (provided an unlocking sequence is executed); this prevents any possible future RP register changes
0 = The IOLOCK bit can be set and cleared as needed (provided an unlocking sequence is executed)

FIGURE 28-4: FSCM TIMING DIAGRAM



28.4.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexer selects the clock source selected by the OSCCON register. Fail-Safe Clock Monitoring of the power-managed clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTOSC multiplexer. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, subsequent interrupts while in Idle mode will cause the CPU to begin executing instructions while being clocked by the INTOSC source.

28.4.4 POR OR WAKE FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is EC, RC or INTOSC modes, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, HSPLL, LP or MS), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FCSM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the device clock and functions until the primary clock is stable (when the OST and PLL timers have timed out).

This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTOSC returns to its role as the FSCM source.

Note:	The same logic that prevents false oscillator failure interrupts on POR, or wake from Sleep, also prevents the detection of the oscillator's failure to start at all following these events. This is avoided by an OST time-out condition and by using a timing routine to determine if the oscillator is taking too long to start. Even so, no oscillator failure interrupt will be flagged.

As noted in **Section 28.3.1 "Special Considerations for Using Two-Speed Start-up"**, it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new power-managed mode is selected, the primary clock is disabled.

ADDWFC **ADD W and Carry bit to f**

Syntax: ADDWFC f {,d {,a}}

Operands: $0 \le f \le 255$
$d \in [0,1]$
$a \in [0,1]$

Operation: (W) + (f) + (C) → dest

Status Affected: N,OV, C, DC, Z

Encoding:

0010	00da	ffff	ffff

Description: Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank.

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See **Section 29.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `ADDWFC REG, 0, 1`

Before Instruction
Carry bit = 1
REG = 02h
W = 4Dh
After Instruction
Carry bit = 0
REG = 02h
W = 50h

ANDLW **AND Literal with W**

Syntax: ANDLW k

Operands: $0 \le k \le 255$

Operation: (W) .AND. k → W

Status Affected: N, Z

Encoding:

0000	1011	kkkk	kkkk

Description: The contents of W are ANDed with the 8-bit literal 'k'. The result is placed in W.

Words: 1

Cycles: 1

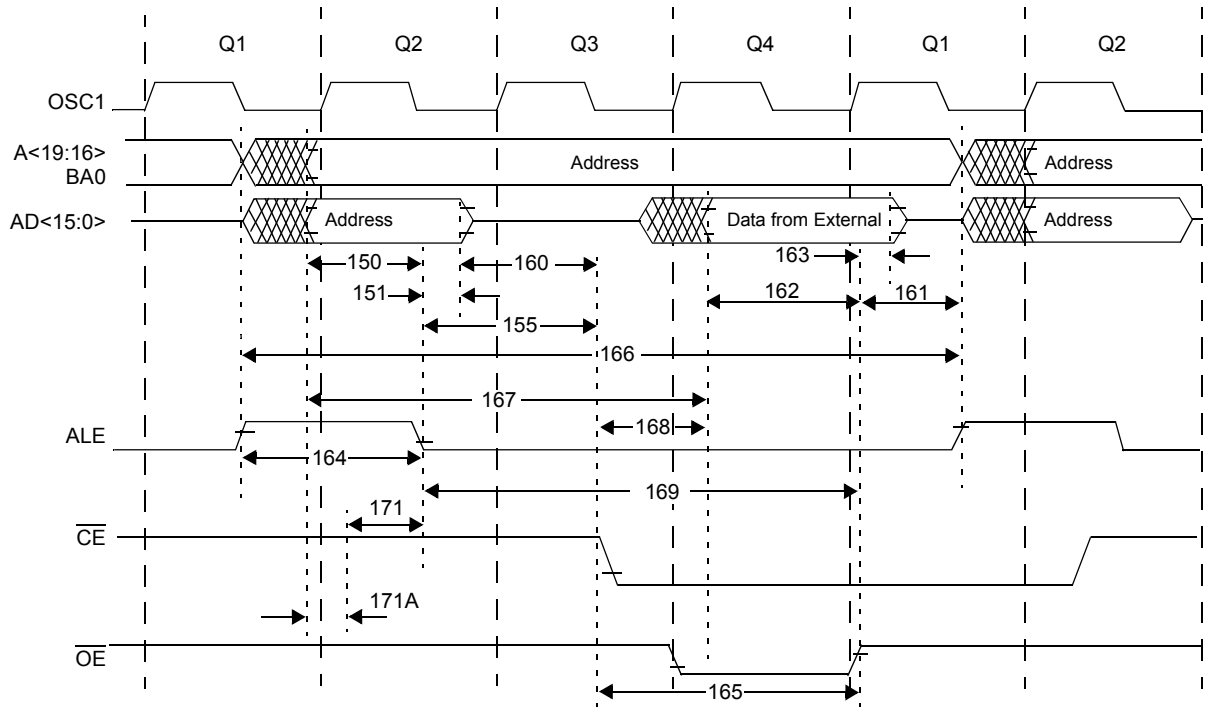
Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to W

Example: `ANDLW 05Fh`

Before Instruction
W = A3h
After Instruction
W = 03h

FIGURE 30-6: PROGRAM MEMORY READ TIMING DIAGRAM



Operating Conditions: 2.0V < VCC < 3.6V, -40°C < TA < +125°C unless otherwise stated.

TABLE 30-25: CLKO AND I/O TIMING REQUIREMENTS

Param. No.	Symbol	Characteristics	Min.	Typ.	Max.	Units
150	TadV2alL	Address Out Valid to ALE ↓ (address setup time)	0.25 TCY – 10	—	—	ns
151	TalL2adl	ALE ↓ to Address Out Invalid (address hold time)	5	—	—	ns
155	TalL2oeL	ALE ↓ to $\overline{OE}$ ↓	10	0.125 TCY	—	ns
160	TadZ2oeL	A/D High-Z to $\overline{OE}$ ↓ (bus release to $\overline{OE}$)	0	—	—	ns
161	ToeH2adD	$\overline{OE}$ ↑ to A/D Driven	0.125 TCY – 5	—	—	ns
162	TadV2oeH	LS Data Valid before $\overline{OE}$ ↑ (data setup time)	20	—	—	ns
163	ToeH2adl	$\overline{OE}$ ↑ to Data In Invalid (data hold time)	0	—	—	ns
164	TalH2alL	ALE Pulse Width	—	0.25 TCY	—	ns
165	ToeL2oeH	$\overline{OE}$ Pulse Width	0.5 TCY – 5	0.5 TCY	—	ns
166	TalH2alH	ALE ↑ to ALE ↑ (cycle time)	—	TCY	—	ns
167	Tacc	Address Valid to Data Valid	0.75 TCY – 25	—	—	ns
168	Toe	$\overline{OE}$ ↓ to Data Valid		—	0.5 TCY – 25	ns
169	TalL2oeH	ALE ↓ to $\overline{OE}$ ↑	0.625 TCY – 10	—	0.625 TCY + 10	ns
171	TalH2csL	Chip Enable Active to ALE ↓	0.25 TCY – 20	—	—	ns
171A	TubL2oeH	A/D Valid to Chip Enable Active	—	—	10	ns